The EXOGAM Escape Suppression Shield (ESS) Card

Contents:

1.0 Introduction

The EXOGAM segmented Clover Ge detectors will all use escape suppression shields made of Bismuth Germanate (BGO) at the sides and Caesium Iodide (CsI) as back-catchers. The number of BGO crystals in the shield will vary depending on whether EXOGAM is operating in its close packed mode or its normal mode, but the phototubes will be ganged together to give 4 outputs from the side pieces and another 4 from the back catcher in both cases. All that will change is that extra phototubes will be added to the daisy chain when the extra side pieces of BGO are added.

The HV will be daisy chained between phototubes with a small potentiometer provided on each base for gain matching. It will not be possible to individually switch HV on/off to gain match or test individual phototubes via this VXI card.

The 8 signals from a shield will be handled by a single channel of electronics which will measure the sum energy of all 8 inputs and the timing of each quarter of the shield measured against its respective Ge CFD. In addition to energy and timing, a 12 bit hit pattern will be generated from each shield and its associated Clover Ge. All inputs can be time-aligned before incorporation into the pattern or use in TDCs.

Four Vetos will be provided from each shield (one per Ge crystal) for the associated Ge cards. The user may select whether each Veto is generated from all the shield elements (i.e. all 4 are the same) or generated individually from just the quarter nearest its Ge crystal. The user may also select whether the Veto is derived from the side pieces alone, the back catcher alone or from the back catcher and side pieces taken together. The timing (delay and width) of each veto will be adjustable for optimum suppression.

The ESS card is designed primarily to enhance the Ge peak-total, hence the name, Escape Suppression Shield (ESS) card. The card will also measure the shield's sum energy in the range 0-20MeV. The ESS card's prime purpose is providing good Veto information.

The signals from the phototubes to the ESS card will be driven from buffers in the HV distribution box mounted close to the shield. The signals will be amplified and driven by line drivers, in the preamplifiers, along cables to the ESS card. There will be no shaping in the preamplifiers to reduce the signal delays and therefore give the best timing. All signal shaping will take place within the ESS card.

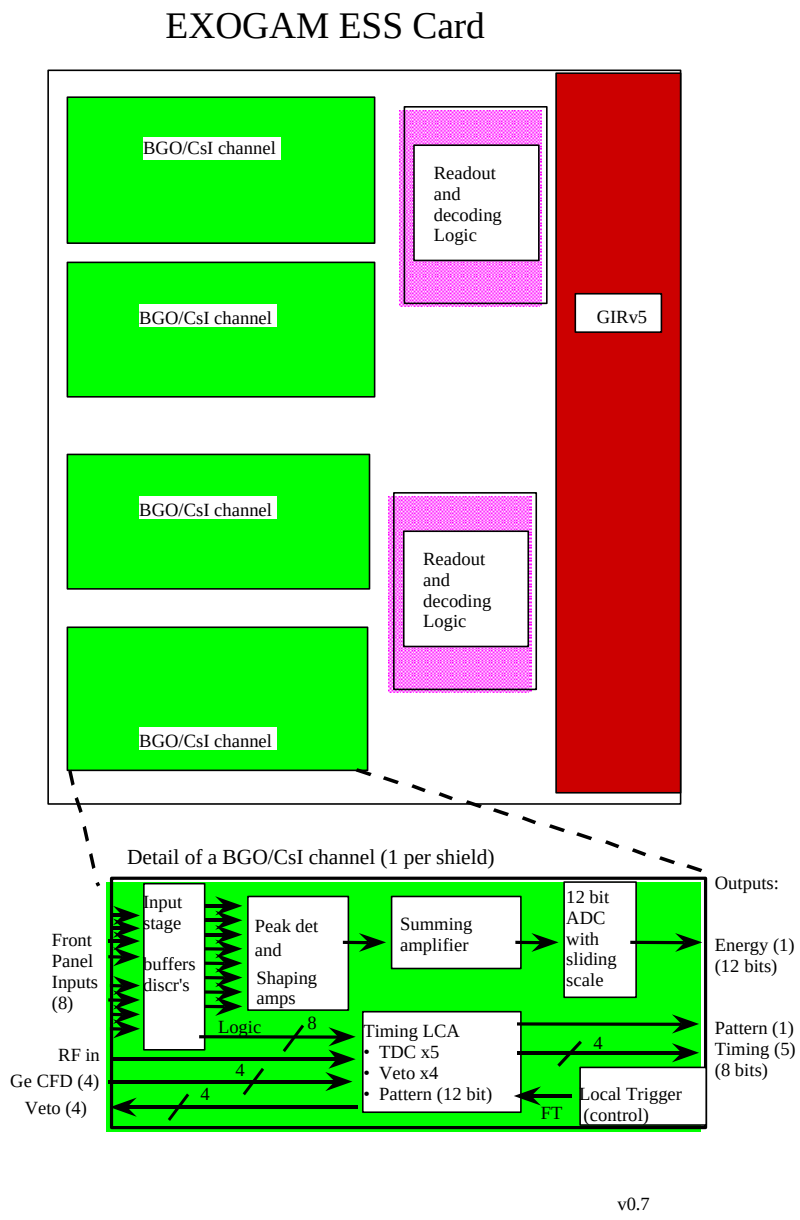
A front panel sumbus output will be provided generating 4mA/active shield.

Each ESS card will instrument 4 complete escape suppression shields.

v1.1 (Changed October 1999 following changes agreed by the September 1999 Exogam Steering Committee meeting)
Last revised to add pinouts for front panel connectors 10th November 2000

Written by Ian Lazarus, CLRC Daresbury Lab, Warrington WA4 4AD, UK

2.0 General Architecture



v0.7

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Last revised to add pinouts for front panel connectors 10th November 2000

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3.0 Details of signal processing and adjustable parameters.

Initial calculations and estimates suggest that for 137Cs (662keV) we will obtain about 240 photoelectrons from the BGO crystals (and 1900 from the CsI(Na) backcatcher. The noise threshold from the shield (at the preamplifier output) is expected to be 20-25keV.

3.1 Input Stage:

The signals from the PMTs will be received from preamps containing a x20 gain stage (with no shaping) and line drivers. The inputs will be buffered to shaping amplifiers with peak detectors for energy measurements. For timing the PMT signals will be amplified (x20) and connected to 8 leading edge discriminators to obtain 8 logic outputs which will be connected to the timing LCA.

The 8 logic signals will comprise four discriminator outputs fired by the 4 groups of BGO side pieces associated with each of the 4 Ge crystals, and four from the discriminators fired by the CsI back catchers. Each of the 8 inputs will have its own independent threshold adjustment. The input signals will be amplified before the discriminators to reduce timing walk and allow veto thresholds to be set just above the noise (typical minimum useable threshold will be 25keV).

Adjustment:

• The 8 discriminators will each be adjustable over the range 0 to 250keV in 1 keV steps. (not calibrated) (DAC range 0 to +1V)

3.2 Alignment LCA

New in this revision (v1.0) is the alignment LCA. This module takes the 12 logic signals from the 8 input stage discriminators and the 4 Ge CFD inputs as inputs. The outputs are delayed copies of each input signal, delayed by a software selectable period in the range 10 to 650ns, in steps of 10ns. The pulse width is not affected except to be rounded to the nearest 10ns. The inputs and outputs of this LCA are available on logic inspection lines to enable the users to perform this alignment remotely.

The Local Trigger start signal is also generated in this LCA and is the logical OR of all 8 BGO/CsI inputs. Optionally, under software control, the Local Trigger start can include the OR of the Ge CFD inputs too so that patterns in the Ge can be recorded regardless of whether the shield was hit.

Adjustments:

- BGO1 alignment delay (10-650ns in 10ns steps)
- BGO2 alignment delay (10-650ns in 10ns steps)
- BGO3 alignment delay (10-650ns in 10ns steps)
- BGO4 alignment delay (10-650ns in 10ns steps)
- CsI1 alignment delay (10-650ns in 10ns steps)
- CsI2 alignment delay (10-650ns in 10ns steps)
- CsI3 alignment delay (10-650ns in 10ns steps)
- CsI4 alignment delay (10-650ns in 10ns steps)
- Ge1 alignment delay (10-650ns in 10ns steps)
- Ge2 alignment delay (10-650ns in 10ns steps)
- Ge3 alignment delay (10-650ns in 10ns steps)
- Ge4 alignment delay (10-650ns in 10ns steps)
- Control bit for LT start [BGO/CsI only (=0) LT start from Ge OR BGO/CsI (=1)]

3.3 Timing LCA

The timing LCA will perform 3 functions: firstly it contains 5 TDCs, secondly it generates 4 Vetos, and thirdly it generates a hit pattern.

The TDC range will be 2.5μs with a step size of 10ns. The first 4 TDCs (Ge-ESS TDCs) will each be started by their associated Ge crystal's CFD and stopped by a delayed version of one of these 6 logic signals (selected by software):

- BGO discriminator output from nearest quarter only
- BGO discriminator output from whole shield
- CsI discriminator output from nearest quarter only
- CsI discriminator output from whole shield
- Logical OR of BGO + CsI discriminator outputs from nearest quarter
- Logical OR of BGO + CsI discriminator outputs from whole shield

The delay in the stop signal will not be adjustable. Its nominal value will be 900ns. If the Ge and the shield fire simultaneously, the TDC will measure just the STOP delay of 900ns. The TDC can record shield events up to 900ns before and 1600ns after the Ge fires.
(The delay is biased towards the time after the Ge fired so that the slower CsI signals are not lost.)

A 5th TDC will be included (2.5μs range, 10ns step size) using one of the following 3 logic signals (selected by software) as the start:

- BGO discriminator output from whole shield
- CsI discriminator output from whole shield
- Logical OR of BGO + CsI discriminator outputs from whole shield

The TDC will stopped by either RF or the system's Fast Trigger pulse (back edge). The stop signal is also selected by software.

The Veto pulses will be started by whichever logic condition is selected to stop the Ge-ESS TDCs:

- BGO from nearest quarter only
- BGO from whole shield
- CsI from nearest quarter only
- CsI from whole shield
- Logical OR of CsI and BGO from nearest quarter only
- Logical OR of CsI and BGO from whole shield

The width of Vetos will be adjustable by software to obtain optimum suppression in steps of 20ns from 0 to 1200ns. (Common adjustment within each shield.). The Veto output pulse will not be delayed.

A pattern will be generated for each Clover comprising Ge CFDs, BGO and CsI discriminators, a total of 12 bits (3 bits from each of 4 Ge crystals). The pattern will be generated by starting a local coincidence window when the first of the 12 inputs is detected. The width of the coincidence window will be programmable in 20ns steps up to a maximum of 1200ns.

Adjustments (common to all 4 Vetos) :

The Veto and TAC stop selected to come from BGO, CsI, (BGO OR CsI) or none.
The Veto and TAC stop selected to come from quarter of shield or whole shield.
Veto width in range 0 - 1200ns in steps of 20ns.

Local coincidence window (for pattern) 0-1200ns in 20ns steps

3.4 Energy Measurement

The 8 analogue signals in the input stage will be integrated using simple integrating shaping amplifiers whose outputs are gated from the time the associated discriminator fires for a period of 1.5µs for BGO and 3µs for CsI. The BGO peak is held for a further 1.5µs with its gate closed until the CsI input has been integrated for 3µs. The sum of the BGO and CsI peaks is transferred to the ADC. The peak hold capacitors are discharged after the ADC convert command is issued.

The peak detector gate and hold signals will be reset by one of the following situations:

- failure of FT or Validation sample point to coincide with FT or Val pulse
- event reject signal being active
- successful completion 3µs charge collection period (normal reset)
- watchdog timeout (error recovery condition)

The energy output will be a single sum energy measurement for the whole shield (side and back). The energy range to be measured is 0 to 20MeV to account for direct hits in the CsI back catcher even though the Compton scattered spectra are all in the 0-2MeV range. With a 12 bit ADC this equates to 5keV/channel, so for the minimum expected discriminator threshold (25keV) the resolution is 20%.

Adjustment:

• There are no adjustments in the energy channel.

3.5 ADC

The ADC will be in a module containing a Burr Brown ADS 7800 coder with its own independent sliding scale correction. The output will be 12 bits. Input voltage 0 to +5V.

Adjustment:

• The ADC sliding scale can be set to 0 or 255 for calibration (no adjustments in normal usage)

3.6 Readout of parameters:

Each parameter will be associated with an item number (to identify the parameter as energy, timing or pattern) and a group number (to identify the shield). The following parameters may be read from each channel (each shield):

Energy:	0 - 20MeV in 4k channels
Timing A:	0 - 2.5us in 256 channels
Timing B:	0 - 2.5us in 256 channels
Timing C:	0 - 2.5us in 256 channels
Timing D:	0 - 2.5us in 256 channels
Timing E:	0 - 2.5us in 256 channels
Pattern:	12 bits (BGO_1, BGO_2, BGO_3, BGO_4, CsI_1, CsI_2, CsI_3, CsI_4, Ge_1, Ge_2, Ge_3, Ge_4)

Adjustment:

• The readout of each parameter (Energy, Timing and Pattern) has its own enable/disable.

3.7 Control (Local Trigger)

The local trigger (LT) will contain the trigger interface for sampling the Fast Trigger and Validation, timing circuits to control ADC conversion and the channel's participation in readout. LT start comes from the Alignment LCA as described above. The LT can be reset whilst active by any one of these 4 conditions:

- the system's "event reject" signal
- the failure of a Fast Trigger or Validation sample point,
- the successful completion of readout
- a watchdog timeout.

Adjustment:

- Enable and disable for the shield (individual inputs cannot be disabled except by threshold)
- Fast Trigger sample point 0-2µs in 8ns steps (DAC range 0 to +3V)
- Validation sample point 0-10µs in 40ns steps (DAC range 0 to +3V)
- Watchdog timeout 0-100µs in 400ns steps (DAC range 0 to +3V)

3.8 Inspection Lines:

Logic and analogue inspection lines will be connected to all important internal signals and may be switched to the VXI bus inspection lines under software control.

Note on software: the hardware will be designed such that a write to the parameter (signal) selection register is applied to all channels, and the channel to be enabled is selected via the channel selection register. The 2 registers may be written in either order to achieve the same result after the 2nd write.

3.8.1 Logic Inspection Lines:

Each of the 4 channels has 64 signals (in 3 groups) for use on either (or both) of the two LI lines. The LI line parameter register selects 1 of 64 signals and the channel is chosen by the LI channel registers. LI lines will be disconnected by selecting channel 0 (parameter 0 does not disconnect the LI lines). Channels 1-4 select electronics for one of the 4 shields, and channel 5 selects the common LI signals.

Group A (General x32)	ADC Output Enable	Group B (Align LCA, x16)
BGO discriminators (x4)	Read TAC1-5 (x5)	Ge CFD 1 (in)
CsI discriminators (x4)	Read Pattern	Ge CFD 2 (in)
PD Gate BGO		Ge CFD 3 (in)
PD Hold/Reset BGO		Ge CFD 4 (in)
PD Gate CsI		Ge CFD 1 Aligned (out)
PD Hold/Reset CsI		Ge CFD 2 Aligned (out)
Veto (x4)		Ge CFD 3 Aligned (out)
Local Trigger (LT) Start		Ge CFD 4 Aligned (out)
LT FT sample		BGO 1 Aligned (out)
LT Val sample		BGO 2 Aligned (out)
LT Reset out		BGO 3 Aligned (out)
LT Valack		BGO 4 Aligned (out)
LT Watchdog		CsI 1 Aligned (out)
ADC busy		CsI 2 Aligned (out)
ADC Clock		CsI 3 Aligned (out)
ADC Fail		CsI 4 Aligned (out)

Group C (TDC LCA, x16)
TAC1 start
TAC2 start
TAC3 start
TAC4 start
TAC5 start
TAC1 stop
TAC2 stop
TAC3 stop
TAC4 stop
TAC5 stop
Any BGO
Any CsI
Any Ge
Start Pattern
Pattern Gate
TAC reset in

Common LI lines x10 (channel 5)
Fast Trigger
Validation
Inhibit Action
LT Reset in
Internal readout strobe
Internal readout acknowledge
Internal readout ren-in
Internal readout ren-out
ADC Sliding scale=0
ADC Sliding scale=full scale
There is room for 6 more signals

3.8.2 Analogue Inspection lines

Each of the 4 channels has 16 signals (only 13 defined: 3 are spare) for use on either (or both) of the two AI lines. The AI line parameter register selects 1 of 16 signals and the channel is chosen by the AI channel registers. AI lines will be disconnected by selecting channel 0 (parameter 0 does not disconnect the AI lines). Channels 1-4 select electronics for one of the 4 shields.

Analogue Inspection x13 signals per channel
BGO input (buffered) x4
CsI input (buffered) x4
BGO Peak
CsI Peak
Sum of BGO+CsI peak
BGO PZ test point
CsI PZ test point
There is room for 3 more signals

3.8.3 Voltage inspection Lines

There will be no voltage inspection lines in the analogue part of the ESS card although some supplies may be inspected via the GIRV5.

Voltage monitor chips will drive front panel LEDs to indicate that power supplies are operating within permitted tolerances.

3.9 VXI Interface and Fast Readout

The ESS card will connect to the VXI bus via a GIRv5. The GIRV5 handles all bus cycles both for control and for readout. All configuration and address decoding is handled by the GIRV5 which loads serial DACs and generates register outputs for controlling each channel to carry out the adjustments described in this document. The GIRV5 modules will be designed and built at CSNSM Orsay.

The GIRV5 readout will conform to the standard Eurogam/Euroball common dead time readout system and will be compatible with the STR8080 readout engines used in EXOGAM.

4.0 Inputs and Outputs

4.1 Front Panel Signals

4.1.1 Inputs:

- Each channel of shield electronics will have 8 inputs from the phototubes.

Connector type: 3M SCI coaxial with RG174 cable.
Signal Type: Analogue (50 ohm)

TOP

GND (16)	CsI_D (15)
GND (14)	CsI_C (13)
GND (12)	CsI_B (11)
GND (10)	CsI_A (9)
GND (8)	BGO_D (7)
GND (6)	BGO_C (5)
GND (4)	BGO_B (3)
GND (2)	BGO_A (1)

Pinout looking at ESS front panel

- Each channel of shield electronics will have 4 inputs from the Ge CFDs.

Connector type: IDC header (twisted pair ribbon cable)
Signal Type: ECL (twisted pair ribbon cable)

TOP

Veto_D- (16)	Veto_D+ (15)
Veto_C- (14)	Veto_C+ (13)
Veto_B- (12)	Veto_B+ (11)
Veto_D- (10)	Veto_A +(9)
CFD_D-(8)	CFD_D+ (7)
CFD_C- (6)	CFD_C+ (5)
CFD_B- (4)	CFD_B+ (3)
CFD_A- (2)	CFD_A+ (1)

Pinout looking at ESS front panel

4.1.2 Outputs:

- Each channel of shield electronics will generate 4 Vetos .

Connector type: IDC header (twisted pair ribbon cable)
Signal Type: ECL (twisted pair ribbon cable)

- Each card will generate a sumbus output indicating the number of active shields.

Pulse width determined by the width of the Veto pulse.
Connector type: Lemo 00 (2, for daisy chain in/out)
Signal Type: Analogue, 4mA per active shield.

4.1.3 LEDs

"Comfort" LEDS will be provided to indicate that discriminators are active.

4.2 Back panel:

The back of the card will connect to the VXI bus P1, P2 and P3 using the GIRV5 board which will handle all VME bus cycles for set-up and readout. There will be no other back panel connections.

5.0 Timescale and responsibility

Revised timescales following the decision of the September 1999 steering committee to change from 6 to 4 channels per card and to add the requirement to time align all inputs:

- Sub-modules designed and prototypes built whilst awaiting decision.
- Prototype VXI card ready Q3 2000
- Production cards built during Q4 2000, ready Q1 2001

The ESS card is the responsibility of the UK. Work on the ESS card is being carried out at Daresbury Laboratory and at the University of Liverpool using GIRV5 cards supplied by CSNSM Orsay.