The EXOGAM Escape Suppression Shield (ESS) Card
Register Map and GIR interface definition

1. VXI Configuration registers

Normal VXI configuration registers are included in A16 address space:

Offset from VXI slot base address	Register
0	ID/Logical Address
2	Device Type, model code
4	Status/Control register
6	Offset Register (base address for channel/common registers)
8	Serial number

2. Main Address Map:

All addresses are relative to the base address contained in the configuration offset register and all respond to 16 bit access cycles. This table shows groups of registers which are described in more detail in the rest of this document.

Register Group	Address Range
Common Register Area	0x0000 to 0x009e
GIR Readout control and status register area	0x00A0 to 0x00FE
Readout Setup Area	0x0100 to 0x0ffe
Channel 1	0x1000 to 0x10fe
Channel 2	0x1100 to 0x11fe
Channel 3	0x1200 to 0x12fe
Channel 4	0x1300 to 0x13fe

2.1 Common Registers

Address	Bus Width	Read/Write	Function
0x00	16 bit	R/W	Module Control Register (MCR)
0x02-0x1F			*Not yet allocated*
0x20	16 bit	R/W	Logic Inspection Line 1 Channel Select
0x22	16 bit	R/W	Logic Inspection Line 1 Parameter Select
0x24	16 bit	R/W	Logic Inspection Line 2 Channel Select
0x26	16 bit	R/W	Logic Inspection Line 2 Parameter Select
0x28	16 bit	R/W	Analogue Inspection Line 1 Channel Select
0x2a	16 bit	R/W	Analogue Inspection Line 1 Parameter Select
0x2c	16 bit	R/W	Analogue Inspection Line 2 Channel Select
0x2e	16 bit	R/W	Analogue Inspection Line 2 Parameter Select
0x40-0x5e	16 bit	R only	Read default DAC Buffer settings from XCProm
0x60-0x7e	16 bit	W only	Write new default DAC Buffer settings to XCProm
0x80-0x9e	16 bit	W only	Overwrite default DAC Buffer settings (volatile)
0xa0-0xfe	16 bit	R/W	For use inside GIR (readout control etc.)

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2.1.1 Module Control Register

The MCR register is implemented in the GIR's LCA and so needs one AP connector pin per bit.

Data Bit	Meaning when 0	Meaning when 1
0	*Not yet defined*	*Not yet defined*
1	*Not yet defined*	*Not yet defined*
2	*Not yet defined*	*Not yet defined*
3	*Not yet defined*	*Not yet defined*
4-15	*Not yet defined*	*Not yet defined*

2.1.2 Logic Inspection Line Registers.

Each logic inspection line has a pair of registers which select the channel and the parameter within the channel which is to be displayed on that inspection line.

2.1.2.1 The channel registers (0x20, 0x24) select one of 6 channels as follows:

Channel (data 0-15)	Meaning
0x0000	Disconnect the inspection line
0x0001	Connect Inspection line to channel 1
0x0002	Connect Inspection line to channel 2
0x0003	Connect Inspection line to channel 3
0x0004	Connect Inspection line to channel 4
0x0005	Connect Inspection line to common signals (used on all channels)
0x0006 - 0x001f	Not used (disconnect inspection line)
0x0020	GIR signals
0x0021-0xffff	Not used (disconnect inspection line)

The parameters to be displayed are defined by the parameter selection register. Channels 1-4 have the same selection of lines available, and the common signals have a different group of parameters. So the meaning of the inspection line parameter register depends on the value written to the channel register.

The hardware will be designed such that a write to the parameter (signal) selection register is applied to all channels, and the channel to be enabled is selected via the channel selection register. The 2 registers may be written in either order to achieve the same result after the 2nd write.

The GIR must supply the following signals to control the logic inspection lines:

- *EnableLI1_Channel_n (n=1,2,3,4,5)*
- *EnableLI2_Channel_n (n=1,2,3,4,5)*
- *DigStrobe1 (common to all multiplexers on LI1)*
- *DigStrobe2 (common to all multiplexers on LI2)*
- *Data lines D0-D6 Data clocked in to LI mux local register every time DigStrobe goes from 0 to 1*

2.1.2.2 Logic Inspection Parameter register signals (0x22, 0x26) when connected to channels 1-4

Data value	Parameter selected in channels 1-4
0x0000	BGO discriminator 1
0x0001	BGO discriminator 2
0x0002	BGO discriminator 3
0x0003	BGO discriminator 4
0x0004	CsI discriminator 1
0x0005	CsI discriminator 2
0x0006	CsI discriminator 3
0x0007	CsI discriminator 4
0x0008	PD Gate BGO
0x0009	PD Hold/Reset BGO
0x000A	PD Gate CsI
0x000B	PD Hold/Reset CsI
0x000C	Veto1
0x000D	Veto2
0x000E	Veto3
0x000F	Veto4
0x0010	Local Trigger (LT) Start
0x0011	LT FT sample
0x0012	LT Val sample
0x0013	LT Reset out
0x0014	LT Valack
0x0015	LT Watchdog
0x0016	ADC busy
0x0017	ADC Clock
0x0018	ADC Fail
0x0019	ADC Output Enable
0x001A	Read TDC1
0x001B	Read TDC2
0x001C	Read TDC3
0x001D	Read TDC4
0x001E	Read TDC5
0x001F	Read Pattern
0x0020	Ge CFD 1 (in)
0x0021	Ge CFD 2 (in)
0x0022	Ge CFD 3 (in)
0x0023	Ge CFD 4 (in)
0x0024	Ge CFD 1 Aligned (out)
0x0025	Ge CFD 2 Aligned (out)
0x0026	Ge CFD 3 Aligned (out)
0x0027	Ge CFD 4 Aligned (out)
0x0028	BGO 1 Aligned (out)
0x0029	BGO 2 Aligned (out)
0x002A	BGO 3 Aligned (out)
0x002B	BGO 4 Aligned (out)
0x002C	CsI 1 Aligned (out)
0x002D	CsI 2 Aligned (out)
0x002E	CsI 3 Aligned (out)
0x002F	CsI 4 Aligned (out)
0x0030	TAC1 start
0x0031	TAC2 start
0x0032	TAC3 start
0x0033	TAC4 start
0x0034	TAC5 start
0x0035	TAC1 stop
0x0036	TAC2 stop
0x0037	TAC3 stop
0x0038	TAC4 stop
0x0039	TAC5 stop
0x003A	Any BGO
0x003B	Any CsI
0x003C	Any Ge
0x003D	Start Pattern
0x003E	Pattern Gate

0x003F	TDC reset in

2.1.2.3 Logic Inspection Parameter register signals (0x22, 0x26) for common signals (ch 5)

Data value	Parameter selected in channel 5 (common)
0x0000	Fast Trigger
0x0001	Validation
0x0002	Inhibit Action
0x0003	LT Reset in
0x0004	Internal readout strobe
0x0005	Internal readout acknowledge
0x0006	Internal readout ren-in
0x0007	Internal readout ren-out
0x0008	ADC Sliding scale=0
0x0009	ADC Sliding scale=full scale
0x000A	*Not yet allocated*
0x000B	*Not yet allocated*
0x000C	*Not yet allocated*
0x000D	*Not yet allocated*
0x000E	*Not yet allocated*
0x000F	*Not yet allocated*
0x0010	Readout LCA signal (to be defined)
0x0011	Readout LCA signal (to be defined)
0x0012	Readout LCA signal (to be defined)
0x0013	Readout LCA signal (to be defined)
0x0014	Readout LCA signal (to be defined)
0x0015	Readout LCA signal (to be defined)
0x0016	Readout LCA signal (to be defined)
0x0017	Readout LCA signal (to be defined)
0x0018	Readout LCA signal (to be defined)
0x0019	Readout LCA signal (to be defined)
0x001A	Readout LCA signal (to be defined)
0x001B	Readout LCA signal (to be defined)
0x001C	Readout LCA signal (to be defined)
0x001D	Readout LCA signal (to be defined)
0x001E	Readout LCA signal (to be defined)
0x001F	Readout LCA signal (to be defined)

2.1.2.3 Logic Inspection Parameter register signals (0x22, 0x26) for GIR signals (ch 0x20)

Data value	Parameter selected in channel 0x20 (GIR)
0x0000-0xFFFF	To be added later

2.1.3 Analogue Inspection Line Registers.

Each Analogue inspection line has a pair of registers which select the channel and the parameter within the channel which is to be displayed on that inspection line.

2.1.3.1 The channel registers (0x28, 0x2C) select one of 5 channels as follows:

Channel (data 0-15)	Meaning
0x0000	Disconnect the inspection line
0x0001	Connect Inspection line to channel 1
0x0002	Connect Inspection line to channel 2
0x0003	Connect Inspection line to channel 3
0x0004	Connect Inspection line to channel 4
0x0005 - 0xffff	Not used (disconnect inspection line)

The hardware will be designed such that a write to the parameter (signal) selection register is applied to all channels, and the channel to be enabled is selected via the channel selection register. The 2 registers may be written in either order to achieve the same result after the 2nd write.

The GIR must supply the following signals to control the analogue inspection lines:

- *AI1_Channel_Enable_n (n=1,2,3,4)*
- *AI2_Channel_Enable_n (n=1,2,3,4)*
- *AIWritestrobe1 (common to all multiplexers on AI1)*
- *AIWritestrobe2 (common to all multiplexers on AI2)*
- *Data lines D0-D3*

2.1.3.2 Analogue Inspection Parameter register signals (0x2A, 0x2E)

Data value	Parameter selected
0x0000	BGO input 1 (buffered)
0x0001	BGO input 2 (buffered)
0x0002	BGO input 3 (buffered)
0x0003	BGO input 4 (buffered)
0x0004	CsI input 1 (buffered)
0x0005	CsI input 2 (buffered)
0x0006	CsI input 3 (buffered)
0x0007	CsI input 4 (buffered)
0x0008	BGO Peak
0x0009	CsI Peak
0x000A	Sum of BGO+CsI peak
0x000B	BGO PZ test point
0x000C	CsI PZ test point
0x000D	*Not yet allocated*
0x000E	*Not yet allocated*
0x000F	*Not yet allocated*

2.1.4 Voltage Inspection Line

There will be no voltage inspection lines in the analogue part of the ESS card although some supplies may be inspected via the GIRV5.

2.1.5 GIR Readout and status registers (0x00A0 to 0x00FE)

Details of registers within GIR to be added later.

2.2 Readout Setup Registers

Address	Bus Width	Read/Write	Function
0x100	16 bit	R/W	Readout Enable Register
0x102-10e			*Not allocated*
0x110	16 bit	R/W	Define Channel 1 TDC1 item/group
0x112	16 bit	R/W	Define Channel 1 TDC2 item/group
0x114	16 bit	R/W	Define Channel 1 TDC3 item/group
0x116	16 bit	R/W	Define Channel 1 TDC4 item/group
0x118	16 bit	R/W	Define Channel 1 TDC5 item/group
0x11a	16 bit	R/W	Define Channel 1 Pattern item/group
0x11c	16 bit	R/W	Define Channel 1 Energy item/group
0x11e			*Not allocated*
0x120	16 bit	R/W	Define Channel 2 TDC1 item/group
0x122	16 bit	R/W	Define Channel 2 TDC2 item/group
0x124	16 bit	R/W	Define Channel 2 TDC3 item/group
0x126	16 bit	R/W	Define Channel 2 TDC4 item/group
0x128	16 bit	R/W	Define Channel 2 TDC5 item/group
0x12a	16 bit	R/W	Define Channel 2 Pattern item/group
0x12c	16 bit	R/W	Define Channel 2 Energy item/group
0x12e			*Not allocated*
0x130	16 bit	R/W	Define Channel 3 TDC1 item/group
0x132	16 bit	R/W	Define Channel 3 TDC2 item/group
0x134	16 bit	R/W	Define Channel 3 TDC3 item/group
0x136	16 bit	R/W	Define Channel 3 TDC4 item/group
0x138	16 bit	R/W	Define Channel 3 TDC5 item/group
0x13a	16 bit	R/W	Define Channel 3 Pattern item/group
0x13c	16 bit	R/W	Define Channel 3 Energy item/group
0x13e			*Not allocated*
0x140	16 bit	R/W	Define Channel 4 TDC1 item/group
0x142	16 bit	R/W	Define Channel 4 TDC2 item/group
0x144	16 bit	R/W	Define Channel 4 TDC3 item/group
0x146	16 bit	R/W	Define Channel 4 TDC4 item/group
0x148	16 bit	R/W	Define Channel 4 TDC5 item/group
0x14a	16 bit	R/W	Define Channel 4 Pattern item/group
0x14c	16 bit	R/W	Define Channel 4 Energy item/group
0x14e-0xffe			*Not allocated*

The GIR must supply the following signals to set up the readout registers:

- *RGI select (indicates a VME cycle with valid AM code for an address in the range 0x100 to 0xffe)*
- *Read/Write (VME r/w line)*
- *RegStrobe (Clocks VME write data into RGI registers)*
- *VME address lines A1-A11 (to select registers within RGI address space)*
- *VME data lines D0-D31*

2.2.1 The Readout Enable Register (0x100)

This register is implemented in the Readout LCA. It is accessed by the GIR's RGI select, r/w, RegStrobe, Address and Data lines pins as defined in section 2.2

Data Bit	Meaning when 0	Meaning when 1
0	Disable TDC1 readout	Enable TDC1 readout
1	Disable TDC2 readout	Enable TDC2 readout
2	Disable TDC3 readout	Enable TDC3 readout
3	Disable TDC4 readout	Enable TDC4 readout
4	Disable TDC5 readout	Enable TDC5 readout
5	Disable Pattern readout	Enable Pattern readout
6	Disable Energy readout	Enable Energy readout
7-15	*Not used*	*Not used*

2.2.2 Item and Group registers (0x110 to 0x14c)

These registers define the 14 bits used for item and group fields for each of the 7 readout parameters in the 4 channels (28 registers). Data lines d0-d13 are used and the top 2 data bits (d14, d15) are ignored.

The data may be read back over the lower 16 data lines (d0-13 used). During event by event fast block transfers the item and group number are placed onto d16-d29.

These registers are implemented in the Readout LCA. They are accessed by the GIR's RGI select, r/w, RegStrobe, Address and Data lines pins as defined in section 2.2

2.3 Channel Registers

Addresses are shown in the table for channel 1. For channel 2 address, replace 0x10nn with 0x11nn, for channel 3 use 0x12nn and for channel 4 use 0x13nn.

Address	Bus Cycle Width	Read/Write	Function
0x1000	16 bit	W only	DAC setting for BGO1 threshold
0x1002	16 bit	W only	DAC setting for BGO2 threshold
0x1004	16 bit	W only	DAC setting for BGO3 threshold
0x1006	16 bit	W only	DAC setting for BGO4 threshold
0x1008	16 bit	W only	DAC setting for CsI1 threshold
0x100A	16 bit	W only	DAC setting for CsI2 threshold
0x100C	16 bit	W only	DAC setting for CsI3 threshold
0x100E	16 bit	W only	DAC setting for CsI4 threshold
0x1010	16 bit	W only	Local Trigger Fast Trigger Sample
0x1012	16 bit	W only	Local Trigger Validation Sample
0x1014	16 bit	W only	Local Trigger Watchdog setup
0x1016	*16 bit*	*W only*	*Not yet allocated*
0x1018	16 bit	W only	Connect to BGO Peak detector
0x101A	16 bit	W only	Connect to CsI Peak detector
0x101C	*16 bit*	*W only*	*Not yet allocated*
0x101E	*16 bit*	*W only*	*Not yet allocated*
0x1020	16 bit	R/W	Channel Control Register
0x1022	16 bit	W only	BGO 1 alignment delay
0x1024	16 bit	W only	BGO 2 alignment delay
0x1026	16 bit	W only	BGO 3 alignment delay
0x1028	16 bit	W only	BGO 4 alignment delay
0x102A	16 bit	W only	CsI 1 alignment delay
0x102C	16 bit	W only	CsI 2 alignment delay
0x102E	16 bit	W only	CsI 3 alignment delay
0x1030	16 bit	W only	CsI 4 alignment delay
0x1032	16 bit	W only	Ge 1 alignment delay
0x1034	16 bit	W only	Ge 2 alignment delay
0x1036	16 bit	W only	Ge 3 alignment delay
0x1038	16 bit	W only	Ge 4 alignment delay
0x103A	16 bit	W only	TDC1 stop select
0x103C	16 bit	W only	TDC2 stop select
0x103E	16 bit	W only	TDC3 stop select
0x1040	16 bit	W only	TDC4 stop select
0x1042	16 bit	W only	TDC5 start and stop select
0x1044	16 bit	W only	Veto delay
0x1046	16 bit	W only	Veto width
0x1048	16 bit	W only	Pattern Width
0x104a-0x10FE			*Not yet allocated*

2.3.1 DAC Setting registers (0x1n00 to 0x1n14) (detail)

The signals required for the GIR to control the DACs are as follows:

- *DCSna (n=1,2,3,4) Chip select for Threshold DACs on channels 1,2,3 or 4*
- *DCSnb (n=1,2,3,4) Chip select for Local Trigger DACs on channels 1,2,3 or 4*
- *DCLKn (n=1,2,3,4) Clock for both DACs on channel 1,2,3 or 4*
- *DDINn (n=1,2,3,4) Serial data in for both DACs on channel 1,2,3 or 4*

(Total 16 signals for the 4 channels)

Address	Bus Cycle Width	Read/Write	Function
0x1000	16 bit	W only	DAC setting for BGO1 threshold
0x1002	16 bit	W only	DAC setting for BGO2 threshold
0x1004	16 bit	W only	DAC setting for BGO3 threshold
0x1006	16 bit	W only	DAC setting for BGO4 threshold
0x1008	16 bit	W only	DAC setting for CsI1 threshold
0x100A	16 bit	W only	DAC setting for CsI2 threshold
0x100C	16 bit	W only	DAC setting for CsI3 threshold
0x100E	16 bit	W only	DAC setting for CsI4 threshold
0x1010	16 bit	W only	Local Trigger Fast Trigger Sample
0x1012	16 bit	W only	Local Trigger Validation Sample
0x1014	16 bit	W only	Local Trigger Watchdog setup
0x1016	16 bit	W only	*Not yet allocated*
0x1018	16 bit	W only	Connect to BGO Peak detector
0x101A	16 bit	W only	Connect to CsI Peak detector
0x101B	16 bit	W only	*Not yet allocated*
0x101E	16 bit	W only	*Not yet allocated*

The 8 threshold discriminators will each be adjustable over the range 0 to 250keV in 1 keV steps. (not calibrated) (DAC range 0 to +1V)
The Local trigger signals' DAC range is 0 to +3V in 256 steps.

2.3.2 Channel Control Register, CCR (0x1n20)

The 4 CCR registers are implemented in the GIR's LCA and so need one AP connector pin per bit.

Data Bit	Meaning when 0	Meaning when 1
0	Disable channel	Enable channel
1	LT started by BGO or CsI	LT started by Ge or BGO or CsI
2	Sliding scale setup off	Sliding scale setup on
3	Sliding scale DAC =0	Sliding scale DAC =0xFF
4-15	*Not yet defined*	*Not yet defined*

2.3.3 Alignment Registers (0x1n22-0x1n38)

These registers are implemented in the Alignment LCA. They are each have their own write enable signal (connected to latch clock enable) and are clocked by a common strobe called RegStrobe. So the GIR must generate the write enable signals by decoding the address and r/w line, and the strobe from the write line and the DS*.

The bottom 6 bits of the data bus (d0-d5) are used to define the delay in steps of 10ns from 10ns (0) to 650ns (0x3f). Higher order data bits are ignored, so for example 0x380 will be interpreted as a delay of 10ns.

For the 12 alignment registers, the GIR must provide a total of 19 pins of which 7 are shared with other registers (RegStrobe and d0-d5), and 12 (the write enable signals) are unique to these registers.

2.3.4 TDC control registers (0x1n3A-0x1n42)

These registers are implemented in the Alignment LCA. *They are each have their own write enable signal (connected to latch clock enable) and are clocked by a common strobe called RegStrobe. So the GIR must generate the write enable signals by decoding the address and r/w line, and the strobe from the write line and the DS*.*

In the Veto/TDC Stop Select registers for quadrants 1-4 (0x1n3A-0x1n40) the bottom 3 bits of the data bus (d0-d2) are used to select which of the 8 possible stop signals is used. Higher order data bits are ignored, so for example 0x382 will be interpreted the same as 0x02.

The 4 Vetos are generated from the same signal which is selected to stop the corresponding TDC.

Data	**Stop signal**
0x0000	BGO (nearest quarter)
0x0001	BGO (whole shield)
0x0002	CsI (nearest quarter)
0x0003	CsI (whole shield)
0x0004	BGO OR CsI (nearest quarter)
0x0005	BGO OR CsI (whole shield)
0x0006	RF
0x0007	FT
0x0009-0xffff	Not used

In the TDC5 control register (0x1n42) the bottom 4 bits of the data bus (d0-d3) are used to select which of the 3 possible stop signals (d3,d2) and which of the 4 possible start signals (d1,d0) is used. Higher order data bits are ignored, so for example 0x382 will be interpreted the same as 0x02.

Data	**Stop Signal (d3,d2)**	**Start signal (d1,d0)**
0x0000	RF	BGO (whole shield)
0x0001	RF	CsI (whole shield)
0x0002	RF	BGO OR CsI (whole shield)
0x0003	RF	Ge (OR of all 4 Ge CFDs)
0x0004	FT	BGO (whole shield)
0x0005	FT	CsI (whole shield)
0x0006	FT	BGO OR CsI (whole shield)
0x0007	FT	Ge (OR of all 4 Ge CFDs)
0x0008	Ge (OR of all 4 Ge CFDs)	BGO (whole shield)
0x0009	Ge (OR of all 4 Ge CFDs)	CsI (whole shield)
0x000A	Ge (OR of all 4 Ge CFDs)	BGO OR CsI (whole shield)
0x000B	Ge (OR of all 4 Ge CFDs)	Ge (OR of all 4 Ge CFDs)
0x000C-0xFFFF	Not used	Not Used

For the 5 TDC control registers, the GIR must provide a total of 10 pins of which 5 are shared with other registers (RegStrobe and d0-d3), and 5 (the write enable signals) are unique to these registers.

2.3.5 Veto delay register (0x1n44)

This register is implemented in the TDC LCA. It has a write enable signal (connected to latch clock enable) and is clocked by a common strobe called RegStrobe. So the GIR must generate a write enable signal by decoding the address and r/w line, and the strobe from the write line and the DS*.

The bottom 4 data lines (d0-d3) are used to define the Veto delay in steps of 10ns from 10-170ns. The remaining 12 data lines are ignored.

For the Veto delay register, the GIR must provide a total of 6 pins of which 5 are shared with other registers (RegStrobe and d0-d3), and 1 (the write enable signal) is unique to this register.

2.3.6 Veto width register (0x1n46)

This register is implemented in the TDC LCA. It has a write enable signal (connected to latch clock enable) and is clocked by a common strobe called RegStrobe. So the GIR must generate a write enable signal by decoding the address and r/w line, and the strobe from the write line and the DS*.

The bottom 8 data lines (d0-d7) are used to define the Veto delay in steps of 10ns from 10-2570ns. The remaining 8 data lines are ignored.

For the Veto width register, the GIR must provide a total of 10 pins of which 9 are shared with other registers (RegStrobe and d0-d7), and 1 (the write enable signal) is unique to this register.

2.3.7 Pattern width register (0x1n48)

This register is implemented in the TDC LCA. It has a write enable signal (connected to latch clock enable) and is clocked by a common strobe called RegStrobe. So the GIR must generate a write enable signal by decoding the address and r/w line, and the strobe from the write line and the DS*.

The bottom 8 data lines (d0-d7) are used to define the local coincidence window for the pattern register in steps of 10ns from 10-2570ns. The remaining 8 data lines are ignored.

For the Pattern width register, the GIR must provide a total of 10 pins of which 9 are shared with other registers (RegStrobe and d0-d7), and 1 (the write enable signal) is unique to this register.

3.0 Summary of GIR signal connections

Assume that all signals are TTL active high unless specifically marked as active low by the use of a * symbol to indicate active low or a voltage (±xV) to indicate an analogue signal.

77 General signals used by more than 1 channel or register

Databus D0-D31
Address Bus A1-A11
VME R/W line
CLK16MHz
CLK25MHz
CLK100MHz
Temperature monitoring sensor 1
Temperature monitoring sensor 2
Over_Temp_1
Over_Temp_2
Under_Temp_1
Under_Temp_2
GIR Temp LED
GIR FIFO error LED
GIR LCA_programmed LED
Event_Number_From_Lbus_0
Event_Number_From_Lbus_1
Event_Number_From_Lbus_2
Event_Number_From_Lbus_3
Event_Number_To_GIR_RO_0
Event_Number_To_GIR_RO_1
Event_Number_To_GIR_RO_2
Event_Number_To_GIR_RO_3
Logic Inspection 1
Logic Inspection 2
Analogue Inspection 1 (±3V)
Analogue Inspection 2 (±3V)g
RDO_Data_Ready
RDO_Data_Ack
RDO_Ren_in
RDO_Lpass
Start_Readout
LT_Reset_in_from_GIR
Val_buf
Fast_Trigger
RF

80 signals needed for register enables and data bits from registers held in GIR LCAs

MCRbit0
MCRbit1
MCRbit2
MCRbit3
LI1_Channel_Enable1
LI1_Channel_Enable2
LI1_Channel_Enable3
LI1_Channel_Enable4
LI2_Channel_Enable1
LI2_Channel_Enable2
LI2_Channel_Enable3
LI2_Channel_Enable4
DigStrobe1
DigStrobe2
AI1_Channel_Enable1
AI1_Channel_Enable2

AI1_Channel_Enable3
AI1_Channel_Enable4
AI2_Channel_Enable1
AI2_Channel_Enable2
AI2_Channel_Enable3
AI2_Channel_Enable4
AI_WriteStrobe1
AI_WriteStrobe2
RGI_select
RegStrobe
DACCS1A
DACCS2A
DACCS3A
DACCS4A
DACCS1B
DACCS2B
DACCS3B
DACCS4B
DCLK1
DCLK2
DCLK3
DCLK4
DDin1
DDin2
DDin3
DDin4
CCR1_bit0
CCR1_bit1
CCR1_bit2
CCR1_bit3
CCR2_bit0
CCR2_bit1
CCR2_bit2
CCR2_bit3
CCR3_bit0
CCR3_bit1
CCR3_bit2
CCR3_bit3
CCR4_bit0
CCR4_bit1
CCR4_bit2
CCR4_bit3
BGO1_Align_Delay_WrEn
BGO2_Align_Delay_WrEn
BGO3_Align_Delay_WrEn
BGO4_Align_Delay_WrEn
CsI1_Align_Delay_WrEn
CsI2_Align_Delay_WrEn
CsI3_Align_Delay_WrEn
CsI4_Align_Delay_WrEn
Ge1_Align_Delay_WrEn
Ge2_Align_Delay_WrEn
Ge3_Align_Delay_WrEn
Ge4_Align_Delay_WrEn
TDC1_Stop_Select
TDC2_Stop_Select
TDC3_Stop_Select
TDC4_Stop_Select
TDC5_Start_Stop_Select
Veto_Delay_WrEn
Veto_Width_WrEn
Pattern_Width_WrEn