EDOC237 EUROGAM Clover Card User Guide

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Introduction

The EUROGAM/EUROBALL Clover card fully instruments a EUROGAM Clover Ge detector and its associated BGO suppression shield. The inputs come from the Ge and BGO pre-amps and, after analogue signal processing, the output from the card is a series of energy and timing data words plus a hit pattern.

The analogue signal processing is the same as used in the EUROGAM phase 1 Ge and BGO cards (full details are given later) except that there is no ballistic deficit correction in the Ge channels. This is not necessary since the crystals in the Ge detectors are smaller than those used in EUROGAM phase 1 and so ballistic deficit does not have such a significant effect on their resolution.

For each Ge channel there is a high and a low gain (4MeV and 20MeV) energy measurement and 2 timing measurements (the peaking time and the difference in time between this channel and a global timing reference derived from the trigger system). The BGO channel provides a single energy measurement (typically 8MeV range) and a single timing measurement (the difference in time between this channel and a global timing reference derived from the trigger system). There is also a hit pattern to show which Ge detectors and which BGO elements are involved in the event.

There are 4 Ge electronics channels plus an additional spare channel which can be cabled in and then reconfigured from software to take the place of any of the other 4 channels should a problem arise during an experiment. The BGO channel accepts signals from the 16 element shield in 8 pairs, each pair of phototubes driving its own pre-amplifier.

Acknowledgements:

The Clover card is a collaborative project and the following people have been involved:

Engineer responsible for overall design:	*Ian Lazarus (Daresbury Lab)*
VXI interface and Readout design:	*Patrick Coleman-Smith (Daresbury Lab)*
CAD work including PCB design:	*Jim Thornhill (Liverpool University)*
Assembly work:	*Manchester University, Dept of Physics Electronics Workshop.*
Ge/BGO signal processing components:	*Alphonse Richard, Zdravko Zojceski, M. Engrand (IPN Orsay)*
	Germain Bosson (ISN Grenoble)
	Nabil Karkour (CSNSM Orsay)
	Michel Goyot (IPN Lyon)
	Charles Ring (CRN Strasbourg)
MIDAS and other software:	*Vic Pucknell, Simon Letts, Peter Owens (Daresbury Laboratory)*

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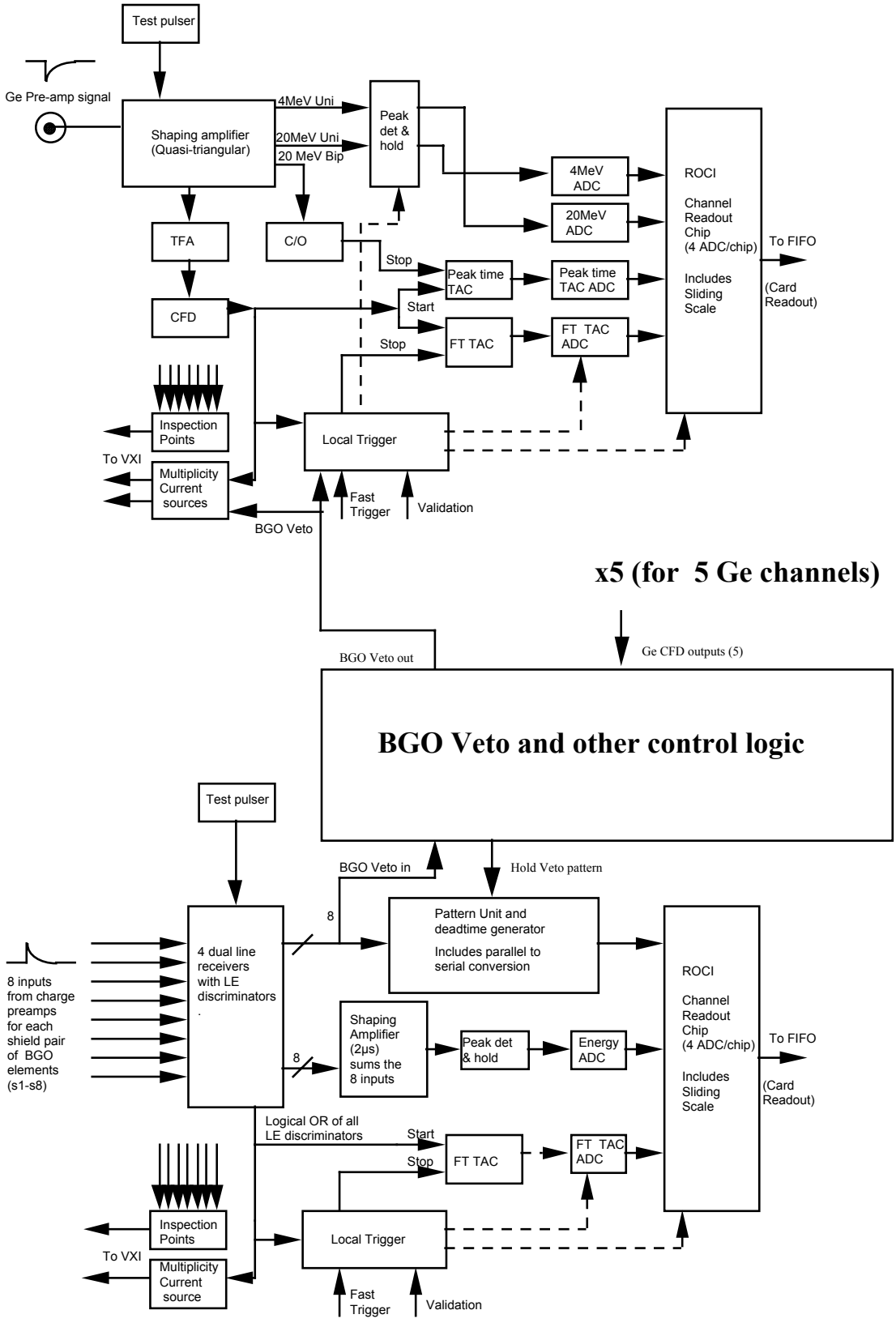

Fig 1 Block diagram of Eurogam Phase 2 Detector Card

Ge Signal Processing

Input:

200mV/MeV (±10%) pre-amp signal with 50Ω pre-amp output impedance.
50μs fall time constant (+/- 5%)
1K input impedance (approx.)

Signal Shaping:

Unipolar output from 6th order quasi-triangular filter.
Peaking time of 4.4μs and FWHM 5 μs.
Pulse width at 0.1% is 11μs.
Output amplifier stage generates 4MeV and 20MeV ranges.
Bipolar (differentiated) outputs available for crossover timing.

Timing:

CFD: min threshold 20keV, pulse pair resolution better than 1μs
timing walk 3ns for 200:1 dynamic range, 25ns for 1000:1 (200ns Tr)
(Figures from phase 1 Ge with 50ns delay; need to re-measure using new 27ns CFD)
TFA with 50ns integration and 180ns differentiation. Gain x3 or x10.
TAC 0-2μs, FWHM 0.6ns, INL <5%

Outputs for coding:

4 MeV Unipolar signal
20 MeV Unipolar signal
TAC measuring peaking time (CFD firing to bipolar crossover)
TAC measuring channel firing time before reference pulse (CFD to FT)

ADC:

13 bits resolution (8192 channels)
Sliding scale
Conversion time 4.5μs
DNL <1%
INL < 250ppm

BGO Signal Processing:

Input:

1000mV/MeV pre-amp signal with approx. 5Ω pre-amp output impedance.
(Phototube voltage must be adjusted to give 1000mV/MeV level.)
30ns rise time constant (+/- 10%)
10μs fall time constant (+/- 1.5%)
50Ω input impedance

Signal Shaping:

Bipolar output from 4th order semi-gaussian filter. (CR^2 RC^4, RC=2μs)
Peaking time of 5.2μs and FWHM 5.5 μs.
Pulse width at 0.1% is 12 x τ = 24μs.
Output 8 MeV full scale
Amplifier resolution is 3keV fwhm.

Outputs for coding:

8 MeV Energy signal
TAC measuring channel firing time before reference pulse (disc. to FT)
Also a serial bit stream indicating the hit pattern from BGO and Ge.

ADC:

13 bits resolution (8192 channels)
Sliding scale
Conversion time 4.5μs
DNL <1%
INL < 250ppm

Clover Detector Card Interconnections

* Primary interconnection mechanism is the VXI backplane as for phase 1.
* The inputs from the Ge pre-amps are connected to the front panel by BNC sockets.
* The BGO input is a 20 way IDC using similar LEMO-IDC cards to phase 1 but smaller to prevent mis-connection of phase 1 shields to phase 2 electronics and vice versa.
* LEDs are provided to indicate that BGO discriminators and Ge CFDs are firing as used in phase 1. A further LED is used to record FIFO errors (indicating readout problems).
* Front panel rate monitoring is provided via a 34 way IDC connector. 13 differential ECL signal pairs are available from 5 CFDs and 8 BGO line receivers.
* Backplane sumbuses and all other VXI connections are retained for full compatibility with phase 1. When the clover card is adjacent to phase 1 cards, the BGO local bus veto signals will be ignored and the Ge local bus Veto inputs will not be driven.
* There are no external Veto inputs or outputs or external amplifier inputs.

Pinouts for connectors are given in fig 2 on the next page.

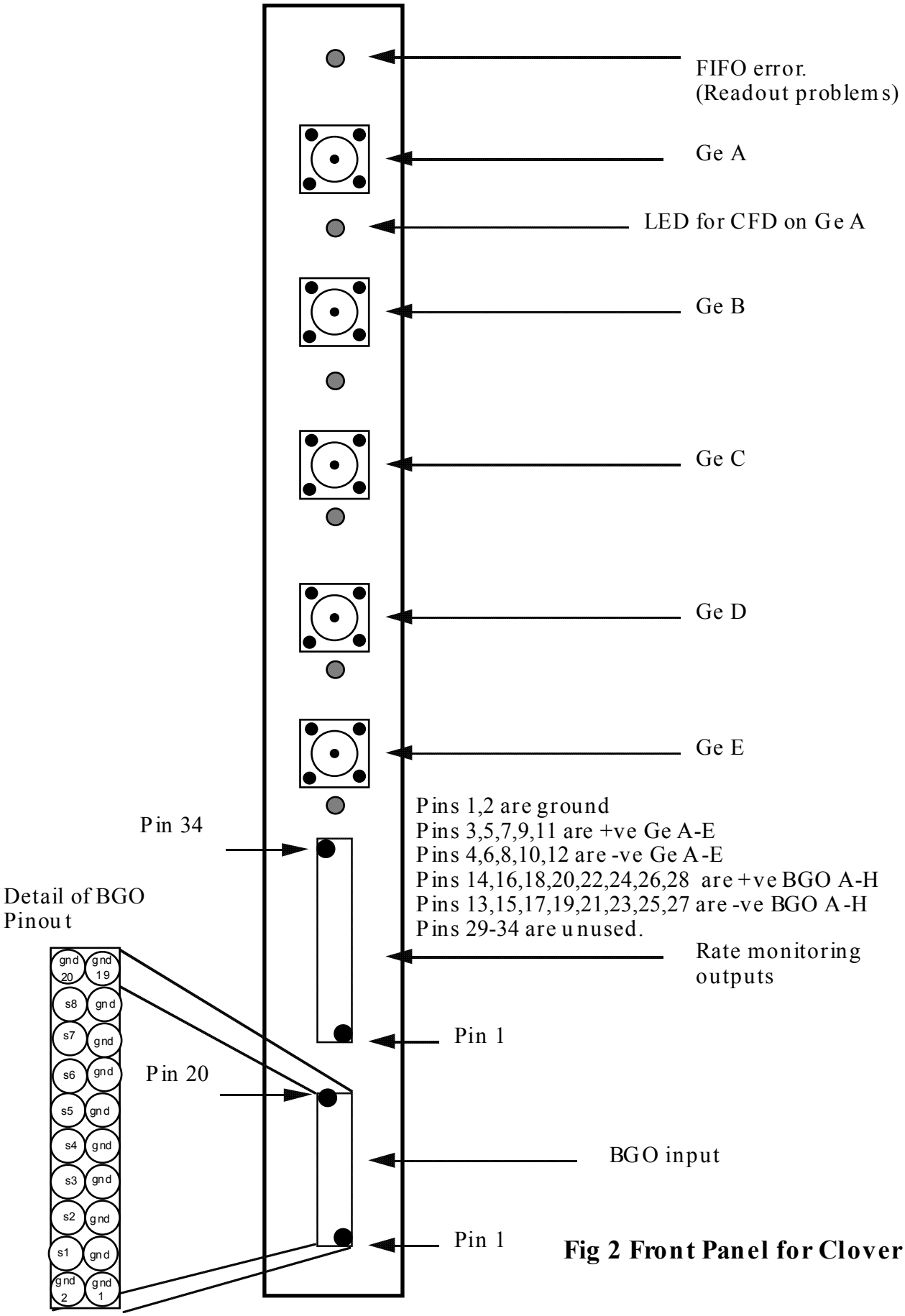

Fig 2 Front Panel for Clover Card

Operating Modes for the Clover Detector

The anti-Compton veto system and sumbuses become more complex with a Clover detector than a conventional tapered detector in deciding what combination of detector hits comprises a clean hit, whether only 1 Ge may be hit (i.e. the Ge's veto each other) or whether a combination of Ge hits is allowed and which parts of the BGO shield veto which Ge detectors. All possible combinations of Ge/BGO hit pattern are programmable in an 8kx4 memory using the 13 bit hit pattern as an address, with the 4 data bits determining which, if any, of the sumbuses (Raw Ge, Clean Ge, BGO) are to be turned on and whether or not to reject the event in hardware (or to mark it, depending on whether the card is in mark or reject mode). Three of the most useful modes of operation are available from the MIDAS software in the top level of the Clover card control menu. These modes are as follows:

Typical Modes of operation (these are all available from MIDAS software):

1) Simple.
In this case, all 5 Ge inputs (4 'real' inputs + 1 spare) are treated as a single detector with a single BGO shield. When 1 or more Ge element fires, a multiplicity of 1 is indicated on the Raw Ge sumbus regardless of what happens in the BGO. The Clean Ge sumbus indicates a multiplicity of 1 if no element in the BGO shield has fired. If 1 or more BGO element does fire, then a multiplicity of 1 is indicated on the BGO sumbus and the Clean Ge sumbus current driver is inhibited.

2) Exactly One Ge.
In this case exactly 1 of the 4 Ge inputs must fire, with the other 3 Ge inputs being used, along with the whole BGO shield, as anti-Compton vetos. The Raw Ge sumbus sees a multiplicity of 1 when 1 or more Ge elements fires (even though the 2nd Ge is part of the veto), but the Clean Ge sumbus indicates a multiplicity of 1 only if exactly 1 Ge has fired and no BGO element has fired. If 1 or more BGO element fires, then a multiplicity of 1 is indicated on the BGO sumbus and the Clean Ge sumbus current driver is inhibited.

3) Ignore Opposite Corner.
This mode is similar to the "Exactly One Ge" mode except that intelligence is applied to the processing of the BGO shield. The 4 BGO elements in the opposite corner are ignored, for example:

Ge A is "clean" if there are no hits in any of the BGO pairs s1,s2,s3,s4,s7,s8 or Ge B-D.
(i.e. BGO elements i,j,k and l in s5 and s6 are ignored.)

The Raw Ge sumbus sees a multiplicity of 1 when 1 or more Ge elements fires, but the Clean Ge sumbus indicates a multiplicity of 1 only if exactly 1 Ge has fired and there have been no BGO hits in the 12 relevant elements in the shield. If one or more BGO element (from the whole 16 element shield) fires, then a multiplicity of 1 is indicated on the BGO sumbus.

Mode	**Raw Ge Σ= 1**	**Clean Ge Σ= 1**	**BGO Σ= 1**	**Anti-Compton**
Simple	≥ 1 Ge	≥ 1 Ge & not AC	≥ 1 BGO	16 BGO + 0 Ge
Exactly 1 Ge	≥ 1 Ge	= 1 Ge & not AC	≥ 1 BGO	16 BGO + 3 Ge
Ignore Opp Corner	≥ 1 Ge	= 1 Ge & not AC	≥ 1 BGO	12 BGO + 3 Ge

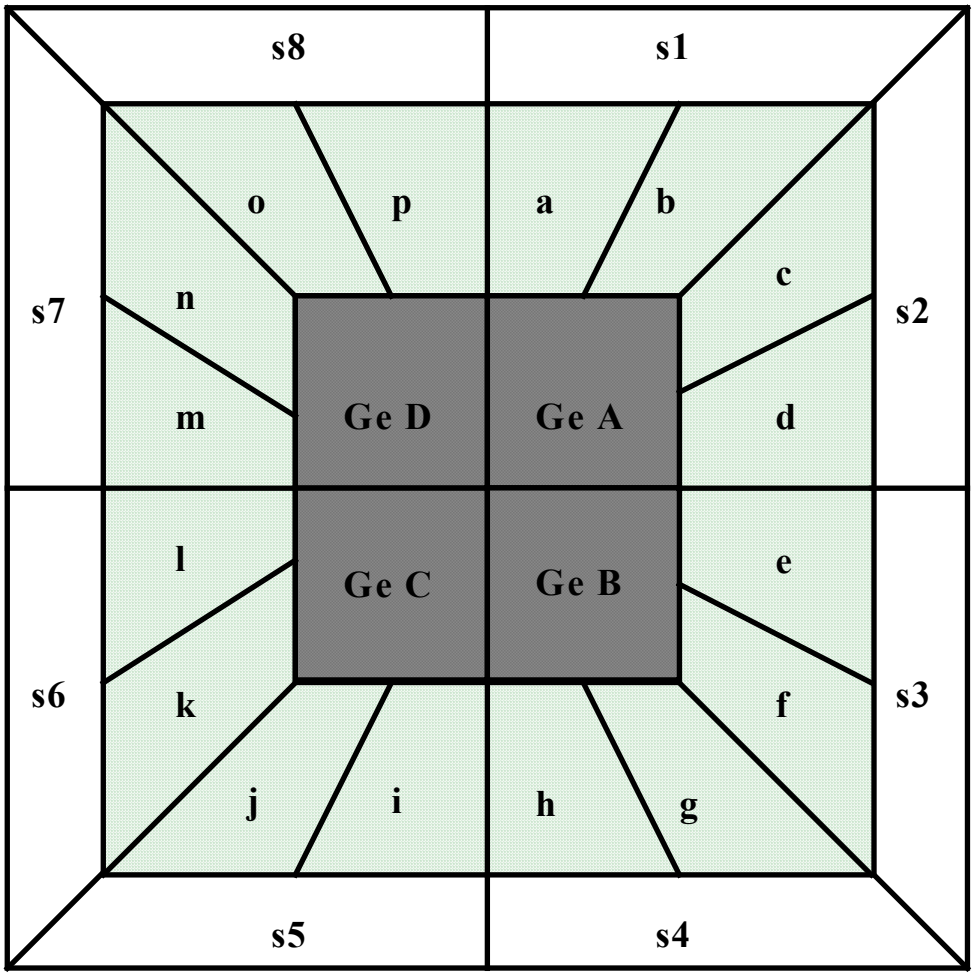

Fig 3
Naming scheme for Clover Ge and BGO elements showing the mapping from 16 BGO elements to 8 BGO signals for the phase 2 electronics.

Drawn: I.L. Nov 1992

MIDAS Software Interface For Clover Card.

The following pages show typical screens from MIDAS software, used in Euroball to control the Clover Card.

Fig 4 shows the Base Frame, and indicates that you should select the Card Setup menu, where you will find an entry for the Clover Card. The result of selecting this is shown in the same diagram. The enable buttons toggle the on/off function for each channel (also available from within the Ge and BGO sub-menus). This is the point at which the Suppression mode is selected (see page 6) and, in the event of a malfunction in one of the Ge channels, the spare channel configured . The Clover Card's "Engineering" menu and "Readout" button are for use by engineers only and contain no user controllable functions.

The more detailed Ge and BGO menus accessed from the Clover Card Setup menu (or directly from the Base Frame's VXI Module Setup menu) are shown in fig 5 and fig 6 respectively. These 2 menus are very much the same as used for the phase 1 Ge and BGO cards. Note that for each Ge channel the PZ adjustment must be made for the specific detector/pre-amp attached, and should be checked before an experiment. Similarly, the FT sample and Val sample points (trigger timing) should be checked before each experiment. The sample points should be placed in the middle of the FT and Validation pulses respectively. The Ge channels have a common FT sample control, but the BGO channel has its own independent control to cope with the different characteristics of the two types of detector.

The user controls which of the parameters are read out using the RO ticks at the top of each screen (fig 5 and fig 6). The sliding scale (SS) item should always be ticked except for the pattern for which the SS must never be enabled. The pattern includes not only the BGO, but also the Ge hit pattern.

To help in setting up and checking the cards, some typical shapes of the signals on the inspection lines are shown in fig 7 to 10.

From the base frame select the VXI module Setup menu and the Clover Card item

Fig 4 MIDAS Base Frame and Clover card menu selection.

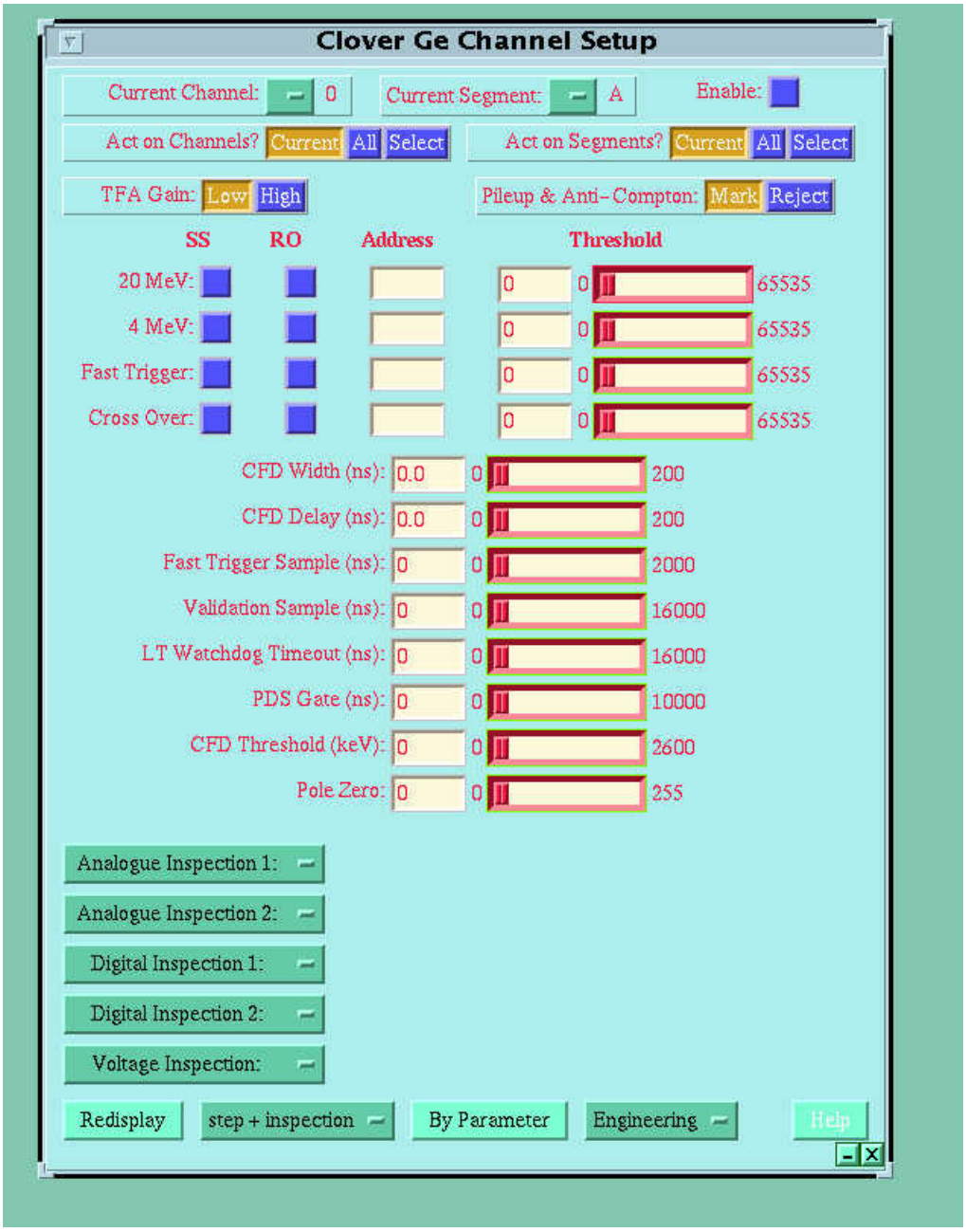

Fig 5 Clover Card Ge channel control window

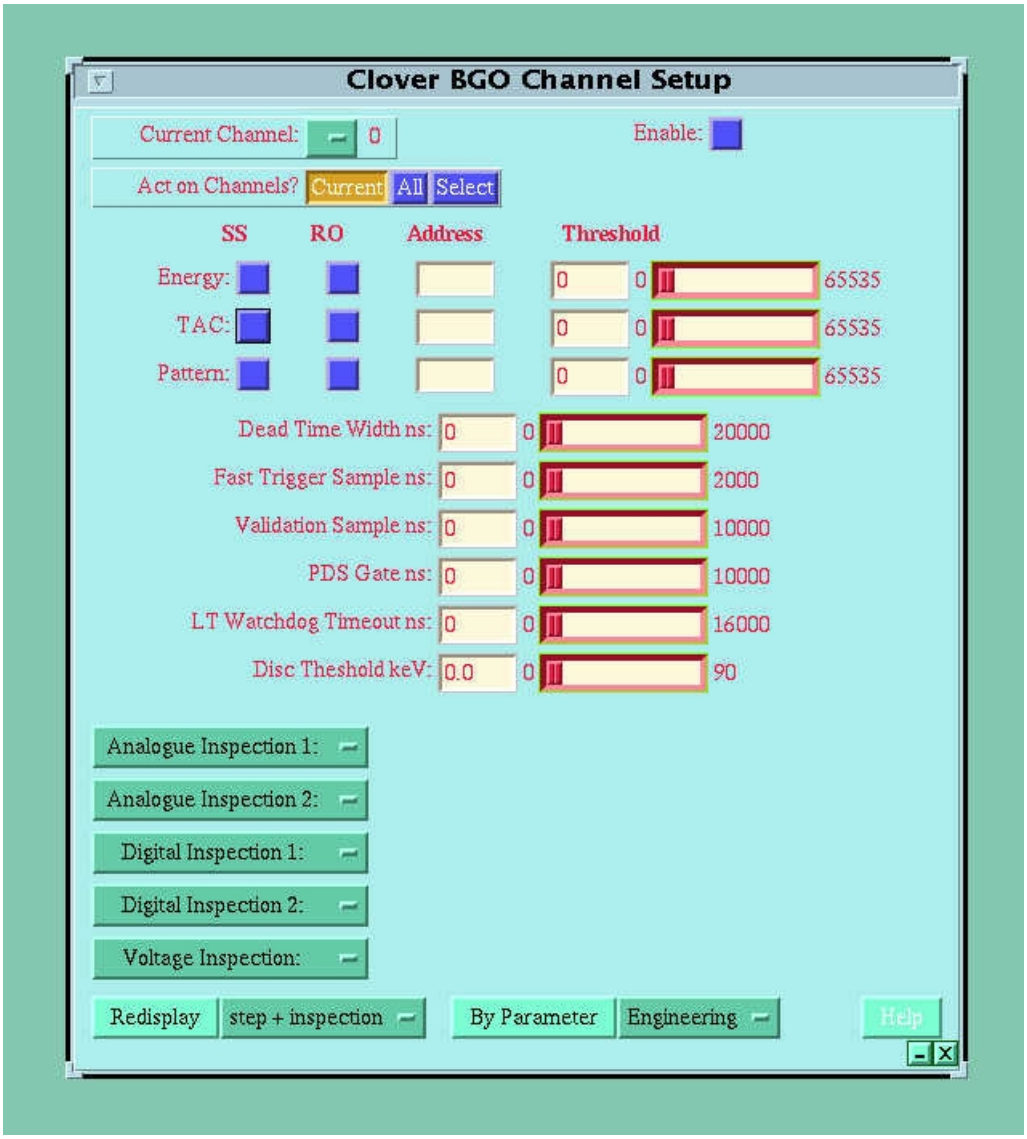

Fig 6 Clover Card BGO channel control window

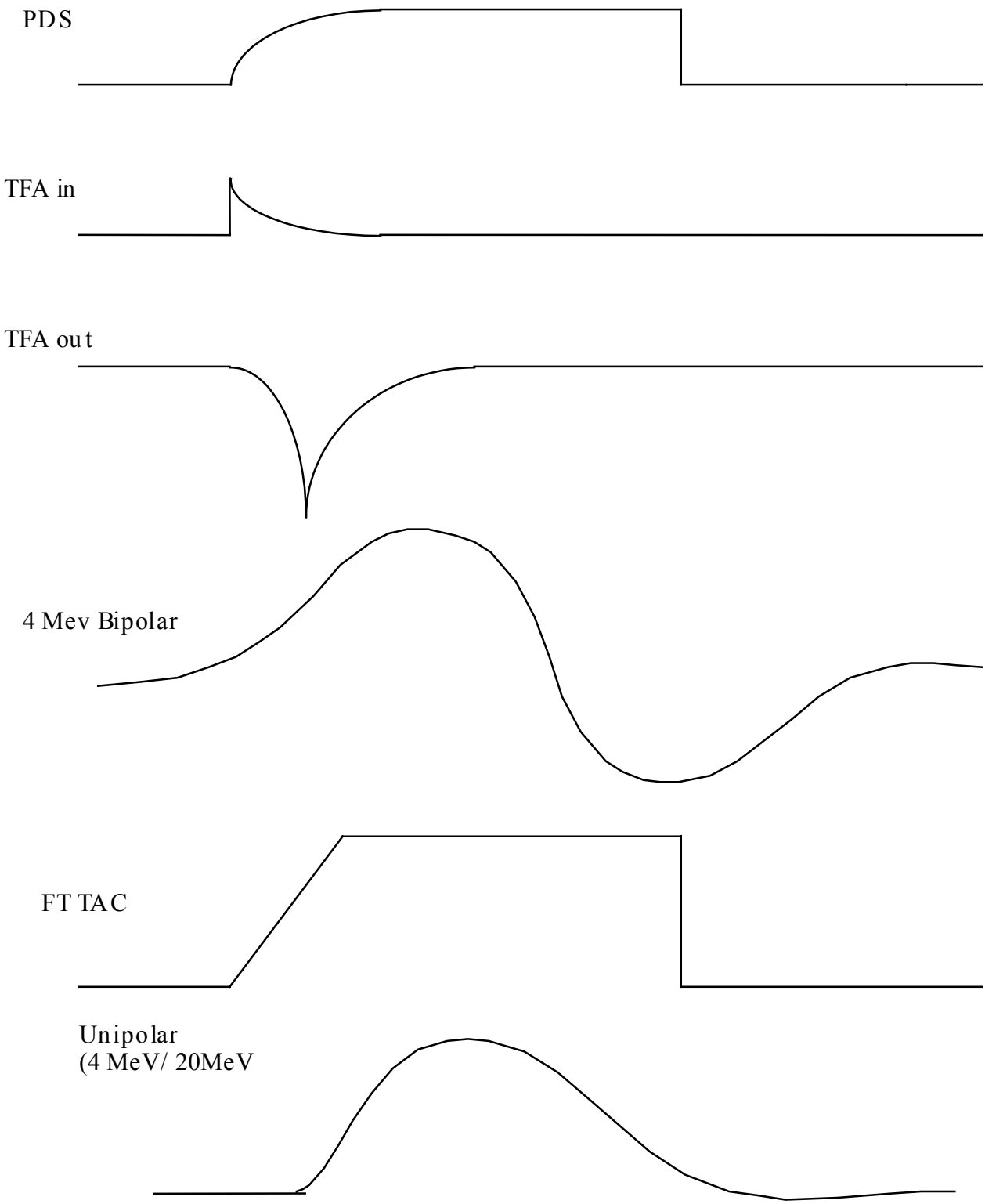

Fig 7 Ge Analogue inspection line signals

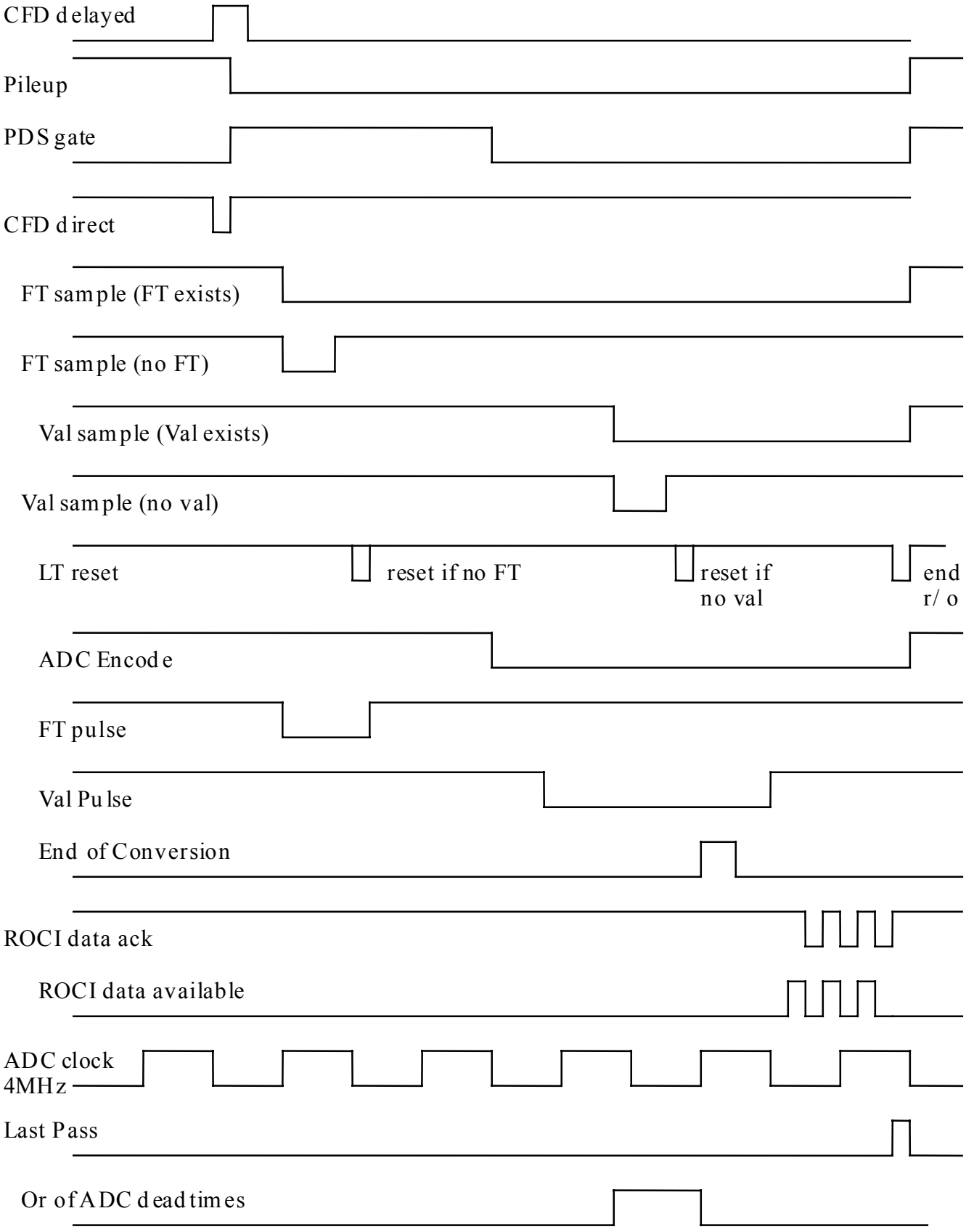

Fig 8 Ge Logic inspection signals

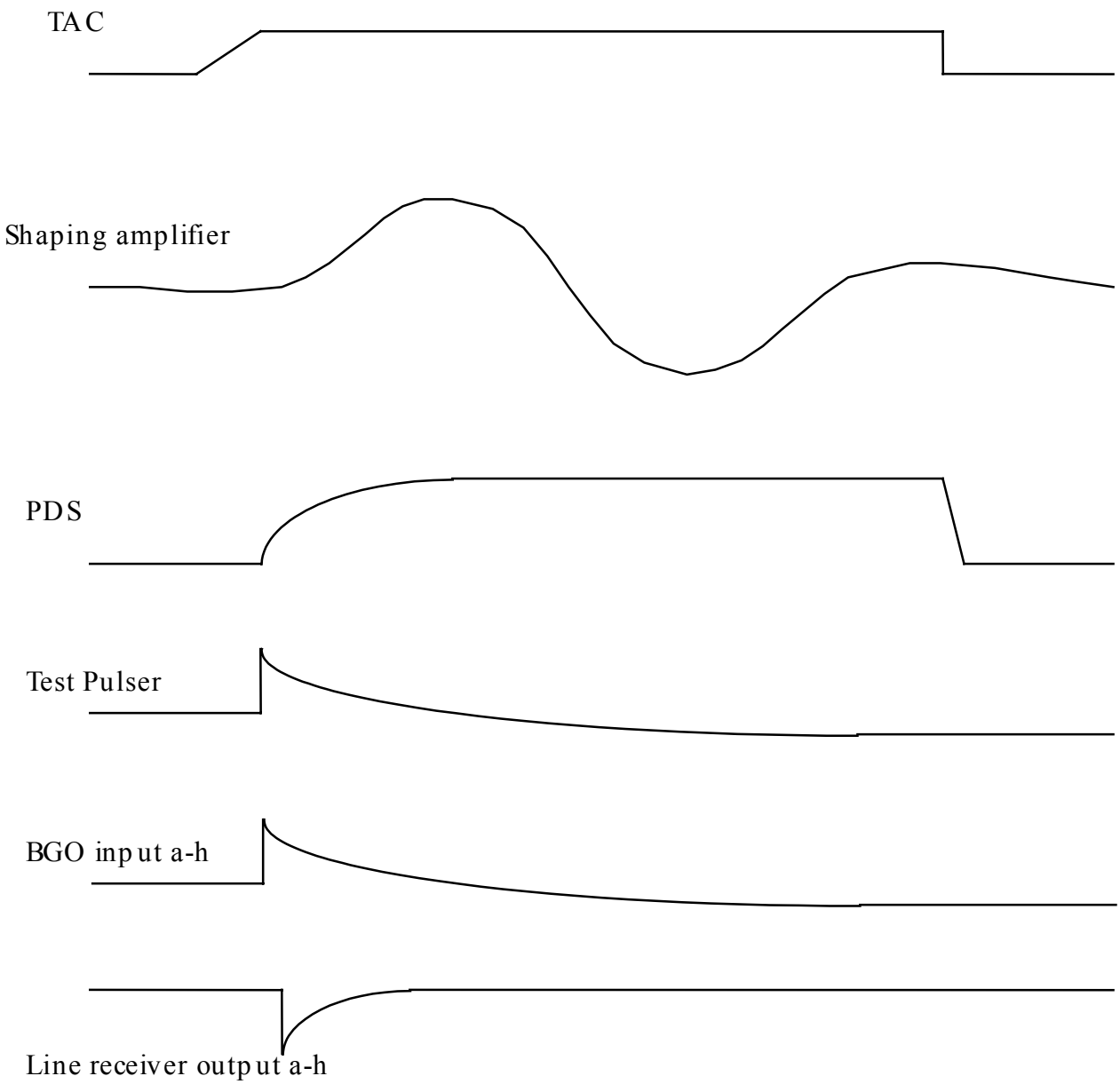

fig 9 BGO Analogue Inspection Lines

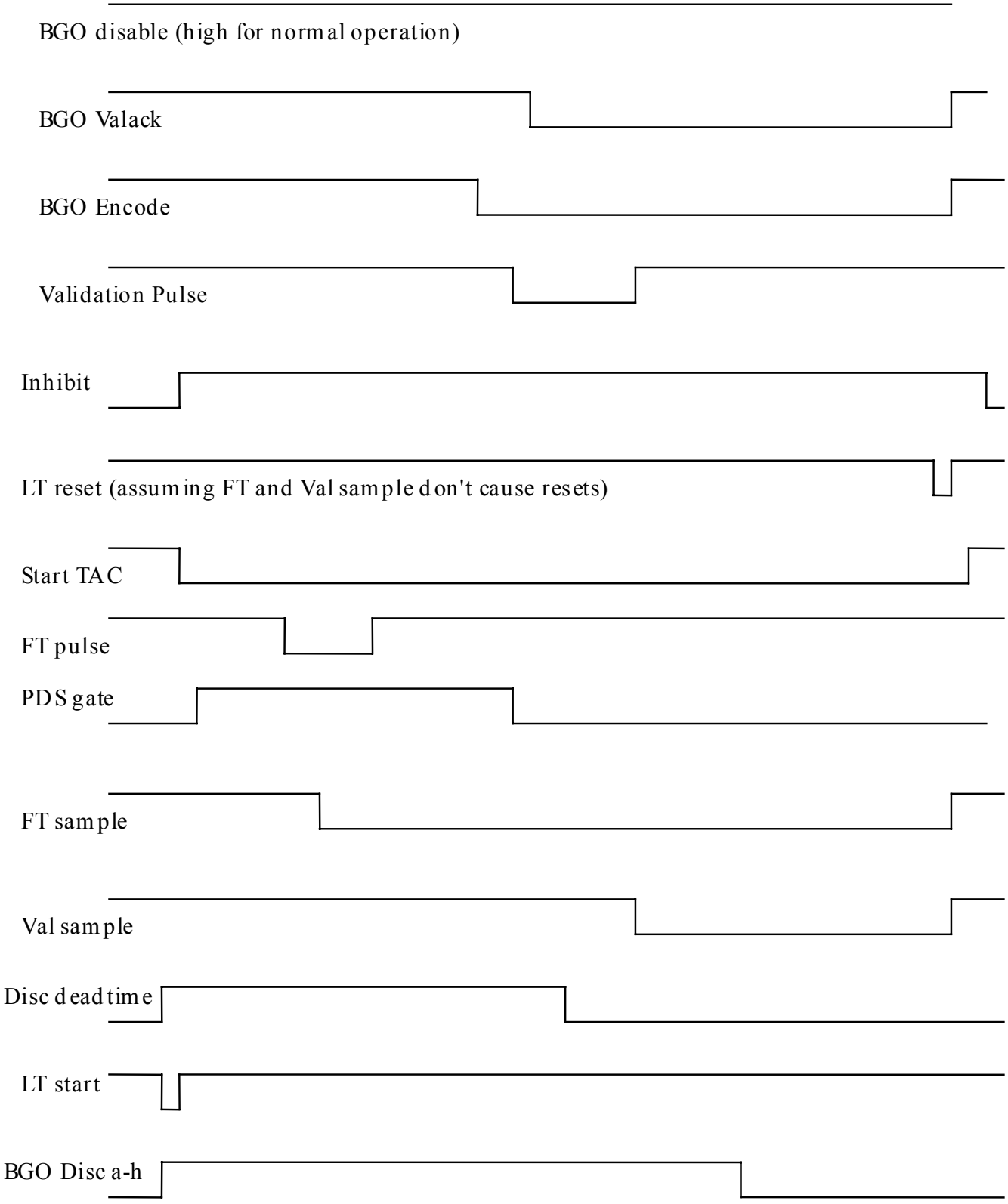

fig 10 BGO logic inspection lines

Details of registers and Addresses for Software Developers

Address Space (offset into VXI address space)	Name
0x0000 to 0x00fe	Ge Common parameters (“Channel 0”)
0x0100 to 0x01fe	Channel 1 Parameters (Ge A)
0x0200 to 0x02fe	Channel 2 Parameters (Ge B)
0x0300 to 0x03fe	Channel 3 Parameters (Ge C)
0x0400 to 0x04fe	Channel 4 Parameters (Ge D)
0x0500 to 0x05fe	Channel 5 Parameters (Ge Spare)
0x0600 to 0x06fe	Channel 6 Parameters (BGO)
0x0700 to 0x07fe	BGO Common parameters (“Channel 7”)
0x2000 to 0x3ffe	Veto Pattern logic Table

Channel 0 Sub-Address Spaces	Function
0x0000 to 0x002e	Ge Common Parameters
0x0030 to 0x00fe	Module Parameters (common to Ge & BGO)

Ge Common Parameters

Name	Offset	Access	Old Ge offset
CFD Width DAC (8 bits)	0x0000	w	0x0000
FT Sample Point DAC (8 bits)	0x0002	w	0x0002
Validation Sample Point DAC (8 bits)	0x0004	w	0x0004
LT watchdog DAC (8 bits)	0x0006	w	0x0006
Test Generator Amplitude DAC (16 bits)	0x0010	w	0x0010

Module Parameters (Common to Ge and BGO parts)

Name	Offset	Access	Old Ge/BGO offset
Analogue Multiplexor Selection	0x0030	w	0x0030
Digital Multiplexor Selection	0x0032	r/w	0x0032
Voltage Inspection Line Selection	0x0034	r/w	0x0034
Controle des Fenetres	*0x0038 bit 6*	r/w	0x0036
Module Configuration Register	0x0038	r/w	0x0038
Test Pulse Attenuator on/off (Ge only)	*0x0038 bit 7*	r/w	0x003a
Test Write to Readout Data FIFO	0x003c	w	0c003c
Test Read from Readout Data FIFO	0x003c	r	0x003e (NB change)

Module Control Register (0x0038)

d15-8 =x	d7	d6	d5	d4	d3	d2	d1	d0
0x38	Test Att on = 1	CDF on =1	not used	not used	1 = Reset FIFO	not used	0 = Rej 1 = mark	LastCard = 1

Channels 1-6

The addresses within the spaces allocated to channels 2 to 5 (Ge A to Ge E) are the same as on the phase 1 Ge Card. The addresses within channel 6 (BGO) are the same as those within channel 6 of the phase 1 BGO card. This permits the software to treat these channels exactly as at present which means that the EUROGAM Register Server software and the EG Session Ge and BGO windows can be used with few changes.

Ge channel Parameters (Channels 1-5)

Name	Offset	Access	Old Ge offset
CFD Threshold (8 bits)	0x0100 etc.	w	0x0000
CFD Delay (8 bits)	0x0102 etc.	w	0x0002
PZ adjust DAC (8 bits)	0x0104 etc.	w	0x0004
PDS gate width DAC (8 bits)	0x0106 etc.	w	0x0006
Channel Control Register	0x0120 etc.	r/w	0x0020

Ge Channel control register:

d15-8 =x	d7	d6	d5	d4	d3	d2	d1	d0
0x120 etc	not used	not used	1 = CFD Disable	1=Test Mode	not used	TFA gain 1=low	not used	not used

BGO channel Parameters (Channel 6)

Name	Offset	Access	Old BGO offset
BGO Threshold (12 bits)	0x0600	w	0x0000
BGO Test Pulser (12 bits)	0x0602	w	0x0002
Channel Control Register	0x0620	r/w	0x0020

BGO Channel control register (0x620):

d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
n/u	n/u	n/u	n/u	n/u	1= Ch dis.	n/u	n/u	1=TG ON	1=TG ON	1=TG ON	1=TG ON	1=TG ON	1=TG ON	1=TG ON	1=TG ON

BGO Common Parameters (Channel 7)

Name	Offset	Access	Old BGO offset
Discriminator DeadTime DAC (8 bits)	0x0702	w	0x0002
FT Sample point DAC (8 bits)	0x0706	w	0x0006
Validation Sample Point DAC (8 bits)	0x0708	w	0x0008
LT Watchdog (8 bits)	0x070a	w	0x000a
PDS Gate Width DAC (8 bits)	0x070c	w	0x000c

Inspection Lines

The Ge and BGO inspection lines are combined as follows:

Channel	Function
Channel 0	Disconnect Inspection Line
Channel 1	Ge channel 1
Channel 2	Ge channel 2
Channel 3	Ge channel 3
Channel 4	Ge channel 4
Channel 5	Ge channel 5 (spare)
Channel 6	BGO channel
Channel 7	Ge common parameters (logic only)

Channels 6 and 7 overlap on certain signals such as Fast Triggers and Validations, but since the Ge and BGO use different FT sample points, it is not unreasonable to keep the two sets of inspection lines entirely as they are now. This has the advantage also that all the phase 1 inspection line software can be re-used. The BGO elements s1-s8 map onto the old a-h inspection lines (analogue and digital); the old i and j inspection lines are not used on phase 2. The address mapping is not exactly as phase 1 and is shown in detail later along with the Voltage Inspection lines.

Veto Pattern Look-up Table

The pattern for Veto generation is loaded into a 8Kx4 memory array whose inputs are the pattern from the 8 BGO and 5 Ge discriminators and outputs are signals to determine the following:
* Veto the event?
* Drive Raw Ge sumbus?
* Drive Clean Ge sumbus?
* Drive BGO sumbus?

This table is controlled by word access at addresses from offsets 0x4000-0x7ffe, each address corresponding to one possible pattern of discriminators. The pattern will be:

not used	not used	not used	Ge Sp	Ge D	Ge C	Ge B	Ge A	s8	s7	s6	s5	s4	s3	s2	s1
msb															lsb

The data at each location is:

not used	not used	not used	not used	1= BGO sumbus on	1= Cl Ge sumbus on	1=Raw Ge sumbus on	1= Veto event.
d7	d6	d5	d4	d3	d2	d1	d0

Multiplexors and Voltage Inspection Lines

d15	d14	d13	d12	d11	d10	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00
fn 5	fn 4	fn 3	fn 2	fn 1	ch 3	ch 2	ch 1	fn 5	fn 4	fn 3	fn 2	fn 1	ch 3	ch 2	ch 1
Multiplex (analogue and digital) line 2								Multiplex (analogue and digital) line 1							

Ge (ch1-5) Function field: Analogue Muxes	**Name**
0	PZ Adjust
1	4 MeV Unipolar
2	20 MeV Unipolar
3	FT TAC out
4	4 MeV Bipolar
5	TFA Output
6	TFA Input
7	4MeV PDS

BGO (ch6) Function field: Analogue Muxes	**Name**
0	TAC output (mtxa110)
1	Shaping Amp output (mtxa111)
2	PDS output (mtxa112)
3	Test Generator output (mtxa113)
4	Renin* (active L)
5	Renout* (active L)
6	FIFOdtack (active H)
7	Lecture (active H)
8	BGO Input H (mtxa121)
9	BGO Input G (mtxa120)
10	BGO Input F (mtxa119)
11	BGO Input E (mtxa118)
12	BGO Input D (mtxa117)
13	BGO Input C (mtxa116)
14	BGO Input B (mtxa115)
15	BGO Input A (mtxa114)
16	Line Receiver output A (mtxa107)
17	Line Receiver output B (mtxa106)
18	Line Receiver output C (mtxa105)
19	Line Receiver output D (mtxa104)
20	Line Receiver output E (mtxa103)
21	Line Receiver output F (mtxa102)
22	Line Receiver output G (mtxa101)
23	Line Receiver output H (mtxa100)
24	BGO Input H (mtxa121)
25	BGO Input G (mtxa120)
26	BGO Input F (mtxa119)
27	BGO Input E (mtxa118)
28	BGO Input D (mtxa117)
29	BGO Input C (mtxa116)
30	BGO Input B (mtxa115)
31	BGO Input A (mtxa114)

Ge (ch1-5) Logic Inspection Function Select	Meaning
0	CFD Delayed Output
1	Pre-pulse Pileup
2	PDS Gate
3	CFD Direct Output
4	FT Sample Point (W1)
5	Val Sample Point (W2)
6	LT reset
7	ADC Encode Command

BGO (ch 6) Logic Inspection Function Select	Meaning
0	BGO Disable (mtxd118e)
1	BGO Valack (mtxd119)
2	BGO Encode (mtxd120)
3	Validation Pulse
4	Inhibit (Active Low)
5	LT reset
6	spare
7	spare
8	BGO TAC Start Pulse (mtxd110)
9	Fast Trigger Pulse
10	BGO PDS Gate (mtxd112)
11	BGO Fast Trigger Sample Point (mtxd113)
12	BGO Validation Sample Point (mtxd114)
13	BGO LT RO gate test point (mtxd115)
14	BGO Discriminator Deadtime (mtxd116)
15	BGO LT Start (orcfd-orlrec)
16	BGO disc h (mtxd100)
17	BGO disc g (mtxd101)
18	BGO disc f (mtxd102)
19	BGO disc e (mtxd103)
20	BGO disc d (mtxd104)
21	BGO disc c (mtxd105)
22	BGO disc b (mtxd106)
23	BGO disc a (mtxd107)

Common (ch 7) LI line function select	Meaning
0	Fast Trigger Pulse
1	Validation Pulse
2	End of ADC Conversion
3	ROCI Data Acknowledge
4	OR all 6 ROCI Data Available (Active Low)
5	ADC Clock (4 MHz)
6	Last Pass
7	OR of ADC deadtimes

Voltage Inspection Lines

d7	d6	d5	d4	d3	d2	d1	d0
not used	V Select 4	V Select 3	V Select 2	V Select 1	Mux Sel 3	Mux Sel 2	Mux Sel 1
Voltage Inspection Lines: Bottom 3 lines select the Mux chip, and next 4 lines address it.							

Voltage Inspection Code (Data 7..0)	**Meaning**
xxxxx 000 (0, 8, 16, 24 etc)	Not connected to VXI
x0000 001 (1)	Ge 1 CFD Threshold (VO1(1))
x0001 001 (9)	Ge 1 CFD Output Delay (VO1(2)
x0010 001 (17)	Ge 1 PZ Adjust (VO1(3))
x0011 001 (25)	Ge 1 PDS gate (VO1(4))
x0100 001 (33)	Ge 2 CFD Threshold (VO1(5))
x0101 001 (41)	Ge 2 CFD Output Delay (VO1(6))
x0110 001 (49)	Ge 2 PZ Adjust (VO1(7))
x0111 001 (57)	Ge 2 PDS gate (VO1(8))
x1000 001 (65)	Ge 3 CFD Threshold (VO2(1))
x1001 001 (73)	Ge 3 CFD Output Delay (VO2(2)
x1010 001 (81)	Ge 3 PZ Adjust (VO2(3))
x1011 001 (89)	Ge 3 PDS gate (VO2(4))
x1100 001 (97)	Ge 4 CFD Threshold (VO2(5))
x1101 001 (105)	Ge 4 CFD Output Delay (VO2(6))
x1110 001 (113)	Ge 4 PZ Adjust (VO2(7))
x1111 001 (121)	Ge 4 PDS gate (VO2(8))
x0000 010 (2)	Ge 5 CFD Threshold (VO3(1))
x0001 010 (10)	Ge 5 CFD Output Delay (VO3(2)
x0010 010 (18)	Ge 5 PZ Adjust (VO3(3))
x0011 010 (26)	Ge 5 PDS gate (VO3(4))
x0100 010 (34)	Ge Test Pulser Output Level
x0101 010 (42)	CFD Width
x0110 010 (50)	Ge Fast Trigger Sample Point (DW1)
x0111 010 (58)	Ge Validation Sample Point (DW2)
x1000 010 (66)	Ge LT timeout (DW3)
x1001 010 (74)	BGO Threshold
x1010 010 (82)	BGO Test Pulser Output Level (MTXC6)
x1011 010 (90)	BGO DAC ref (MTXC13)
x1100 010 (98)	BGO Fast Trigger Sample Point (MTXC15)
x1101 010 (106)	BGO Validation Sample Point (MTXC16)
x1110 010 (114)	BGO LT Timeout (MTXC17)
x1111 010 (122)	BGO PDS Gate (MTXC18)
x0000 011 (3)	VREFDAC (Ge DAC reference)
x0001 011 (11)	Vee24
x0010 011 (19)	Vee18
x0011 011 (27)	Vee12
x0100 011 (35)	Vee6
x0101 011 (43)	Vee (-5.2V)
x0110 011 (51)	Vee2
x0111 011 (59)	+3V regulator (BGO DAC ref)
x1000 011 (67)	Ground
x1001 011 (75)	Vcc5 Analogue
x1010 011 (83)	Vcc5 Digital
x1011 011 (91)	Vcc6
x1100 011 (99)	Vcc12
x1101 011 (107)	Vcc18
x1110 011 (115)	Vcc20
x1111 011 (123)	Vcc24
xxxxx 1xx	Connected to VXI, but not allocated on card

Inhibit and Sumbus System description (added April 1996)

The Inhibit system logic applies a card level inhibit (signal name inhibecom) whenever one of these 2 conditions is true using a logic OR (IC 17, 27 and 28 on page 11 of circuits):
1) The system's Inhibit Action VXI line is true (0v on backplane)
2) The card is set to Reject (not Mark) mode AND either there is pre-pulse pileup in one of the 5 Ge channels OR there is a Veto from the Sumbus/Veto LookUp Table.

The duration of the card level inhibit is set by:
1) the duration of the system's Inhibit Action signal (until end of readout in CDT mode)
2) the duration of the pre-pulse pileup (7μs) or the Veto (until LT reset)
If both conditions are true then the duration is set by the longer.

The front edge of the card level inhibit is also used to enable the serialisation of the status of the input pattern by the pattern unit (M30). This level must be maintained until parallel to serial conversion is finished.

The inhibit to each of the LT circuits has an inhibit over-ride using that LT's LtStartN signal which prevents the application of an inhibit once the LT is busy. (If Inhibit is applied to a busy LT and the LT's CFD fires again, then that LT will be reset prematurely.)

The sumbus drivers are controlled by a PAL which gates the LUT output with a delayed version of the OR of the Ge CFD outputs. Whenever the CFD's fire, the current pattern of local trigger LtStart signals and BGO line receivers which is applied to the LUT will determine whether or not the sumbuses are driven. In the case of the Ge LT's this will be "stale" latched information if there is a card level inhibit preventing changes in LT state.

In parallel mode the InhAction signal will be short, but the card level inhibit will be extended to 7μs by the pre-pulse pileup (amplifier busy) signals if the reject mode is enabled. *Check how long it takes to serialise the LtStart pattern: maybe we need to stretch the InhAction locally to make a proper card deadtime signal?*

Sumbus deadtime (Added August 1999)

The sumbus inhibit problem described above has a second effect which is to disable the sumbus Ge outputs while Inhibit Action is asserted, regardless of whether this clover is part of the event. The problem can be overcome for the Raw Ge sumbus only in the LUT by programming the all the RawGe entries to be always 1 so that the Raw Ge sumbus is driven whenever the OR of the Ge CFDs is true, regardless of the Ge pattern bits from the LT Start signals. This method can be extended to a simple suppression on the Clean Ge sumbus too by programming the LUT with a "don't care" state in all the 5 Ge bits and using the OR of the Ge CFDs to indicate that one or more of the Ge channels has been hit. The Clean sumbus output from the LUT would be driven then whenever all 8 BGO bits are 0 and the OR of the Ge CFDs is true, regardless of the state of the 5 Ge LT start LUT inputs. NB this LUT configuration is incompatible with the complex Ge pattern based Vetos, but these are rarely/never used anyway so it is not really a problem that they are unavailable.

Data Format Description (Added August 1999)

The data format produced from the Clover card readout is as follows:

Q1	Q0	I5	I4	I3	I2	I1	I0	G7	G6	G5	G4	G3	G2	G1	G0
Qualifiers *See below*		Item *Identifies parameter within clover*						Group *MIDAS sets this within range allocated to clovers*							
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16

The top 16 data bits always look like this and are followed by 16 bits of data as follows:

Pattern word:

not used	*not used*	*not used*	Ge E	Ge D	Ge C	Ge B	Ge A	s8	s7	s6	s5	s4	s3	s2	s1
D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

Energy Data Words (all types):

not used	*not used*	*not used*	E MSB	E	E	E	E	E	E	E	E	E	E	E	E LSB
D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

TAC Data Words (all types)

not used	*not used*	*not used*	T MSB	T	T	T	T	T	T	T	T	T	T	T	T LSB
D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

Qualifiers:

The Ge qualifiers have the following meanings depending on which data word they come with:

Q1, Q0	Spectrum	20MeV	4MeV	FT TAC	CO TAC
00	q0	clean data	clean data	all data	no pileup
01	q1	A/C Veto	A/C Veto	not used	post-pulse pileup
10	q2	Pileup (pre or post)	Pileup (pre or post)	not used	pre-pulse pileup
11	q3	Pileup and A/C Veto	Pileup and A/C Veto	not used	pre and post pileup

The BGO qualifiers are always set to 1,1 for compatibility with the EG 1 BGO cards.

Warning

Users must not remove the shields from the cards. There are no user serviceable parts inside. There are, however, static sensitive components which can be easily damaged by incorrect handling procedures.

Jumpers.

These adjustments should not be attempted by a user. Please contact an engineer.

ST 1,2,3,4,5 must always be inserted to ground the positive input to the shaping amplifiers.

ST8 controls whether the sliding scale is on or off. Shipped in the “on” position.
Top=On
Bottom = Off

ST20 controls whether the BGO channel is started by just the OR of the 5 Ge CFDs or the OR of the BGO inputs OR'ed with the 5 Ge CFDs. Shipped in the “BGO or Ge” position.
Top=Ge only
Bottom= Ge OR BGO

Adjustments.

There are no user adjustments on the card itself.

The ADC sliding scale is set during commissioning and should not be changed.
(On the ADC there are 2 pots: 47k sets DC level and 1k sets gain for SS adjustment.)

The sumbus current output levels are set during commissioning and should not be changed.
(R244 sets BGO sumbus, R274 sets Clean Ge sumbus, R300 sets Raw Ge sumbus)

Power supplies.

Voltage	Typical current (amps)	Typical Power (Watts)
-2V	0.5	1
+5V	2.3	11.5
-5.2V	6.1	31.8
+12V	1.9	22.8
-12V	1.6	19.2
+24V	0.1	2.4
-24V	0	0
		Total 89 Watts

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