AGATA

DIGITISER

DRAFT 4.1

Fig1 Cluster of Digitisers

This documents has been written in collaboration by:
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I. INTRODUCTION.

This document has been written following discussions with the Preamplifier Team, the Detector Team and Local Level Pre-processing Team.

The objective is to create the best design ensuring good quality of the data to be sent to the preprocessing card, and enabling easy maintainability of the system during the experiment and in an electronics workshop.

The Digitiser Team is constituted from the technical groups of 3 Laboratories:

_ **IReS Institut de Recherche d'étude Subatomique** [IN2P3 / CNRS (1)]
_ **Daresbury Lab Nuclear Physics Group** , [CLRRC (2)]
_**University of Liverpool Nuclear Physics** [Electronic Design group (3)]

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II. OVERVIEW OF THE DIGITISER.

II-1 System description.

The principal goal of the digitiser card is to make the interface between the detectors and the preprocessing module.

The Digitiser will do the following:

- Receive the signals from 1 crystal, (36 segments + 1 core).
- Digitise the input signals at a rate of 100 MHz, with 14 bit ADCs.
- Send the signals coded by optical fiber by group of 6.
- Send the Core CFD logic signal to the pre-processor for Ancillary detector using fibre-optic link.
- Provide spare channels and inspection lines for maintainability.
- Provide an interface for re-programming, and control in an electronics workshop
- Provide an interface for slow control during experiments.
- To be mounted a less than 5 m from the Detector Preamplifier.

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II-2 Block diagram.

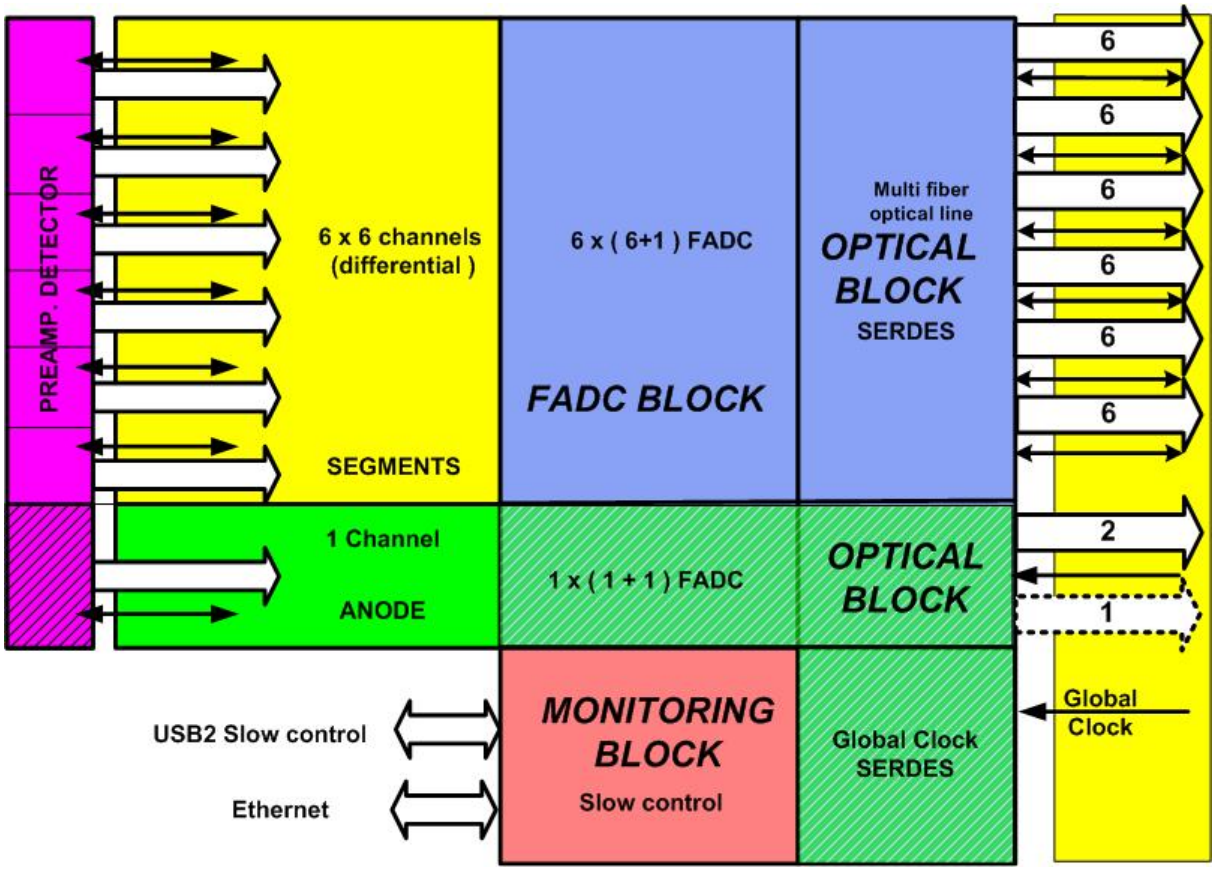

Fig2 Block diagram

FADC block:

The FADC cards contain 100 MHz ADCs producing 14 bit wide data plus other signals needed by the pre-processor.

Monitoring block / Optical block:

The Monitoring block provides control of the spare channels and inspection lines via a slow control link to the GUI system control software. The temperature of the various parts of the digitiser electronics will be accessible to this slow control link.
The FADC card outputs pass through a serialiser circuit permitting the use of fiber-optic links between the ADCs and the pre-processing cards to give flexibility for future upgrades of pre-processing electronics and maximum electrical isolation.
The serialiser will be integrated in the VIRTEX2 FPGA (Rocket I/O). One 12 channel fibre-optic transmitter will be used to each group of 6 segment channels. One optical interface with a low data rate will be used for offset control from pre-processing card for each group of 6 channels.
One 8 channel fiber-optic transceiver (4 RX, 4TX)link will be used to connect to the pre-processing card for the core FADCs data, timing and control The transmit channels will be used for the core 100Mhz FADC data (two channels), the core CFD logic signal (one

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channel), and the Global clock calibration feedback path(one channel). The receive channels will be used for the Global clock signal, the Synchronisation signal, and the offset controls for the core electronics.

III. DESCRIPTION.

III-1 Monitoring.

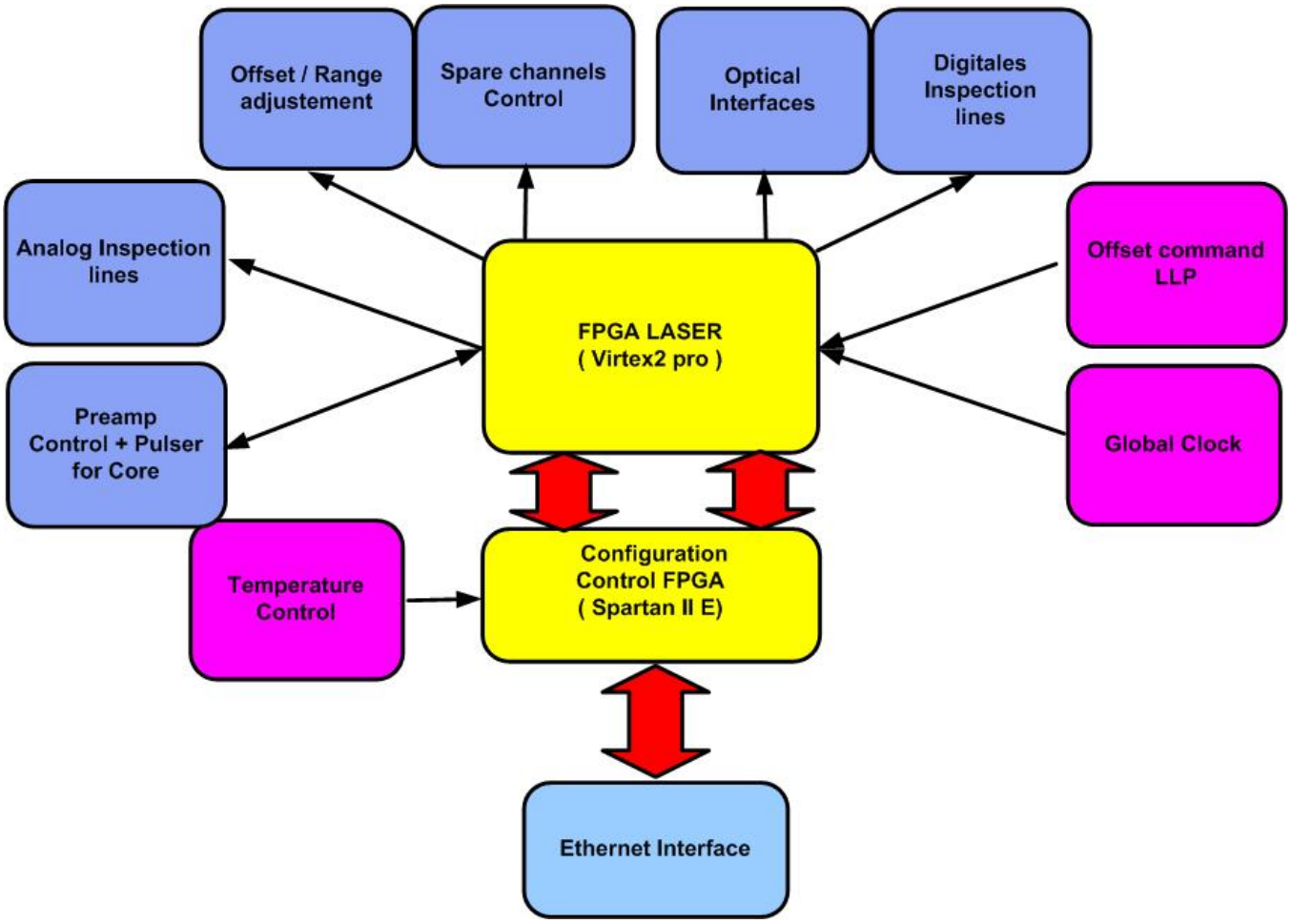

Fig3 Block diagram for Control

a) Temperature Control.

This part will have to manage the monitoring of the temperature of both the digitiser box and FADC and if necessary its regulation. For the final modules one could envisage simplifying it but not for the first prototypes. The values of the temperatures will be recorded in a fifo in order to enable their inspection over time. These temperature values will be available for external monitoring via the slow control interface.

b) Preamplifier Control and Pulser for Core.

This part will manage the control interface for the Core and Segment preamplifiers and the pulser for the Core

c) Analog inspection lines.

Each analog channel from the detector can be inspected before and after coding. Two analogue lines will exist per group of 6 segments channels. These inspection lines will be disabled in an experiment.

d) Offset adjustment and Range monitoring.

The offset value required will be calculated by the pre-processing or the digitiser card to make maximum use of the ADC dynamic range. The adjustments are made by a DAC on each channel. The monitoring block has to control each DAC. There is one DAC per channel. Two input ranges exist for each channel but only one can be selected at a time for each group of 6 channels.

e) Spare Channel control.

- 1 spare FADC input for each group of 6 inputs. The FPGA will rout the output of the spare channel to the data link for the channel to be replaced.
- 1 spare FADC input for the core always enabled.

f) Optical interfaces.

The FADC output (14bits + overflow) and the Inhibit signal (Pion measurement) give a bus with 16 bits. This will be serialised by the Rocket I/O of the Virtex2 Pro FPGA. To transfer this data we need a data rate of 2Gbits/sec .To simplify the Digitser we'll use Parallel Optical Link Transmitter with 12 channels of which only 6 will be used for the serialised data.

One 8 channel fiber-optic transceiver (4 RX, 4TX)link will be used to connect to the pre-processing card for the core FADCs data , timing and control The transmit channels will be used for the core 100Mhz FADC data (two channels), the core CFD logic signal (one channel), and the Global clock calibration feedback path(one channel). The receive channels will be used for the Global clock signal, the Synchronisation signal, and the offset controls for the core electronics.

For the segment offset control we'll use a 100MB/s optical interface as proposed by Agilent in the "Inexpensive 20 to 160 MBd Fiber-Optic Solutions" Application note 1123.

All the optical interfaces include a monitoring function for the laser diodes, these monitors will be available using the slow control.

g) Digital Inspection Lines.

The output of an FADC can be routed, within the FPGA, to one of two DACs with buffered outputs available at the front panel. This will assist in commissioning and fault finding in the electronics lab.

h) Offset command LLP.

The Offset command link will operate via this interface. For the segment offset control we'll use a 100MB/s optical interface as proposed by Agilent in the "Inexpensive 20 to 160 MBd Fiber-Optic Solutions" Application note 1123.

One line will control a group of 6 segment channels.

i) Global Clock.

The Global Clock function will have to reconstruct a high quality clock with a very small jitter (<7pS). This clock will be received through one optical receiver within the core

transceiver. When used in an electronics workshop the digitiser will have to provide its own clock signal for coding (independent of an external system of clock).

j) Ethernet Interfaces.

For slow control an Ethernet Interfaces module will be integrated in the Digitiser. The data rate is slow but good enough for this application. The Ethernet enables the Virtex2pro to be re-programmed without disassembling the digitiser module, and is used to slow control the experiment. This interface will respect the galvanic isolation.

III-2 HARDWARE DESCRIPTION.

III-2-1 FADC SEGMENT BLOCK

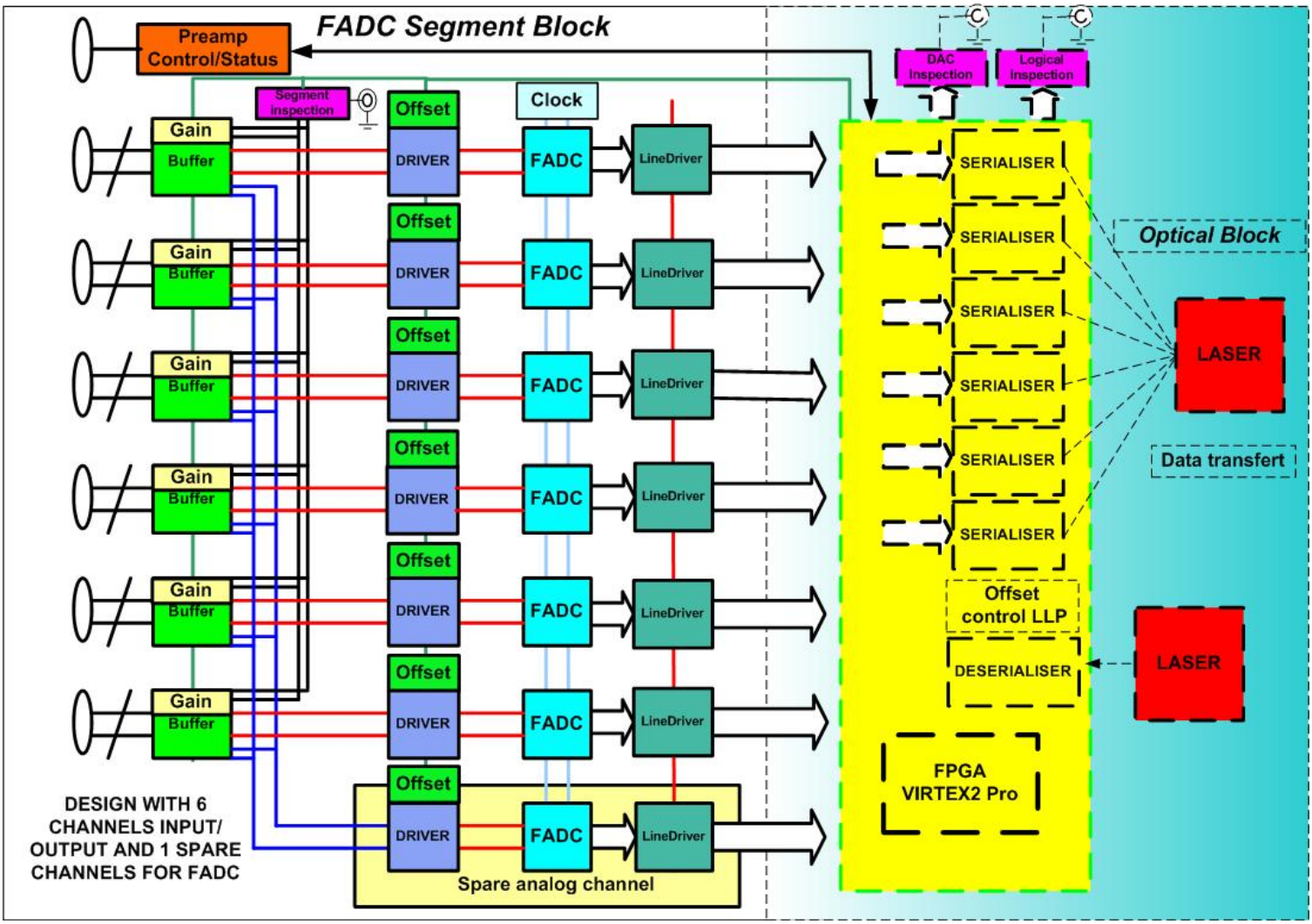

Fig4 Diagram for segment input

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a) Buffer

The Buffer module provides impedance matching and routing of the signals between the FADC, the spare channel, and inspection lines. The input signals are differential. The buffer module includes the range selector.

b) Offset

The offset value required will be dynamically calculated by the pre-processing or the digitiser to maximise the input dynamic range.

c) Driver

The driver adds the offset signal. The anti-aliasing filter is included in the Driver before the FADC. All the offset DACs are based on the same chip: PCM56. We have a great deal of experience with the performance of this device. It has a low noise level, is bipolar, and has a serial control interface. The output will be connected to two buffers, one with a gain of one and the other with a gain of -1. We'll use the Texas ultra low noise buffer OPA692

d) FADC

The ADC must have 14 bits 100 MHz. 16 data bits are sent to the FPGA; bits 0 to 13 are data, bit 14 is the FADC overload and bit 15 could be used as a synchronisation pulse. The overload bit could also be transmitted to the preamplifier for the Pole Zero reset through the FPGA. The ADC is the AD6645 100MHz from Analog Devices.

e) Line Driver

It avoids capacitive loading of the data bus at the output of the FADC, and allows the FADC data bus to be transmitted to the Laser card.

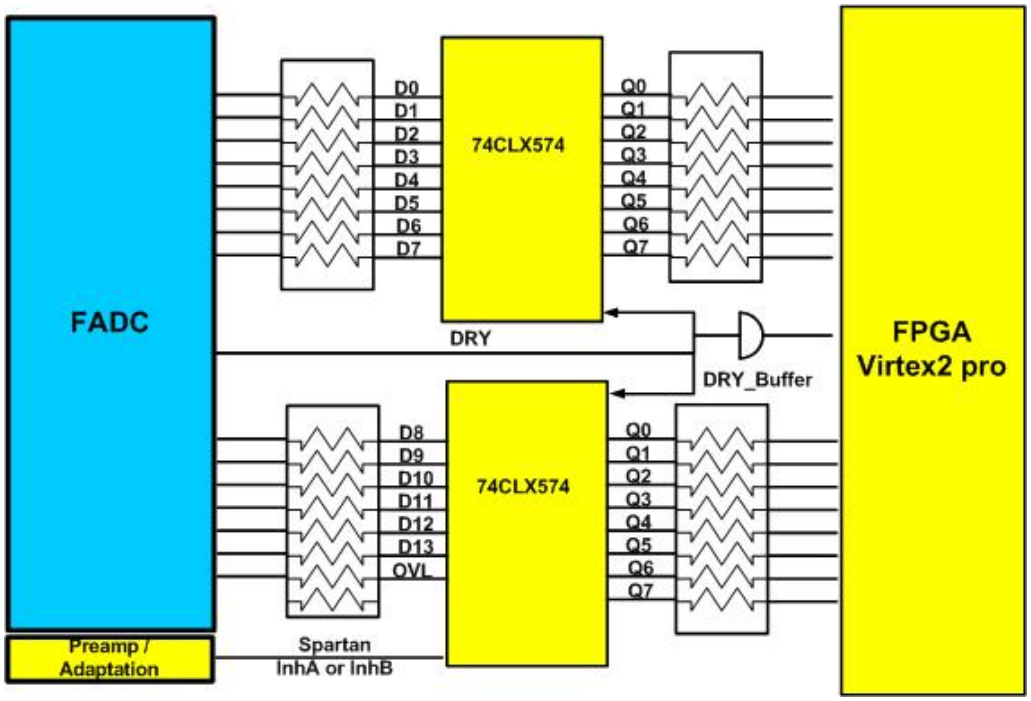

Fig5 Segment Buffer line

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f) Clock

The clock module receives the clock from the digitizer internal Global Clock distribution and transmits it to the FADCs with minimal skew and the smallest possible jitter.

g) Preamp/Control Status

This part assumes the optical isolation from the Digitiser to the Preamplifier.

III-2-1-1FADC segment module details:

a) Buffer Input/Analog inspection line.

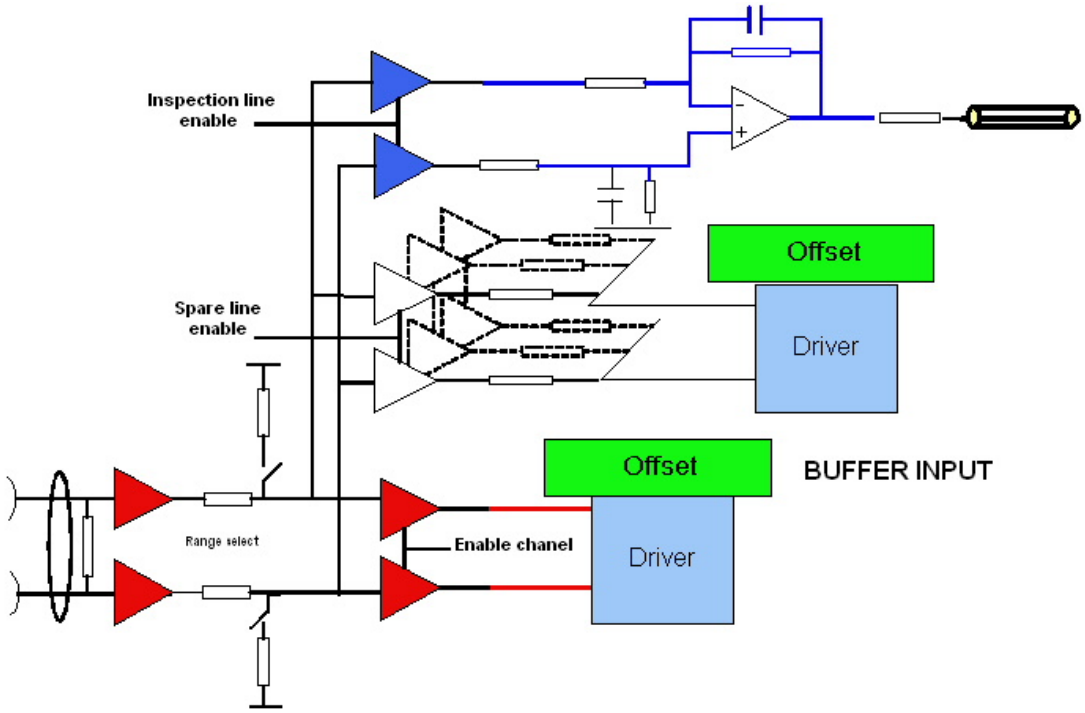

Fig 6 Connections between Spare line / Buffer input / Inspection line

For the buffers at the input we will use OPA692 or OPA2692 (Dual OPA 692) from Texas with disable output, low noise level, and fixed gain.

If the spare channel is needed the 'red' buffers will be disabled and the white buffers will be enabled ***{ there are four red buffers, I think you need to change the colour of the input buffers so there are only two ;-) }***. If we need to check the signal through the inspection line the blue buffer will be enabled.

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b) Range

It has been decided that the analog chain should be designed so as to guarantee the best energy resolution with the typical gain range selection (0-5 Mev), giving the user the option to attenuate the analog signal in front of the ADC so as to extend the range.

Normal Range: 0 – 5 Mev
Extended Range: 0 – 20 Mev

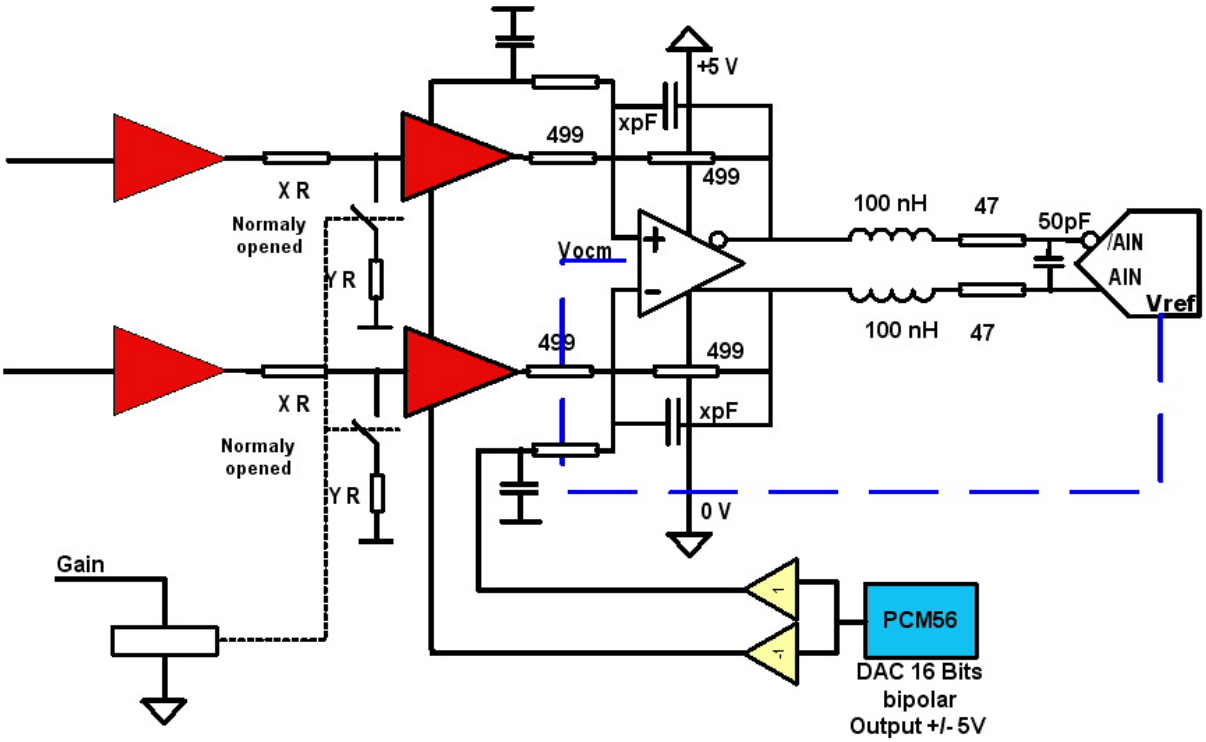

Fig 7 Driver / Offset

c) Driver / Offset

For the FADC driver we will use the AD8138 from Analog Device.
To keep the advantage of the differential signal and after discussion with the Preamplifier Team we'll use the following devices:

_ First buffer could be AD8056 or OPA2692
_ The second stage could be the OPA 692.

d) Preamp Control/Status (based on the AGATA Hybrid Preamplifiers4 from A.Pullia).

One cable serves 6 segment preamplifiers (or 2 triple preamplifiers: e.g. preampA tied to segment 1 2 3, preampB tied to segments 4 5 6). The maximum lengh of the cable is 5 meters.

The signals coming out of the preamplifiers are read out through 26-way lvds cables with MDR (Mini Delta Ribbon) male connectors on either end. The cable has a "camera-link" format with 11 individually shielded twisted pairs (Pairs 1, 2, ..., 11) and 4 spare pins connected to the shielding (pins 1, 13, 14, and 26). The pin assignments are defined in Fig 10.

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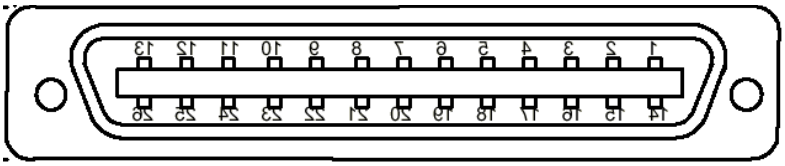

Fig 8 MDR26 Male connector

Preamp side	Digitiser side	Cable name	Preamp side	Digitiser side	Cable name	Preamp side	Digitiser side	Cable name	Preamp side	Digitiser side	Cable name
1	1	shield	17	10	pair 3+	8	19	pair 7-	24	3	pair 10+
14	14	shield	5	22	pair 4-	21	6	pair 7+	12	15	pair 11-
2	25	pair 1-	18	9	pair 4+	9	18	pair 8-	25	2	pair 11+
15	12	pair 1+	6	21	pair 5-	22	5	pair 8+	13	13	shield
3	24	pair 2-	19	8	pair 5+	10	17	pair 9-	26	26	shield
16	11	pair 2+	7	20	pair 6-	23	4	pair 9+			
4	23	pair 3-	20	7	pair 6+	11	16	pair 10-			

Fig 9 Pairs Pins association

Fig 10 The signals in the Segment cable.

Type	*Name*	*Source*	*Type/Format*	*Q.ty*	*Position*
Analog	**Segment**	**Preamp**	**Analog signal / 1 differential pair**	**6**	**Pairs 1 to 6***
Digital	**SHDN_A**	**Digitiser**	**Logic Level / +5.x V = High, GND = Low**	**1**	**Pair 7+**
	SHDN_B	**Digitiser**	**Logic Level / +5.x V = High, GND = Low**	**1**	**Pair 7-**
	Reserved	**-**	**For future expansion**	**1**	**Pair 9**
	Inh_A	**Preamp**	**Digital signal / +5.x V = High, GND = Low**	**1**	**Pair 10****
	Inh_B	**Preamp**	**Digital Signal / +5.x V = High, GND = Low**	**1**	**Pair 11*****
Power	**+5.x V**	**Preamp**	**Supply for Logic Isolators**	**1**	**Pair 8+**
	GND	**Preamp**	**Ground**	**1**	**Pair 8-**
	GND	**Preamp**	**Cable shields & Supply for Logic Isolators**	**4**	**pins 1,13,14,26**

* Pair i+ is positive swing, pair i- is negative swing, with i=1, 2,...,6

** Pair 10- swings dynamically, pair 10+ is tied to common ground, i.e. to pins 1,13,14,26

*** Pair 11+ swings dynamically, pair 11- is tied to common ground, i.e. to pins 1, 13,14,26

Signals Descriptions :

SHDN_A, and SHDN_B

Active High Logic Level.

Switch off the fast reset mechanism in triple preamplifiers A and B. If this is pulled up the fast reset mechanism will be permanently switched off. If this is pulled down the fast reset

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mechanism will automatically work in each of the six preamplifiers when needed. The analog levels for SHDN_A, SHDN_B are detector GND (low) and +5.x V (high) (coming with the cable). So these Power Supply voltages will be used on the isolator on the cable side..

INH_A, and INH_B

Active High (set dynamically by preamplifiers A and B)

This is a digital signal (TTL) that will be pulled up if any of the preamplifiers in triples A and B is undergoing a fast reset. It will be pulled down as soon as the fast reset is over. This can be used to inhibit acquisition of false events due to a reset transient. A source termination on the preamp side will be used. Please put no termination resistor on the receiver side to avoid half splitting of the TTL signal. The analog levels for InhibitAB are detector GND (low) and +5.x V (high) (coming with the cable). So these Power Supply voltages will be used on the isolator on the cable side

+5.x V

Power supply provided by the preamplifiers for the Logic isolators except for the core Inhibit. The actual value will range between +5 and +6 V.

-5.x V

Power supply provided by the core preamplifier for the Logic isolator for the core Inhibit. The actual value will range between -5 and -6 V.

GND

All grounds, including the internal shielding are to be connected at the preamplifier side and should not be connected to the digitiser's ground.

FUTURE UPGRADE

In a future version the spare twisted pairs could be used as a serial transmission link (lvds) from the receiver to the triples/core preamplifiers (using a microcontroller to receive and distribute the signals). This link could be used to set the P/Z fine adjustment of the triple/core preamplifiers.

IMPORTANT NOTES:

1) All detector GND's carried to the receiver along the cable must be connected at the receiver end to the cable shields found on pins 1, 13, 14 and 26 of the MDR connector.

2) All digital signals transmitted from the receiver to the detector should enter the cable through a source series termination resistor of 75 Ohms. Instead, no termination resistor should be put at the detector side to avoid half splitting of the TTL signal (with the possible exception of signal "Pulser In", which could be received through a 75 Ohm resistor and a Schmitt-Trigger comparator).

3) All Logic Levels (see column "Format" in Complete Signal List) should be bypassed to ground with 1uF capacitors either at the transmitter or at the receiver sides

e) Clock FADC

The global clock gives the time reference and is used to regenerate the clock for FADC. This clock must have the minimum jitter possible. The clock reference could either be direct or via the pre-processing card through the Virtex2pro from Monitoring board.

Actually the timing distribution is being developed….waiting for result

Fig 11 Clock Functional block diagram.

f) Spare analog channel.

The segment spare channel will not be connected directly to a fibre-optic link(only 6 fibres will be used), but will be routed by multiplexers in the serialiser FPGA such that any of the 6 ADCs can be replaced by the spare ADC channel just by changing a multiplexer setting, and enabling the correct input buffering to route the segment signal to the spare ADC. The use of the segment spare channel will therefore become invisible to the pre-processing.

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III-2-1-2 FADC Laser Interface

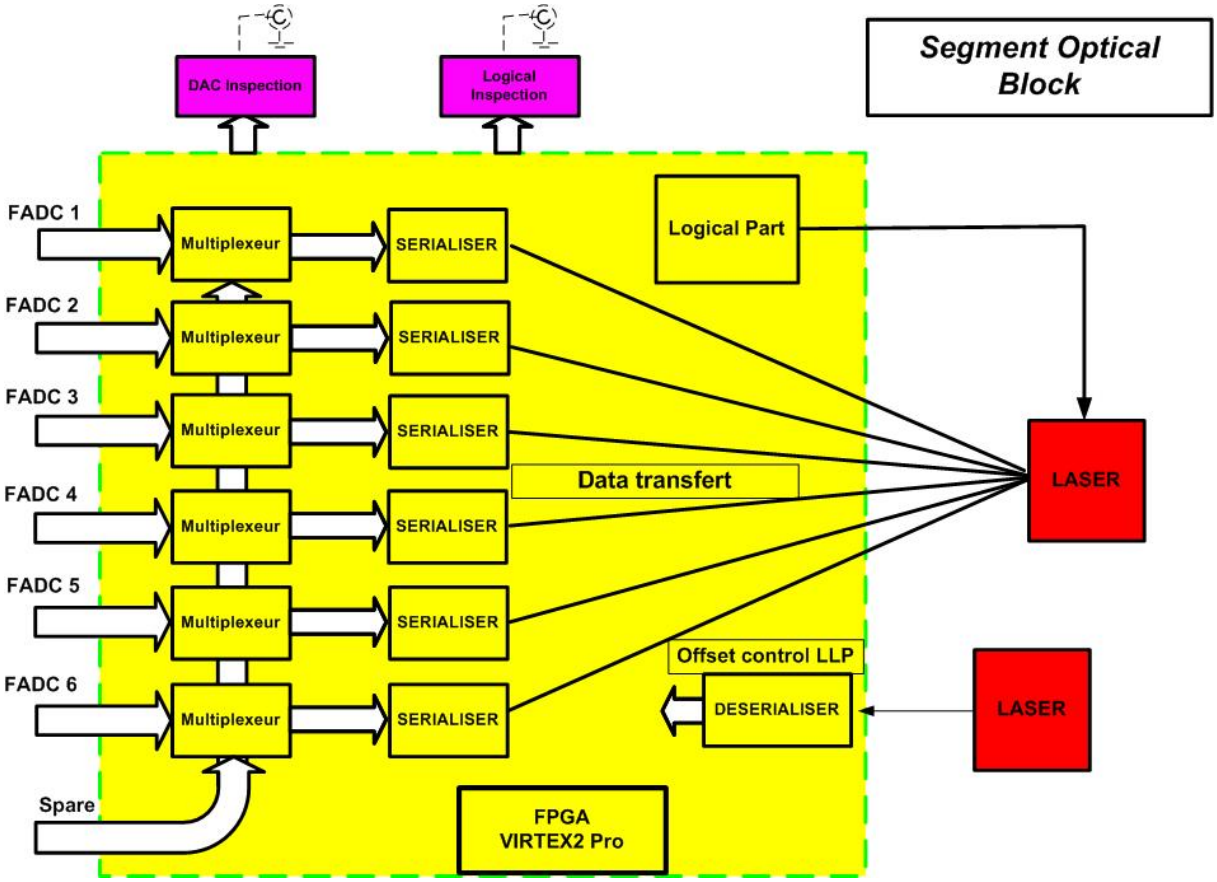

Fig 12 Diagram for segment input

a) Multiplexer

The multiplexer will be used to route the spare FADC output data if the spare ADC is used. The use of the segment spare channel will therefore become invisible to the pre-processing. **But it's very important than the gain of the spare analog chain is well defined for PSA to apply the good normalisation for the channel.**

b) Serialiser

The serialiser is needed to send the data to the optical interface. The Virtex2Pro has a specific hardware module dedicated to this function called ROCKET I/O. They have be designed to be compliant with the optical fibre interface devices. The data transfer rate will be 2 Gbit/s.

The Rocket I/O serialiser has a latency which changes each time the FPGA is power-cycled, or reset. To use all the channels in parallel we must be able to determine the latency of each of them. So a synchronisation protocol between the pre-processor and the digitizer must be defined.

The quality of the clock has a direct influence of the bit error rate of the serial link.

c) Global Clock.

The quality of the clock used in the serialisers has a direct influence on the bit error rate of the data link. The clock will come from the Core module after filtering and be distributed to all FADC cards by Coaxial cable.

d) DAC inspection lines.

A dual 14bitDAC (or 12 bits) two channels will be used to inspect signals after digitisation. This DAC can be disabled if not needed.

e) Logical inspections.

Two lines will be use for electronic workshop or debugging.

f) Laser interface.

To implement 2Gbit/sec the optical interface between the Digitiser Module and the Pre-processing Hardware a Parallel Fiber Optic Link Transmitter will be used.

The transmitter module converts parallel electrical input signals via a laser driver and a VCSEL array into parallel optical output signals at a wavelength of 850 nm.

The modules are pluggable, and are each fitted with an industry-standard 100pin MegArray socket for connection to the host board.

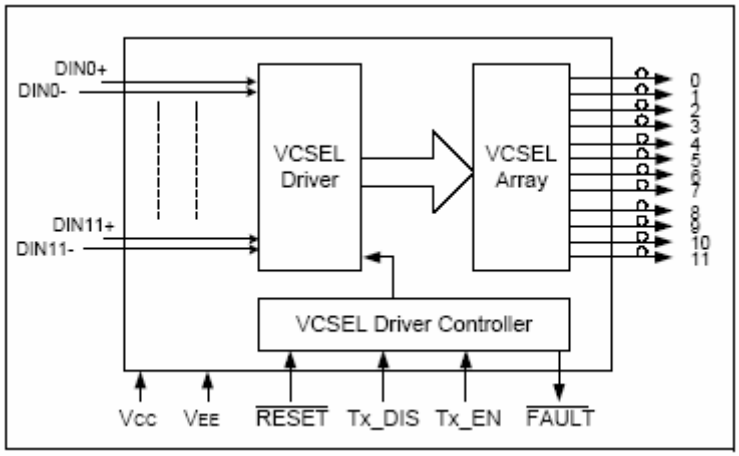

Fig 13 Transmitter block diagram.

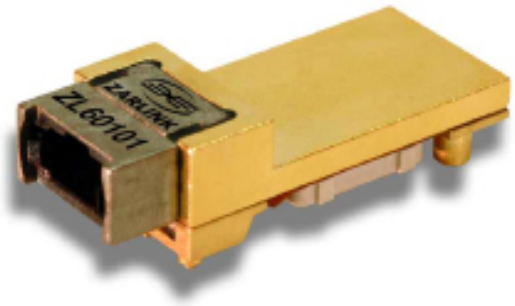

Fig 14 Transmitter ZL60101.

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g) Offset control LLP .

It was agreed that the offset will not be adjusted on a sample by sample basis. Instead a slow adjustment will be used at a rate such that it doesn't affect the MWD algorithm noticeably. The exact rate is to be determined after tests to see how fast we can adjust a baseline offset without affecting MWD.

Following a proposal from P.J.Coleman-Smith we have decided to use Agilent Fiber Optic Components from Agilent. The Application Note 1123 describes an inexpensive 20 to 160 MBd Fiber Optic Solution.

The communication protocol is not defined yet but it should not be complicated to implement.

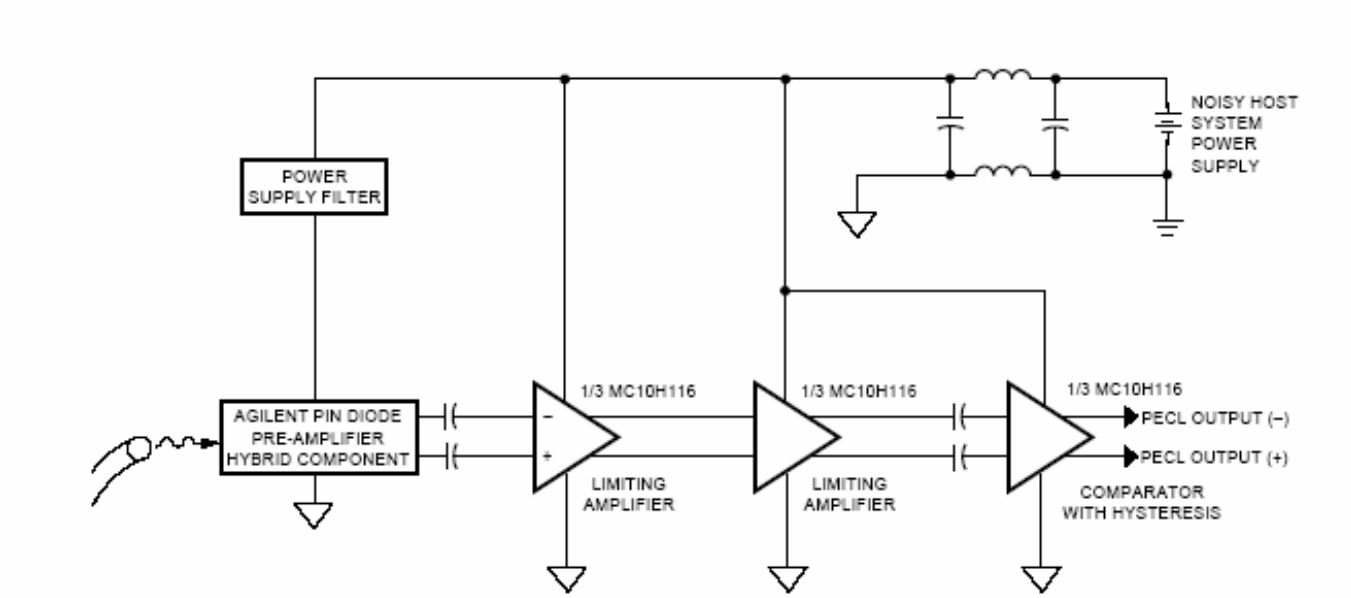

Fig 15 +5 V PECL _ compatible 160 MBD Fiber optic Receiver.

Because of the low data rate a deserialiser will be implemented in the Virtex2Pro.

h) Important note about use of the spare channel.

The use of the segment spare channel will become invisible to the pre-processing.

- But it's very important that the gain of the analog chain is well defined for PSA to apply good normalisation to the channel.

- The LLP offset adjustment is given for a specific preamplifier, if this segment is coded through the spare FADC the Virtex has to transfer the offset adjustment to the spare channel.

III-2-3 FADC CORE BLOCK

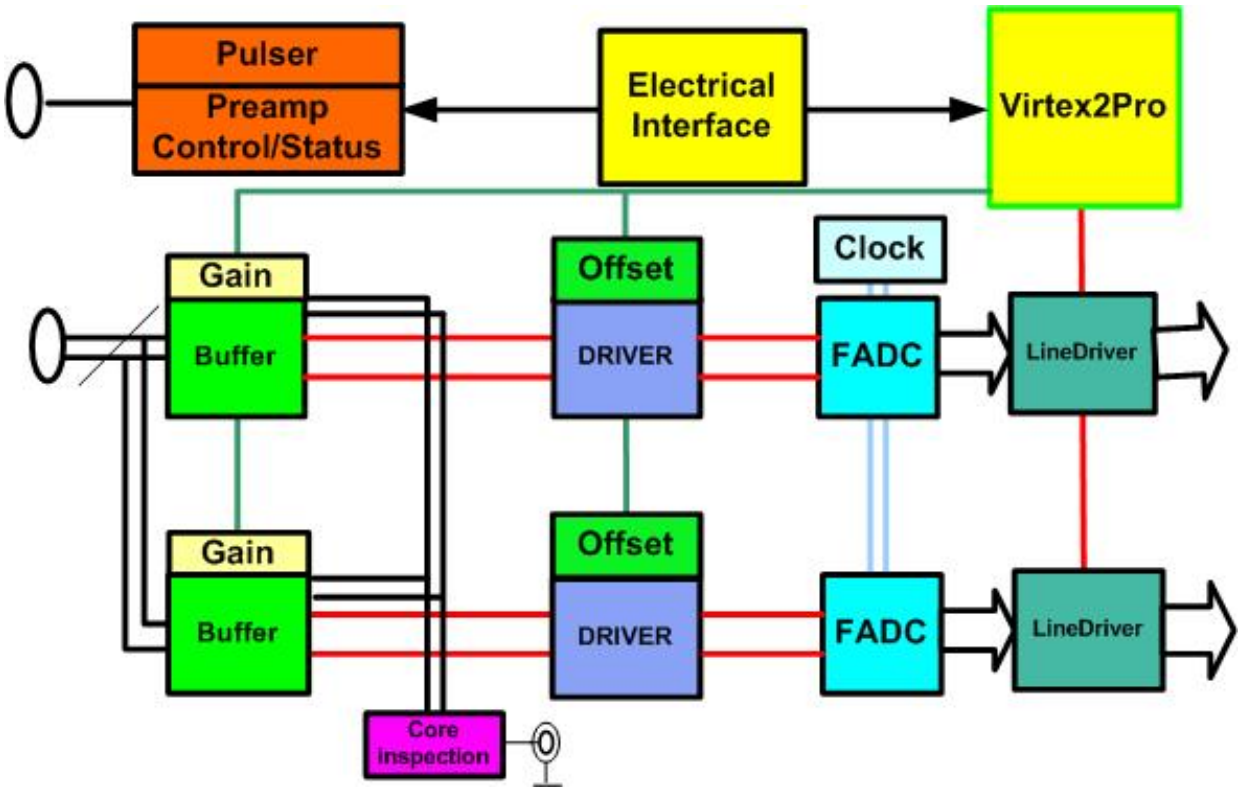

Fig 16_Diagram for Core input.

a) Buffer

The Buffer module provides impedance matching and routing of the input signals between the FADC, and inspection lines. The input signals are differential. The buffer module includes the range selector.

b) Offset

The offset value required will be dynamically calculated by the pre-processor or the digitiser to extend the ADC dynamic range.

c) Driver

The driver adds the offset signal. The anti-aliasing filter is included in the Driver before the FADC. All the offset DACs are based on the same chip: PCM56. We have a great deal of experience with the performance of this device. It has a low noise level, is bipolar and has a serial control interface. The output will be connected to two buffers one with a gain of one, and the other with a gain of -1. We'll used Texas ultra low noise buffer OPA692

d) FADC

The ADC must have 14 bits at 100 Mhz, 16 data bits are sent to the FPGA; bits 0 to 13 are data, bit 14 is the FADC overload and bit 15 could be used as a synchronization pulse. The overload bit could be also be transmitted to preamplifier for the pole zero reset through the FPGA. The ADC is the AD6645 100 Mhz from Analog Device.

e) Line Driver

It avoids capacitive loading of the data bus of the FADC, and allows the FADC data bus to be transmitted to the Laser Board.

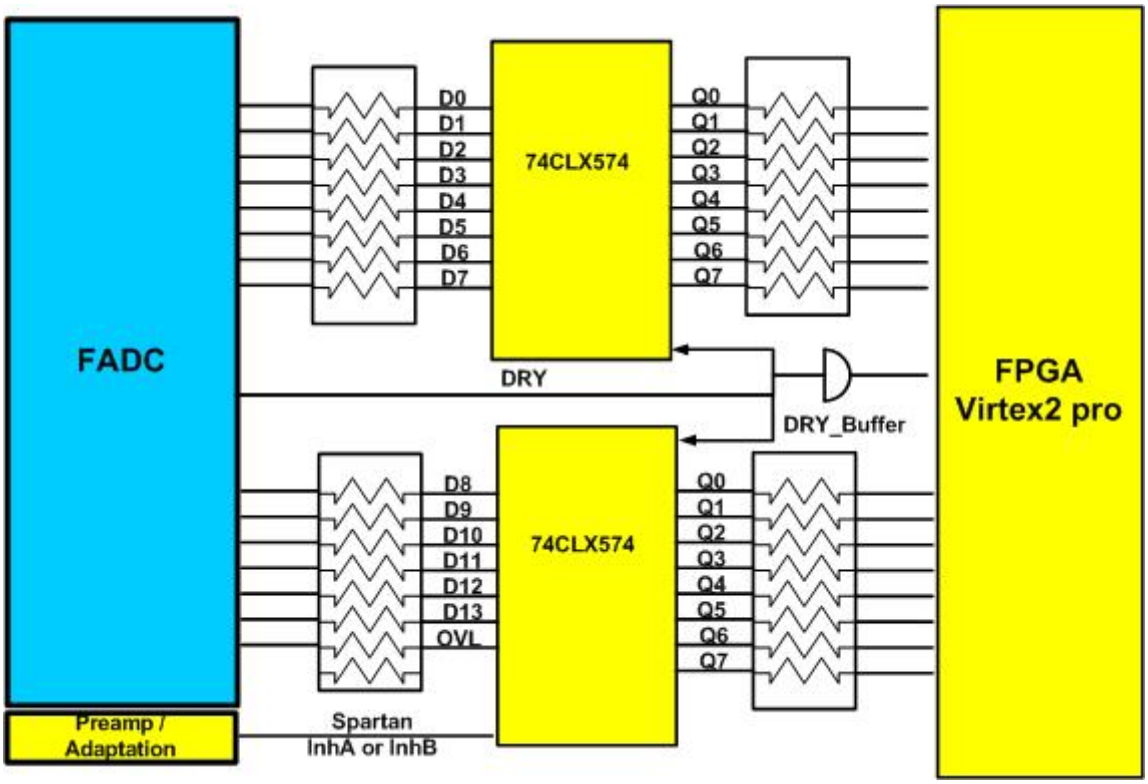

Fig 17 Core Buffer line.

f) Clock

The clock module receives the clock of the Global Clock and transmits it to the FADCs with minimal jitter.

g) Preamp Control / Status

This part implements the optical isolation between the Digitiser and the Preamplifier for control and status signals, and the Pulse module signals.

This documents has been written in collaboration by:
R.Baumann; P.J.Coleman-Smith; I.H.Lazarus; P.Medina; C.Santos; J.Thornill; D.Wells

III-2-3-1 FADC Core module details:

a) Buffer input and Inspection line

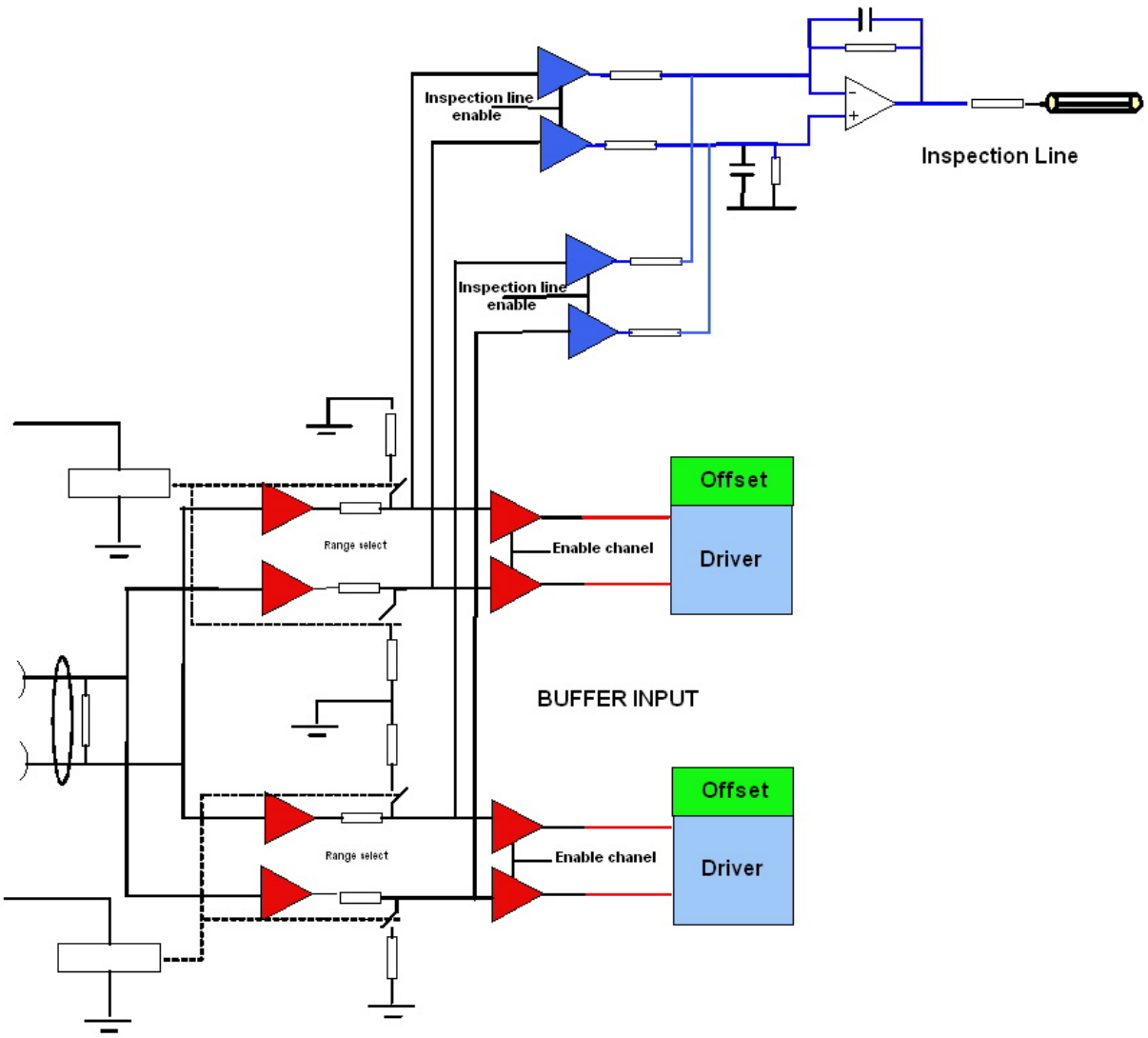

Fig 18 Core Buffer input.

For the buffer input we use OPA692 or OPA2692 (Dual OPA 692) from Texas with output disable, low noise level, and fixed gain.

If we need to check the signal through the inspection line the blue buffer will be enabled.

b) Range

It has been decided that the analog chain should be designed so as to guarantee the best energy resolution with the typical gain range selection (0-5 Mev), giving the user the option to attenuate the analog signal in front of the ADC so as to extend the range.

Normal Range: 0 – 5 Mev
Extended Range: 0 – 20 Mev

c) Driver / Offset

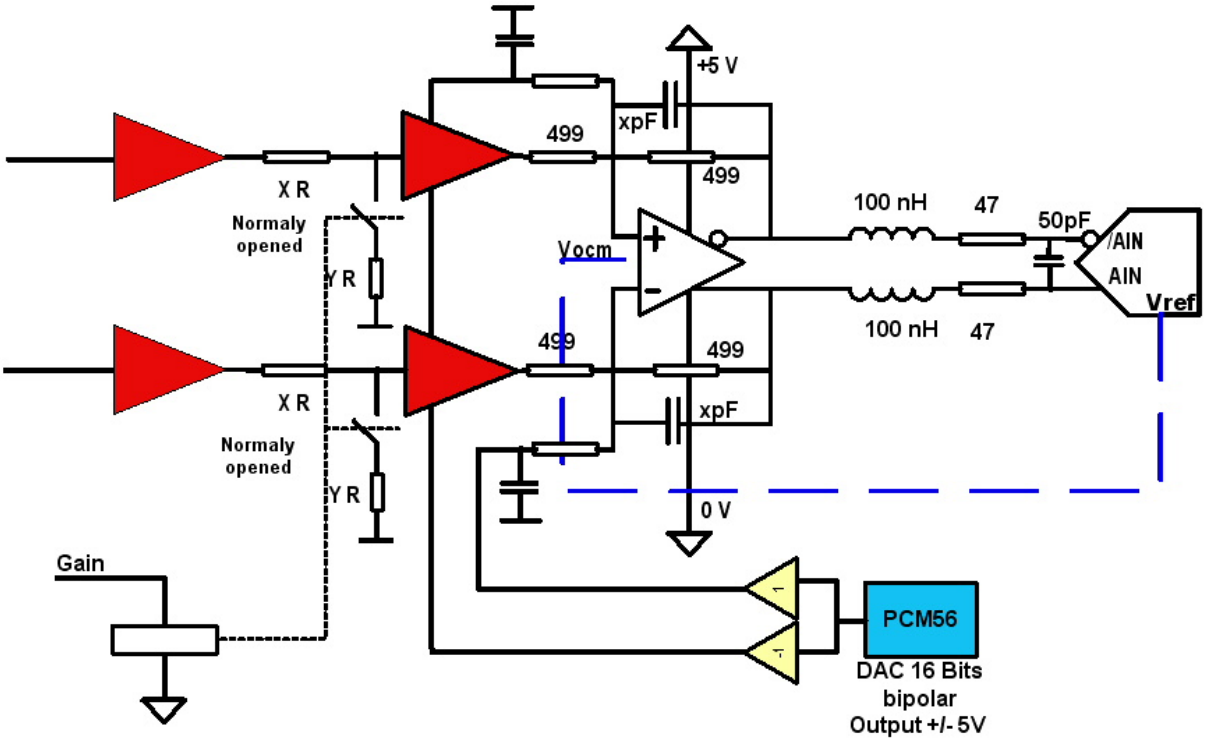

Fig 19 Driver / Offset

For the FADC driver we will use the AD8138 from Analog Device.
To maintain the advantage of the differential signal and after discussion with the Preamplifier Team we'll use the following devices:

_ First buffer could be AD8056 or OPA2692
_ The second stage could be the OPA 692.

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d) Preamp/Control Status and Pulse Generator Control. (based on the AGATA Hybrid Preamplifier 4 from A.Pullia).

One cable serves the core preamplifier and the pulse generator. The maximum length of the cable is 5 meters.

The signals coming out of the preamplifiers are read out through 26-way lvds cables with MDR (Mini Delta Ribbon) male connectors on either end. The cable has a "camera-link" format with 11 individually shielded twisted pairs (Pairs 1, 2, ..., 11) and 4 spare pins connected to the shielding (pins 1, 13, 14, and 26). The pin assignments are defined in Fig 21.

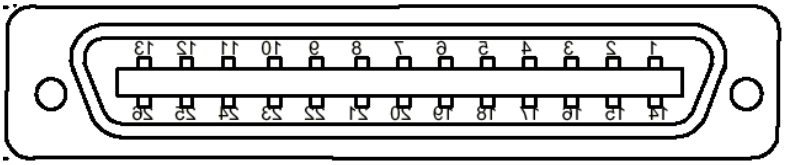

Fig 20 MDR26 Male connector

Preamp side	Digitiser side	Cable name	Preamp side	Digitiser side	Cable name	Preamp side	Digitiser side	Cable name	Preamp side	Digitiser side	Cable name
1	1	shield	17	10	pair 3+	8	19	pair 7-	24	3	pair 10+
14	14	shield	5	22	pair 4-	21	6	pair 7+	12	15	pair 11-
2	25	pair 1-	18	9	pair 4+	9	18	pair 8-	25	2	pair 11+
15	12	pair 1+	6	21	pair 5-	22	5	pair 8+	13	13	shield
3	24	pair 2-	19	8	pair 5+	10	17	pair 9-	26	26	shield
16	11	pair 2+	7	20	pair 6-	23	4	pair 9+			
4	23	pair 3-	20	7	pair 6+	11	16	pair 10-			

Fig 21 Pairs Pins association

Fig 22 The signals in the Core cable.

Type	*Name*	*Source*	*Type/Format*	*Q.ty*	*Position*
Analog	**Core**	**Preamp**	**Analog signal / 1 differential pair**	**1**	**Pair 1***
Digital	**AT10**	**Digitiser**	**Logic Level / +5.x V = High, GND = Low**	**1**	**Pair 2+**
	AT10	**Digitiser**	**Logic Level / +5.x V = High, GND = Low**	**1**	**Pair 2-**
	AT20	**Digitiser**	**Logic Level / +5.x V = High, GND = Low**	**1**	**Pair 3+**
	AT20	**Digitiser**	**Logic Level / +5.x V = High, GND = Low**	**1**	**Pair 3-**
	Clk	**Digitiser**	**Digital Signal / +5.x V = High, GND = Low**	**1**	**Pair 4+**
	MODE	**Digitiser**	**Logic Level / +5.x V = High, GND = Low**	**1**	**Pair 4-**
	DIN	**Digitiser**	**Digital Signal / +5.x V = High, GND = Low**	**1**	**Pair 5****
	/CS	**Digitiser**	**Digital Signal / +5.x V = High, GND = Low**	**1**	**Pair 6****
	SHDN_C	**Digitiser**	**Logic Level / GND= High, -5.x V = Low**	**1**	**Pair 7+**
	EN_PS	**Digitiser**	**Logic Level / +5.x V = High, GND = Low**	**1**	**Pair 7-**
	Pulser In	**Digitiser**	**Digital Signal / +5.x V = High, GND = Low**	**1**	**Pair 8****
	Reserved	**-**	**For future expansion**	**1**	**Pair 9**
	Inh_C	**Preamp**	**Digital Signal / GND = High, -5.x V = Low**	**1**	**Pair 10****
Power	**+5.x V**	**Preamp**	**Supply for Logic Isolators**	**1**	**Pair 11+**
	-5.x V	**Preamp**	**Supply for SHDN_C Isolator**	**1**	**Pair 11-**
	GND	**Preamp**	**Cable shields & Supply for Logic Isolators**	**4**	**Pins 1,13,14,26**

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R.Baumann; P.J.Coleman-Smith; I.H.Lazarus; P.Medina; C.Santos; J.Thornill; D.Wells

* Pair 1+ is positive swing, pair 1- is negative swing

** Pair i+ swings dynamically, pair i- is tied to common ground, i.e. to pins 1,13,14,26

Signal Descriptions :

AT10
Active High Logic Level.
Attenuates pulser amplitude by 10dB.
The analog levels for AT10 are detector GND (low) and +5.x V (high) (coming with the cable). These Power Supply voltages are used on the isolator on the cable side.

AT20
Active High Logic Level. Attenuates pulser amplitude by 20dB. The analog levels for AT10 are detector GND (low) and +5.x V (high) (coming with the cable). So please use such Power These Power Supply voltages are used on the isolator on the cable side.

Clk, DIN, /CS
Digital Signals (Clock, Data In, Chip Select) used to set the pulser fine gain.
These signals implement a simple, low-frequency, 3-wire interface through which the 16-bit input of DAC AD5541 from Analog Devices is supplied, which sets the fine gain of the pulser. The maximum clock frequency is 25MHz but it is advisable to use a substantially lower frequency (e.g. 1 MHz). The protocol of this interface can be found on the data sheet of AD5542. It is advisable to use only large numeric values (in the range from 50 to 100% of the full scale) for fine-gain corrections. Otherwise the long-term stability of the pulser could worsen significantly. Use instead AT10 and/or AT20 for coarse-gain setting. The analog levels for Clk, DIN, /CS are detector GND (low) and +5.x V (high) (coming with the cable). These Power Supply voltages are used on the isolator on the cable side.

MODE
Logic Level.
Selects the shape of built-in Pulser. If this is pulled up the built-in pulser provides a positive exponential decay. If this is pulled down the built-in pulser provides a square wave.
The analog levels for EN_PS are detector GND (low) and +5.x V (high) (coming with the cable). These Power Supply voltages are used on the isolator on the cable side.

SHDN_C
Active High Logic Level.
Switches off fast reset mechanism in the Core preamplifier.
If this is pulled up the fast reset mechanism will be permanently switched off. If this is pulled down the fast reset mechanism will automatically work when needed.
The analog levels for SHDN_C are -5.x V (low) (coming with the cable) and detector GND (high). These Power Supply voltages are used on the isolator on the cable side

EN_PS
Active High Logic Level. Switches on the Power Supply of built-in Pulser.
If this is pulled up the built-in pulser circuitry is biased. If this is pulled down the Pulser Power Supply is set to 0V. This permits to save power when the Pulser is not used. This

should not be handled dynamically by the Digitiser. The analog levels for EN_PS are detector GND (low) and +5.x V (high) (coming with the cable). So please use such Power Supply voltages on the isolator on the cable side. Use instead the receiver 0V 5V PS levels on the digitiser side.

Pulser In
Active High Digital Signal.
This is a digital signal (TTL) that will be pulled up to generate a positive transition of the pulser and down to reset it, or generate a negative transition edge (depending on setting of MODE). The analog levels for Pulser In are detector GND (low) and +5.x V (high) (coming with the cable). So please use such Power Supply voltages on the isolator on the cable side. Use instead the receiver 0V 5V PS levels on the receiver side.

Inh_C
Active High (set dynamically by core preamplifier)
This is a digital signal (TTL) that will be pulled up if the core amplifier is undergoing a fast reset. It will be pulled down as soon as the fast reset is over.
This can be used to inhibit acquisition of false events caused by a reset transient. A source termination on the preamp side will be used. Please put no termination resistor on the receiver side to avoid half splitting of the TTL signal.
The Analog levels for InhibitC are -5.x V (low) (coming with the cable) and detector GND (high). These Power Supply voltages are used on the isolator on the cable side. The isolator in this case works also as a voltage translator.
The width of this signal can be used to estimate the amplitude of the energetic event that caused the saturation. Hence this signal should be tied to a precise counter (with the highest possible clock frequency).

+5.x V
Power supply provided by the preamplifiers for the Logic isolators except for the core Inhibit. The actual value will range between +5 and +6 V.

-5.x V
Power supply provided by the core preamplifier for the Logic isolator for the core Inhibit. The actual value will range between -5 and -6 V.

GND
All grounds, including the internal shielding are to be connected at the preamplifier side and should not be connected to the digitiser's ground.

FUTURE UPGRADE
In a future version the spare twisted pairs could be used as a serial transmission link (lvds) from the receiver to the triples/core preamplifiers (using a microcontroller to receive and distribute the signals). This link could be used to set the P/Z fine adjustment of the triple/core preamplifiers.

IMPORTANT NOTES:
1) All detector GND's carried to the receiver along the cable must be connected at the receiver end to the cable shields found on pins 1, 13, 14 and 26 of the MDR connector.
2) All digital signals transmitted from the receiver to the detector should enter the cable through a source series termination resistor of 75 Ohms. Instead, no termination resistor

should be put at the detector side to avoid half splitting of the TTL signal (with the possible exception of signal "Pulser In", which could be received through a 75 Ohm resistor and a Schmitt-Trigger comparator).

3) All Logic Levels (see column "Format" in Complete Signal List) should be bypassed to ground with 1uF capacitors either at the transmitter or at the receiver sides.

e) Clock FADC.

The Global Clock gives the time reference and is used to regenerate the clock for FADC. The clock must have jitter as small as possible. The Core Laser Board sends the clock to the FADC Core Board. A clock driver is used for each FADC.

f) Spare analog channel.

There are two real independent channels in parallel. The LLP preprocessor will receive the two channels in parallel and have to make the choice between them. Digitiser is independent of this choice.

III-2-3-2 Laser Core module:

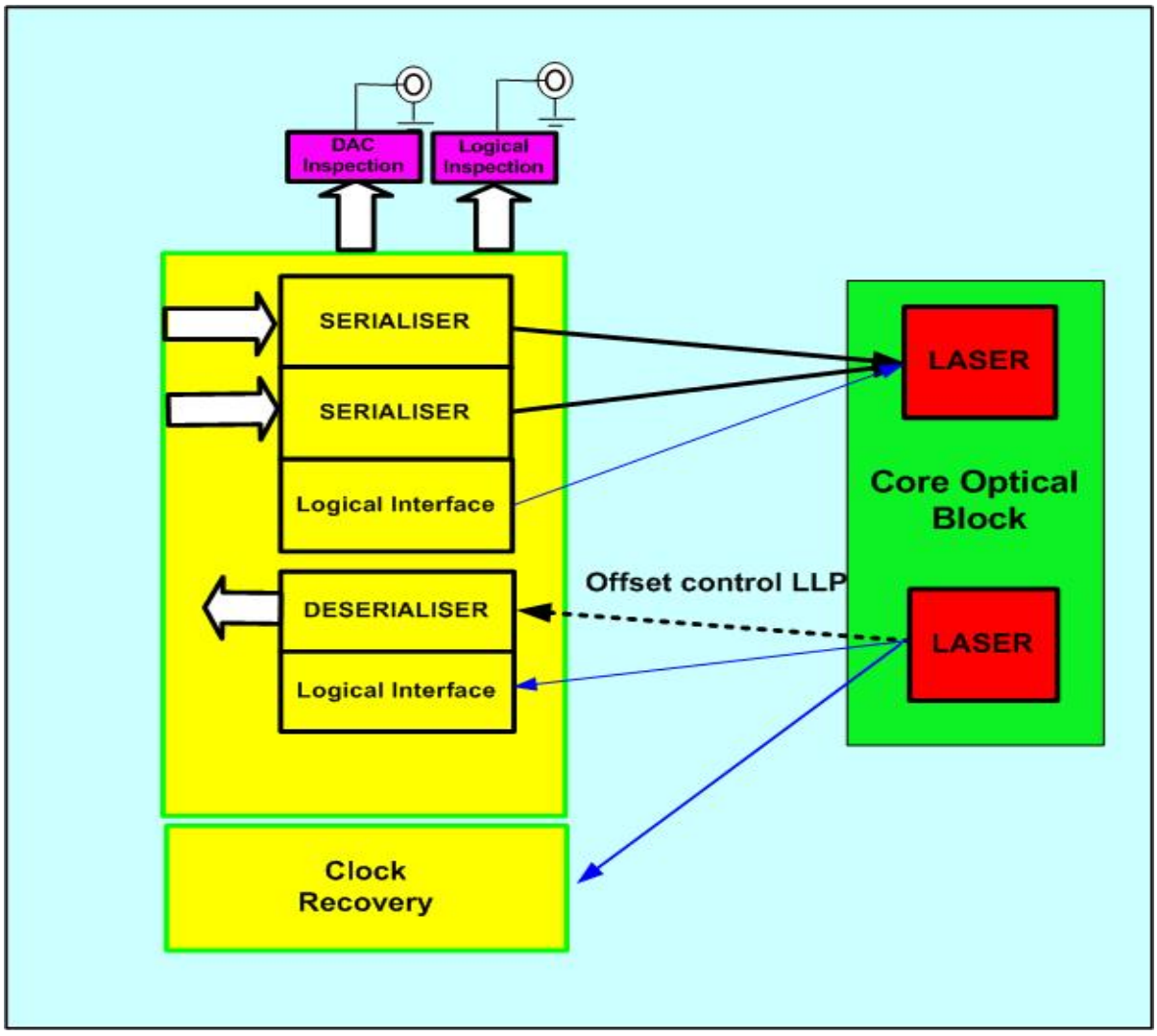

Fig 23 Diagram for core Laser.

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R.Baumann; P.J.Coleman-Smith; I.H.Lazarus; P.Medina; C.Santos; J.Thornill; D.Wells

a) Serialiser

The serialiser is needed to send the data to the optical interface. The Virtex2 Pro has a specific hardware module dedicated to this function called ROCKET I/O. They have been designed to be compliant with the optical fiber interface devices. The data rate transfer will be 2 Gbit/s.

The Rocket I/O serialiser has a latency which changes each time the FPGA is power-cycled or reset. To use all the channels in parallel we must be able to determine the latency of each of them. So a synchronisation protocol between the pre-processor and the digitizer must be defined.

The quality of the clock used in the serialisers has a direct influence of the bit error rate.

b) Laser Interface

To implement the optical interface between the Digitiser core Module and the Pre-processor a Parallel Fiber Optic Link Transceiver will be used.

The transmitter module converts parallel electrical input signals via a laser driver and a VCSEL array into parallel optical output signals at a wavelength of 850 nm. The modules are pluggable, and are each fitted with an industry-standard 100 pin MegArray socket for connection to the host.

The component the most suitable is the Vcsel Zarlink 4x4 Transceiver:

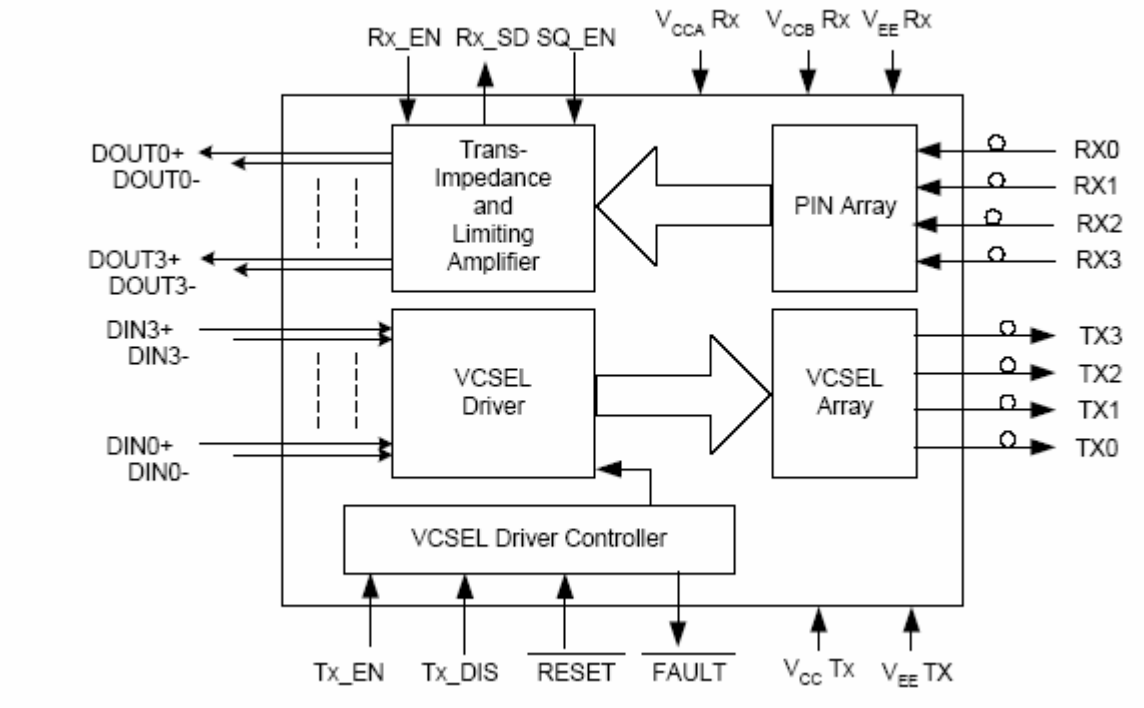


Fig 24 Transceiver block diagram

c) Clock recovery

This is one of the more fundamental parts of the Digitiser.

The clock is send to all FADCs on the digitiser board. For a good SNR with a high frequency signal input the clock must have the smallest jitter possible.

Waiting for tests signals

d) DAC Inspection.

Adual 14bit DAC (or 12 bit) will be used to inspect signals after digitisation. These DACs will be disabled if not needed.

e) Logical Inspection.

Two lines will be use for electronic workshop or debugging.

f) Offset control LLP.

It was agreed that the offset will not be adjusted on a sample by sample basis. Instead a slow adjustment will be used at a rate such that it doesn't noticeably affect the MWD algorithm. The exact rate is to be determined after tests to see how fast we can adjust a baseline offset without affecting MWD.

We will use a receiver line from the laser transceiver.

The communication protocol is not defined yet but it'll be not complicated to implement.

III-2-4 Control and Monitoring part : (J.Thornhill D.Wells)

The control and the monitoring must provide:

- The interface for debugging in an electronic workshop.
- The interface in the detector workshop for detector calibration.
- The interface in the experiment room for control and monitoring.
- The interface for software Virtex2 configuration.

The control and the monitoring interface must respect the Galvanic isolation from the other part of the apparatus.

It must be possible to modify and reload the configuration firmware for all components without opening and dismounting the mechanical housing to avoid complicated manipulation and the destruction of all thermal contacts.

a) On line slow control and monitoring.

In an experiment we need to use the slow control for :

- Spare channel control.
- Temperatures control.
- Channel control
- Etc …

An Ethernet connection has been chosen. Because is not necessary to have high data rate transmission a complete integrated solution have been chosen. The Xport system is the most compact, integrated solution available to web-enable any device with a serial interface.

Fig 25 Xport figure.

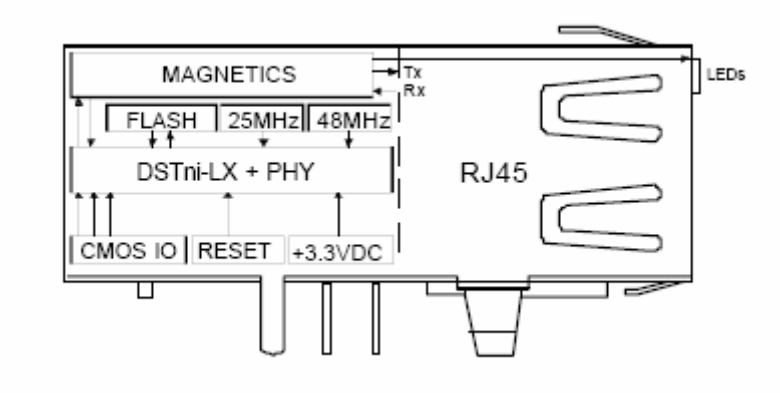


Fig 26 Xport block diagram.

The key features.

- The only device server in a RJ-45 form factor compact size.
- Complete integrated solution
- 10/100BASE-T Ethernet - Auto-Sensing
- EMI tested and compliant.
- 3,3 V power requirements
- Serial to Ethernet conversion.
-

Some tests have been done in Liverpool University show than this type of system work fine. The data rate measure was 200Kbits/s .

b) Debug slow control and monitoring in stand alone.

In electronic workshop or in detector laboratory it'll be important to have a global access to the digitiser with enough data rate.

c) JTAG Interface

To avoid mechanical dismounting of the Digitiser and be able to modify parameters and other points some JTAG interfaces will be mounted in the front panel. This JTAG interface will be used with the Chip Scope Debugger from Xilinx.

d) Virtex2 Loader

For easy debugging and to allow new firmware to be loaded into the Virtex2Pro in the Digitiser it has been decided that all Virtex2 Pro can be reconfigured through the slow control.

We can use the serial or parallel Select Mode Map, but Jtag configuration is also possible.

e) Digitiser Control bus Overview.

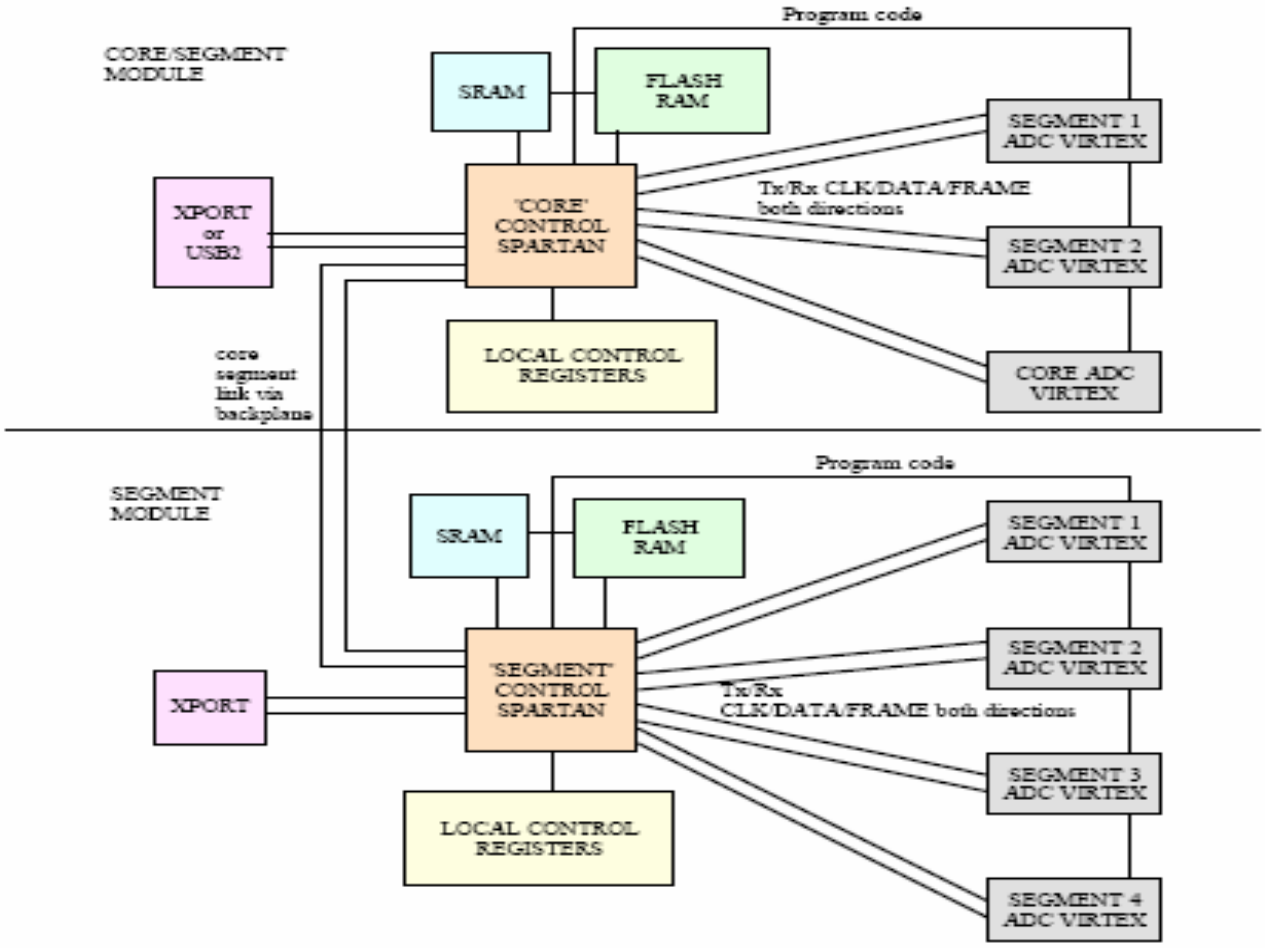


Fig 27 Link Diagram for Digitiser modules

The diagram above shows an overview of the communications within a single AGATA Digitiser box. The box consists of two Modules as follows:-

- Core/Segment Module which contains the Core electronics and the 2 cards with 7 segment channels per card (6+1 spare each card). This gives the Core and 12 usable Segment channels in this module.
- Segment Module which contains 4 PCBs each with 7 channels of segment ADC (6+1spare).This gives 24 usable Segment ADC channels. The communication between all the devices internal to each module and also between modules is serial with 5 wires in each direction. 2 differentials CLOCK,2 differential DATA and a single FRAME. Details of these are discussed later. The FRAME signal has two functions.

1) To show the start and end of a data transfer. Only data and clocks within a FRAME will be accepted.

2) To act as a handshake line from Rx to Tx during data transfers to prevent buffer overruns at the receiving end.

These features are discussed further in this document. All communication is done through the input XPORT device from the 10/100baseT Ethernet link. Neither module can initiate an Ethernet communication, they can only respond to an incoming request.

f) Digitiser Control and status data format.

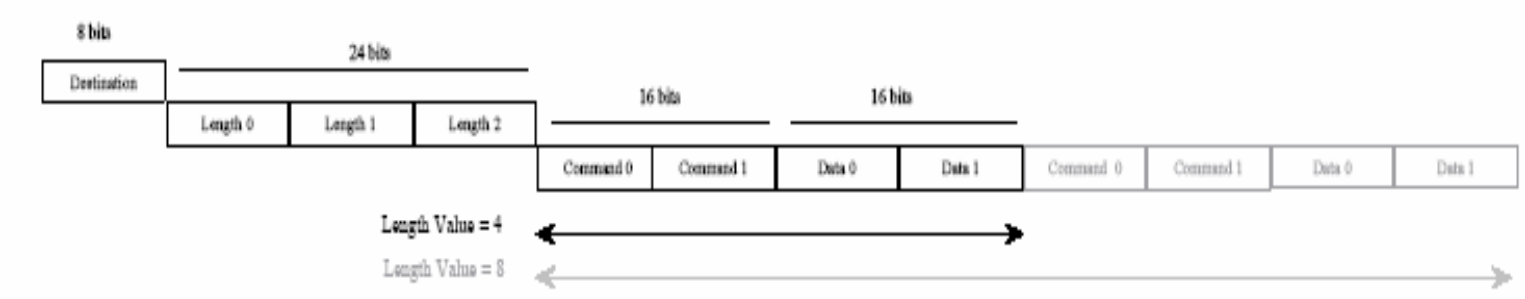
Basic command types

There are 3 allowed command types. These are:-

- *Simple Write* commands
- *Long Write* commands
- *Simple Read* commands

All commands operate on one module (either Core/segment module (module 1) or Segment only module (module 2)) at a time. i.e. Many simple commands can be sent as one command stream but they all must be for one of the 2 modules.
The Long Write command is used for loading the Virtex EEPROM device or may be used for similar future applications, e.g. lookup tables etc. within a Virtex device. By virtue of the Long Write command these cannot be concatenated.
The Simple Write commands are for setting individual registers for e.g. ADC enable, pulser values, gain range etc. commands can be concatenated within a module.
The Simple Read commands are single commands that request information from one of the modules. This may be temperature values, status or Virtex histogram data etc. These commands cannot be concatenated. The overall structure of the three command types is discussed below.

Command structure



The command structure shown above is a typical Simple Write command of one command (and showing how a second command would concatenate). All boundaries in the system are byte based. Breaking down the structure above we get:-

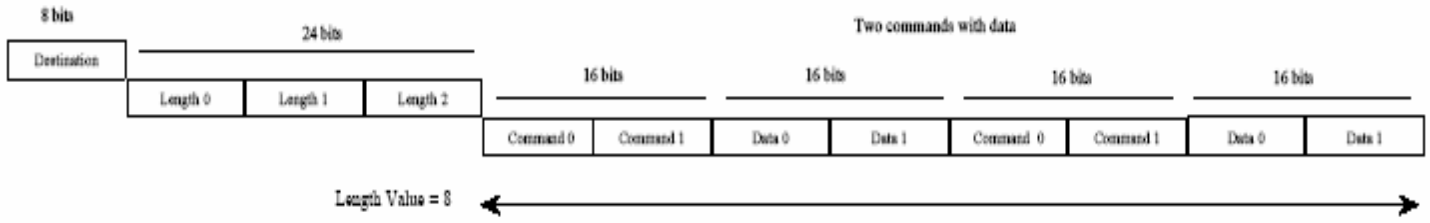
- Destination – This defines the Module (1 or 2) that the string is for. Whether it is a Read or Write command and, if it is a Write whether
it is a Simple or Long type. The set of bits that define this are shown later.
- Length defines the total number of bytes in the stream that follows the last Length byte. This is the same for all Write and Read commands. The length value must always be a multiple of 2 when a EEPROM data load is requested (internally data is treated as16 bits).
- Command 0 and Command 1 form the 16 bit command. The bits pre-defined in this are shown later. Some bits echo those found in the Destination byte.

- Data 0 and Data 1 form the 16 bit data value that relate to the command bytes.

NOTE :- In a Long Write command this will be a continuous byte data stream (Data 0……Data N). For a Long Write the numbers of bytes of data are defined by the value received in the length bytes minus 2 for the control bytes. This will be shown later.
In the next section all types of command will be shown.

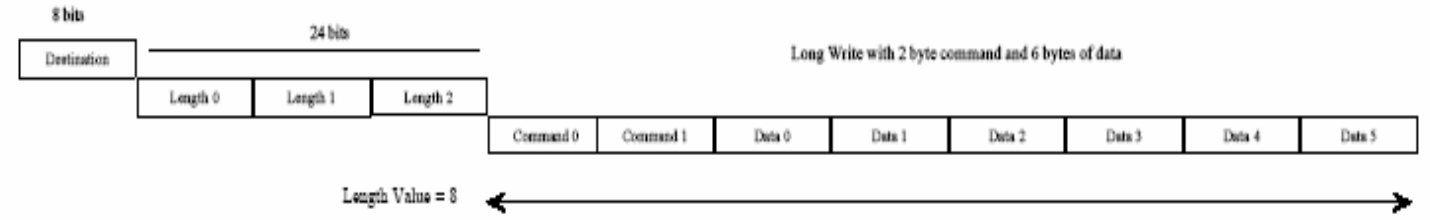
WRITE COMMANDS

Simple Write command



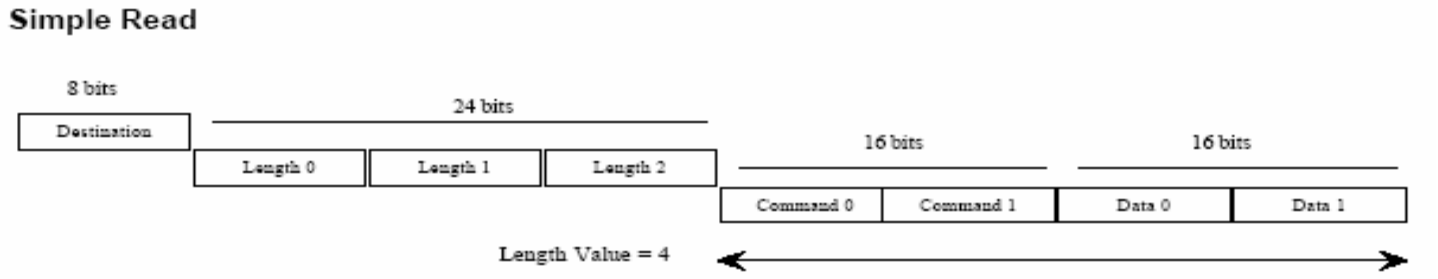
The Simple write command shown above will execute 2 commands. A command and associated data will always be 32 bits (as 4 bytes).

Long Write Command



The Long Write command shown above is an example containing one command and 6 bytes of data. Normally this command would be used for loading the EEPROM Virtex data and would be considerably longer than 8 bytes in length. Although not a current requirement, this type of command may also be used for loading lookup tables etc. into the Virtex devices, Control Spartans or similar.

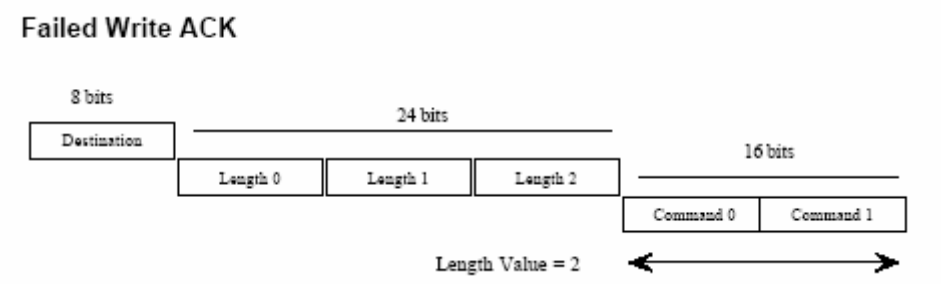
READ COMMAND



Read commands are only done singularly and are as shown above. The Command is again 16bits and defines the read destination, e.g. read Histogram when in test mode. The Data is normally zero but could be used as a means of transferring qualifier bits to the command. For example bits could be set to indicate which temperature sensors are to be read , which of two histograms should be read out or if a ADC scope trace was collected the length to be read. In normal experimental use the data bits are zero but they may be useful in the test modes.

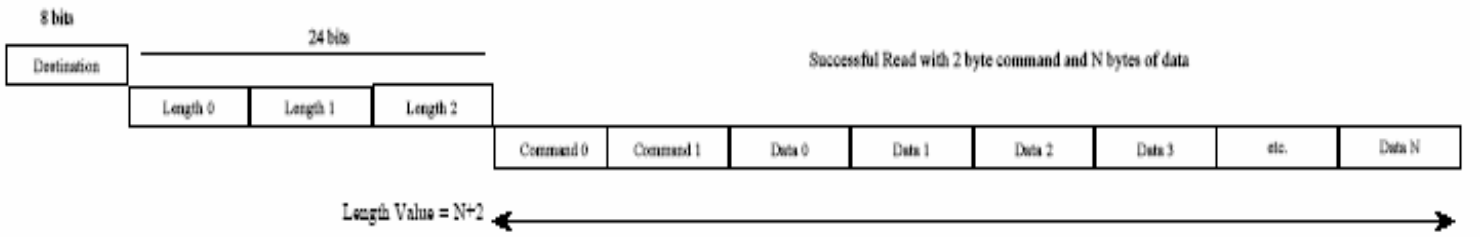
REPONSE TO COMMANDS

The Destination byte is the initial header sent from the controller echoed back unchanged. The Length value will be zero for a good Write sequence with no failures.



The Destination byte is the initial header sent from the controller echoed back unchanged. The Length value will be 2 for a failed Write with the Command on which the failure occurred in the Command 0 and Command 1 bytes. This will allow easy debugging of controller software.

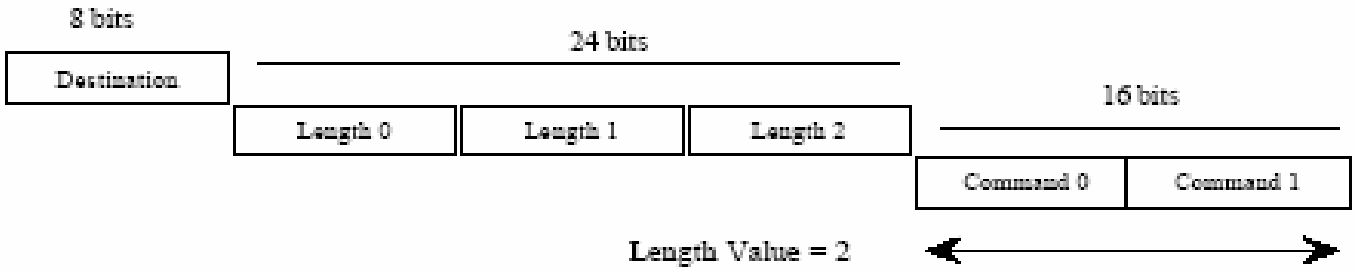
Successful Read ACK



When a successful read is done the controlling machine will receive the expected data stream it has requested in the following format.

Failed Read ACK

When a read fails the ACK sent back to the controlling machine is shown below.



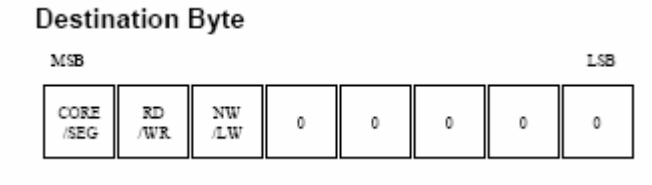
In this case the received stream is the same as that for a failed Write command. The Command bytes will show what the command was that was received by the Digitiser unit and will then have no data following.

NOTE:- It may be possible that data will be sent but due to an unexpected error occurring within the digitiser, the data is truncated before the full length is reached. This will force a timeout within the Digitiser unit and the unit will be ready for further commands approximately 30 seconds or less (to be determined) after the failure was detected. The controlling machine must be able to cope with this eventuality.

Format of Bytes within DATA Stream

To make the following easier to understand it is important to visualise the physical structure of the Digitiser unit.two modules, these are :-

- MODULE 1 = CORE channels with 12(+2) SEGMENT channels. (This is designated as the *CORE MODULE*).
- MODULE 2 = 24(+4) SEGMENT ONLY channels. (This is designated as the *SEGMENT MODULE*).

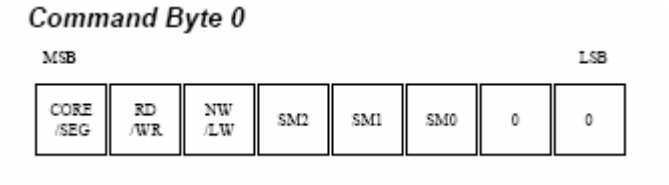


Bit 7 (MSB) selects the *physical Digitiser module* either the Core (=0) or Segment (=1) module as the destination for the command(s).
Bit 6 indicates if the command stream is a Read or Write. (Read =1, Write =0)
Bit 5 indicates that if a Write stream if a Simple Write or a Long Write. (Normal Write = 0, Long Write =1)
Bits 4 to 0 These are set to 0 (reserved for future use).

Length Bytes

Length 0 LSByte
Length 1 ---
Length 2 MSByte
These contain a 24 bit binary number which indicates the length of the following data stream.

Command bytes



There are 6 bits used within this command byte. The top 3 bits echo exactly those of the Destination byte at the start of the data stream. The next 3 bits labelled SM0, SM1 and SM2 are address bits to indicate the destination within the module of the following command and data. These bits are designated as follows:-

CORE

SM2	SM1	SM0	Destination Item
0	0	0	Virtex for Segment ADC card 1
0	0	1	Virtex for Segment ADC card 2
0	1	0	Virtex for Core ADCs
0	1	1	Main board
1	0	0	reserved
1	0	1	reserved
1	1	0	reserved
1	1	1	reserved

SEGMENT

SM2	SM1	SM0	Destination Item
0	0	0	Virtex for segment ADC card 1
0	0	1	Virtex for Segment ADC card 2
0	1	0	Virtex for Segment ADC card 3
0	1	1	Virtex for Segment ADC card 4
1	0	0	Main Board
1	0	1	reserved
1	1	0	reserved
1	1	1	reserved

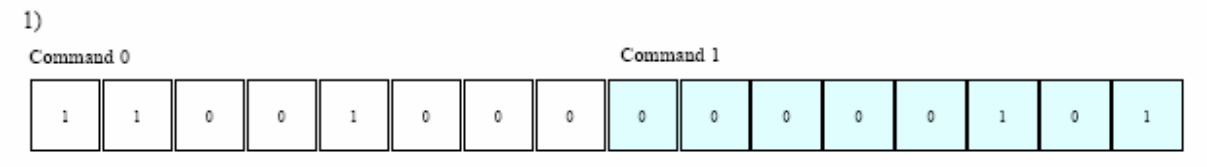
Core is selected when MSB=0 Segment is selected when MSB=1. True for both read and write operations.

The final 2 bits in the Command 0 byte are reserved and set to zero.

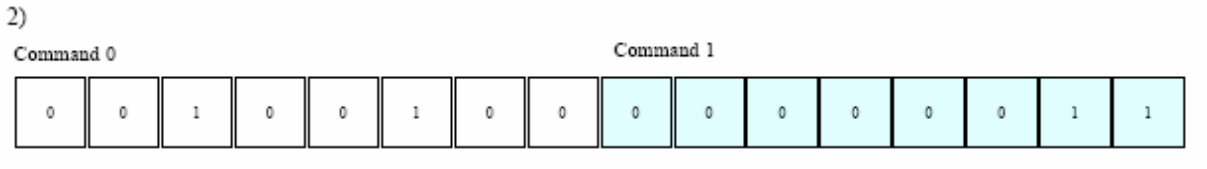
Command Byte 1

This byte contains the address within the destination item indicated by Command byte 0. These addresses (or commands) can be anything that the designer of the destination item requires. The full 8 bits are available giving 256 addresses (or commands) for any item.

Examples of commands are shown below.



This is a Read Command to act on the Segment module. The final destination is the *Virtex for ADC Card 3*. The command to be done within this Virtex device is hex 5.



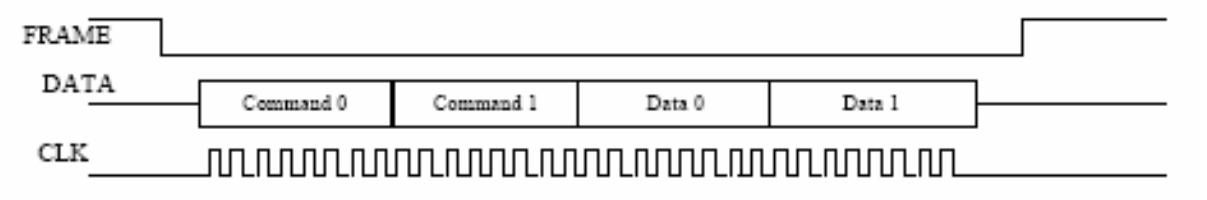
This is a Long Write to the Core module. The final destination is the *Virtex for Segment ADC Card 2*. The address or command to be executed within the Virtex device is hex 3.

Time out on failures.

If an error occurs within any of the state machines within a Control Spartan or Virtex device a watchdog timer will force a Reset. This will take approximately 30 seconds (*subject to review*) to be detected to cover the longest possible internal response time. External controllers must also have a timeout in order to detect any failure within them. The Unit will be ready for a new command after the 30 second period and be fully reset. (Please section later on '*Timeout Reset'*).

Data interface between Control Spartan and the VIRTEX devices.

The Control Spartan device within the Digitiser module will deal with commands on a one by one basis. This is to simplify the code within the Spartan and make the structure more sensible. Each command will be sent to the appropriate Virtex device together with its Data.
In order to appreciate the commands and command structure, some basic concepts about the workings of the serial link between the Spartan and Virtex are required.
The diagram below shows how the FRAME, DATA and CLOCK signals are used for a Simple Write or Read command from the Spartan to the Virtex. The FRAME signal determines the completion of the command transfer. (In the case of a Long Write this may span many hundreds of Data Bytes.) (Note FRAME is active Low)

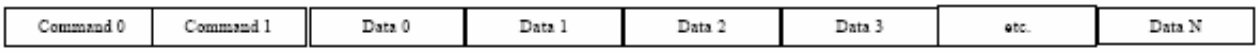


The FRAME signal is monitored to detect the start and end of the command being issued. Only single commands will be received by the Virtex. All Virtex command strings will start with two bytes of Command followed by two bytes of Data, (a total of 32 bits). This is expanded on for the Long Write command and is shown below. If the Virtex fails to recognise the Read or Write command it must issue an error message. This is shown in the ACK section below.

Write Commands.

A total of four bytes (32 bits) will be received for a normal Single Write Command thus:-

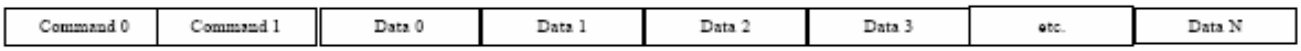
If a Long Write is to be done to a Virtex device then this will take the form:-



It should be noted that a handshake mechanism is in place so that the data stream can be suspended at any byte boundary to allow for processing of the data in the Virtex. (This is true in both directions, Read and Write). It may be necessary to use this to halt data transmission after the first 2 data bytes are received (to produce an initial format similar to Simple Write above) in order to set up the correct data path within the Virtex for the Long Write command. This is similar to RTS/CTS handshaking in RS232.The operation of this handshake is described in the *Electrical specifications and timing* section.

Read Command

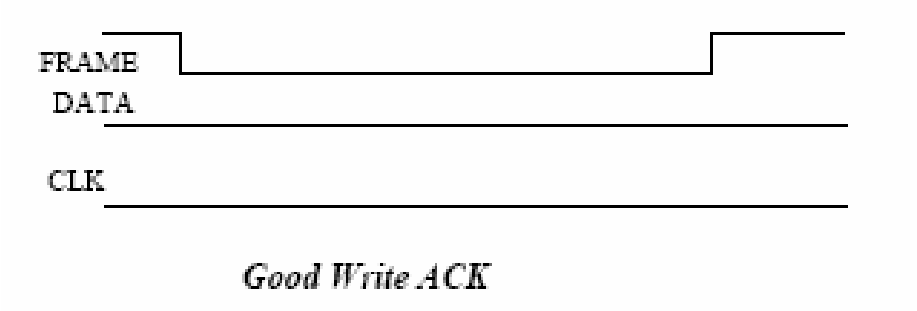
Data read from a Virtex device will take the form:-



Note that the read command is echoed at the start of the data stream.

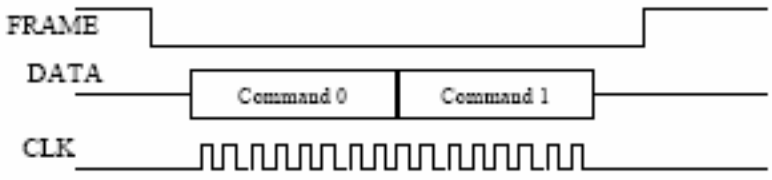
ACK signals from the Virtex to Spartan.

By using the ACK signal it is possible to acknowledge a good Write command without sending any Data or Clocks. The ACK command reply MUST follow the end of the FRAME received from the Spartan and not before. Please see *Electrical specifications and timing* section. The ACK should take the form shown here:-



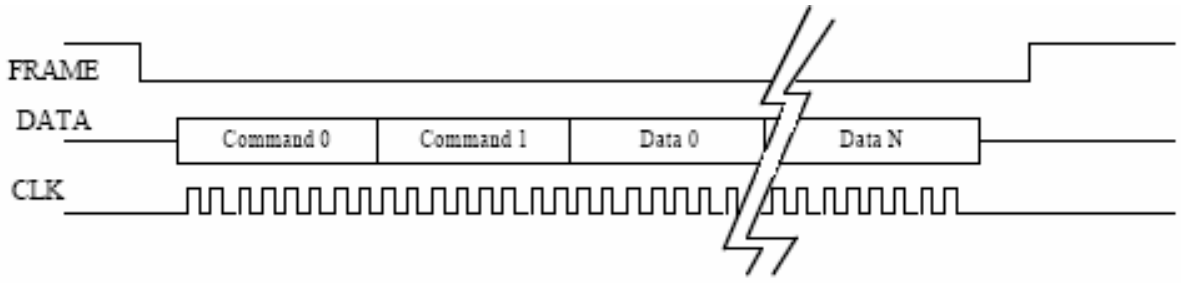
Good Write ACK

Timing is discussed in the *Electrical specifications and timing* section.
If a Read or Write command FAILS for any reason within the Virtex (e.g. not understood, not available etc.) then the following is used as the ACK signal from the Virtex. The Command is echoed back as a debug for the system and will be returned to the original Controlling source PC.



FAILED Read or Write ACK

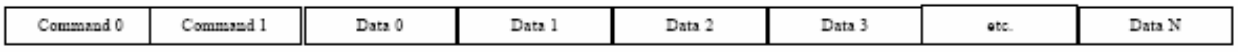
A good Read response from the Virtex to the Spartan is as shown here:-



GOOD data read from Virtex implicitly indicates good Read ACK.

The ACK in this case is the correct data being transmitted as expected.

The Data stream is in the following form, and is the same format as would be received in a Long Write.

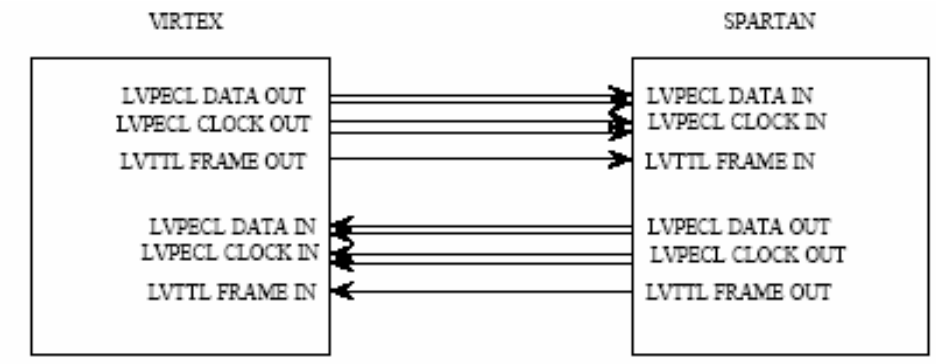


Electrical Specifications and Timing.

This electrical specification is specifically intended to be used between the Spartan and Virtex devices. It equally applies between the Core and Segment Spartans.
There are 5 wires connected in each direction between each Virtex and Spartan. These wires are as follows:-

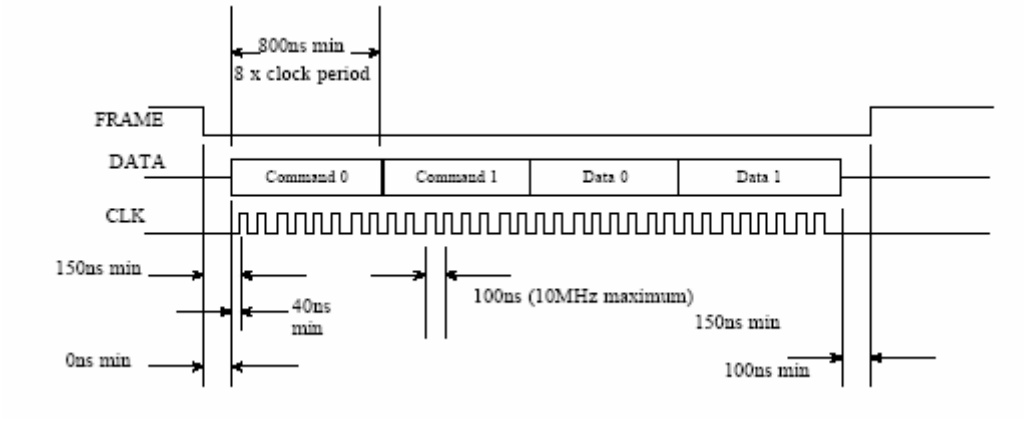
- DATA high – LVPECL
- DATA low – LVPECL
- CLOCK high – LVPECL
- CLOCK low – LVPECL
- FRAME – LVTTL (Active Low)

The CLOCK and DATA lines are complimentary
Differential Low Voltage Positive ECL (LVPECL) , whereas the FRAME signal is Single ended Low Voltage TTL (LVTTL). Only the FRAME is active Low.
The FRAME line controls the data transfer and has two functions depending on where it occurs within a transfer cycle. Primarily the FRAME line is used to instigate a Data transfer. It goes true to start the transfer, remains true during the transfer and goes false at the termination of the transfer. This indicates to the receiving device that it has received the entire data stream. The data transmission is complete and the receiving device can now process the data etc.. Data and clock should not be presented or accepted if the FRAME signal is not true.
In this instance TRUE is active LOW and FALSE is active HIGH with a pull-up on the FRAME input line for any non connected signals. In order to allow for the eventuality that the receiving end is unable to accept further data, the FRAME signal in the *return direction* acts in a similar fashion to an RS232 RTS/CTS status line. This, importantly, occurs during the transfer time only (when the forward direction FRAME signal is true). This means that any transfers can be temporally suspended until the receiving device can again accept them. The timing for this is shown later.



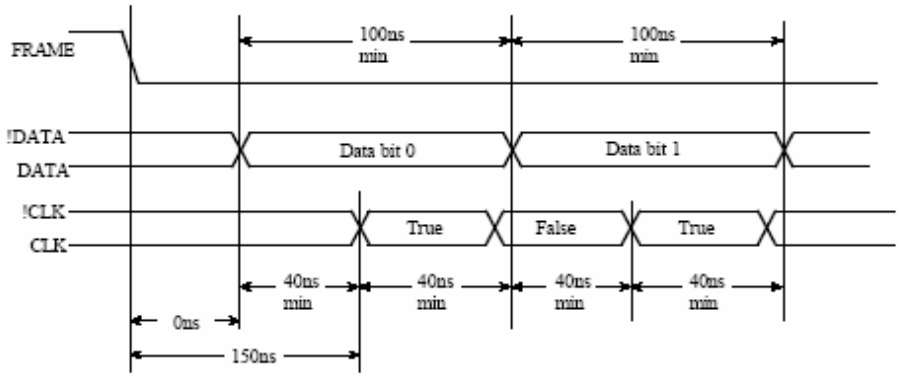
This documents has been written in collaboration by:
R.Baumann; P.J.Coleman-Smith; I.H.Lazarus; P.Medina; C.Santos; J.Thornill; D.Wells

Basic Frame Data Transfer Timing.

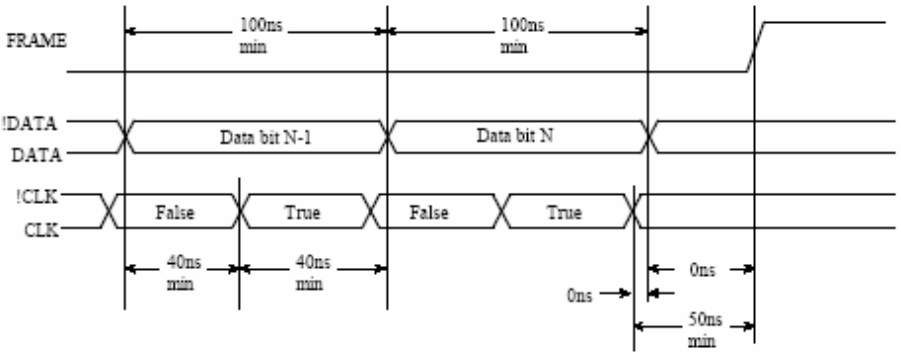


The above diagram shows the typical timing between the Virtex and Spartan in either direction. The Maximum permissible Clock rate is 10MHz and the FRAME, DATA and CLOCK edges should be programmed to have slow slew. The times shown above are assuming a maximum clock speed. Please note that it is possible to have gaps between bytes sent from the transmitting end, however it is anticipated that data will normally be continuous. The clock rate is determined by the source of the transfer up to a maximum of 10MHz. All DATA and CLOCKs are contained within the FRAME.

Timing diagram of start of data transfer. (Transmit end)



Timing diagram of end of data transfer. (Transmit end)



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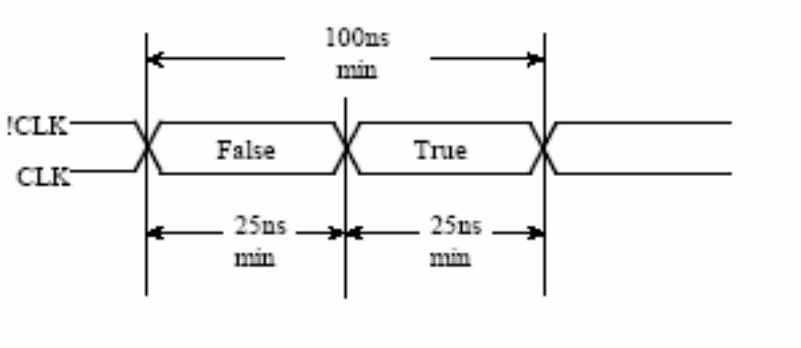
R.Baumann; P.J.Coleman-Smith; I.H.Lazarus; P.Medina; C.Santos; J.Thornill; D.Wells

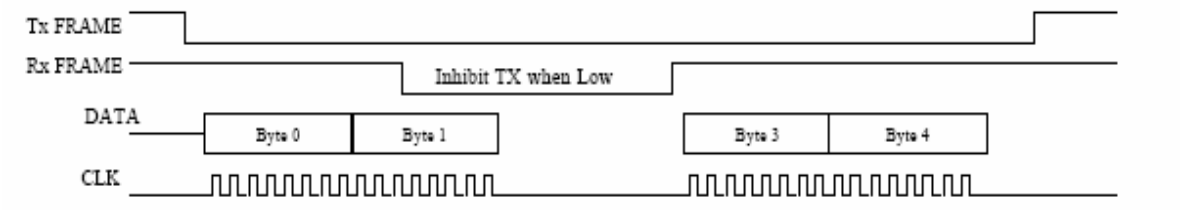
Clock Timing.

The Maximum permissible clock speed is 10MHz . There is no lower limit but a rate of 100kHz would seem reasonable to maintain transfer rate times. The Clock does not need to be a 50% mark space ratio as long as it complies with the timing below:-

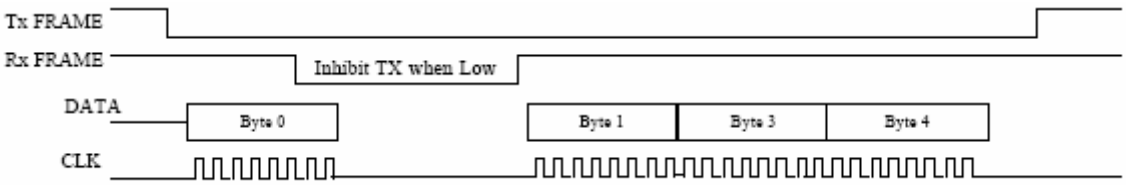


Handshaking

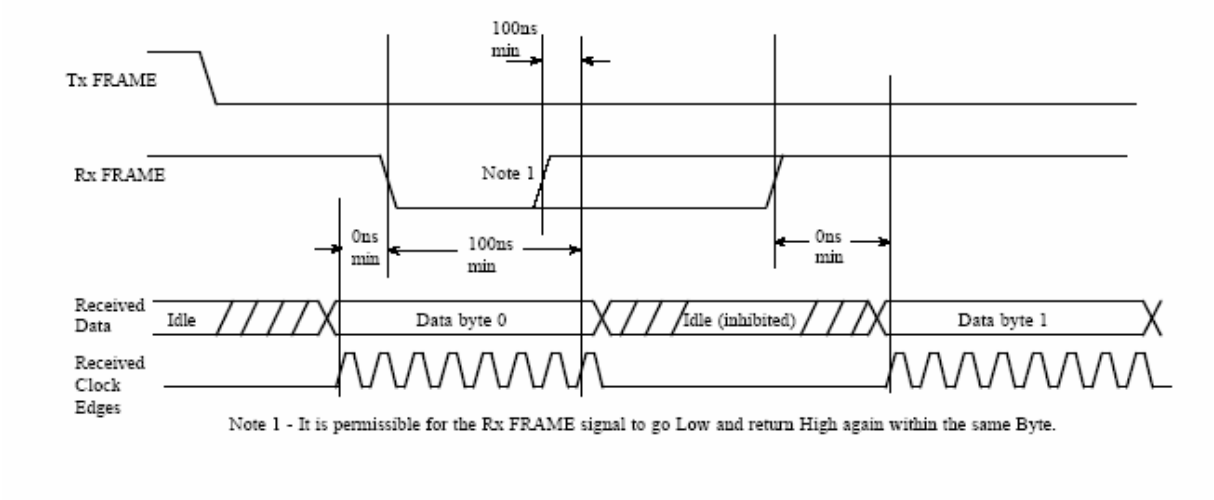
During long data transfers it may be necessary to interrupt the reception of data until space is available in a buffer at the receiver end for example. To facilitate this a method of handshaking using the receiver FRAME output signal has been included.



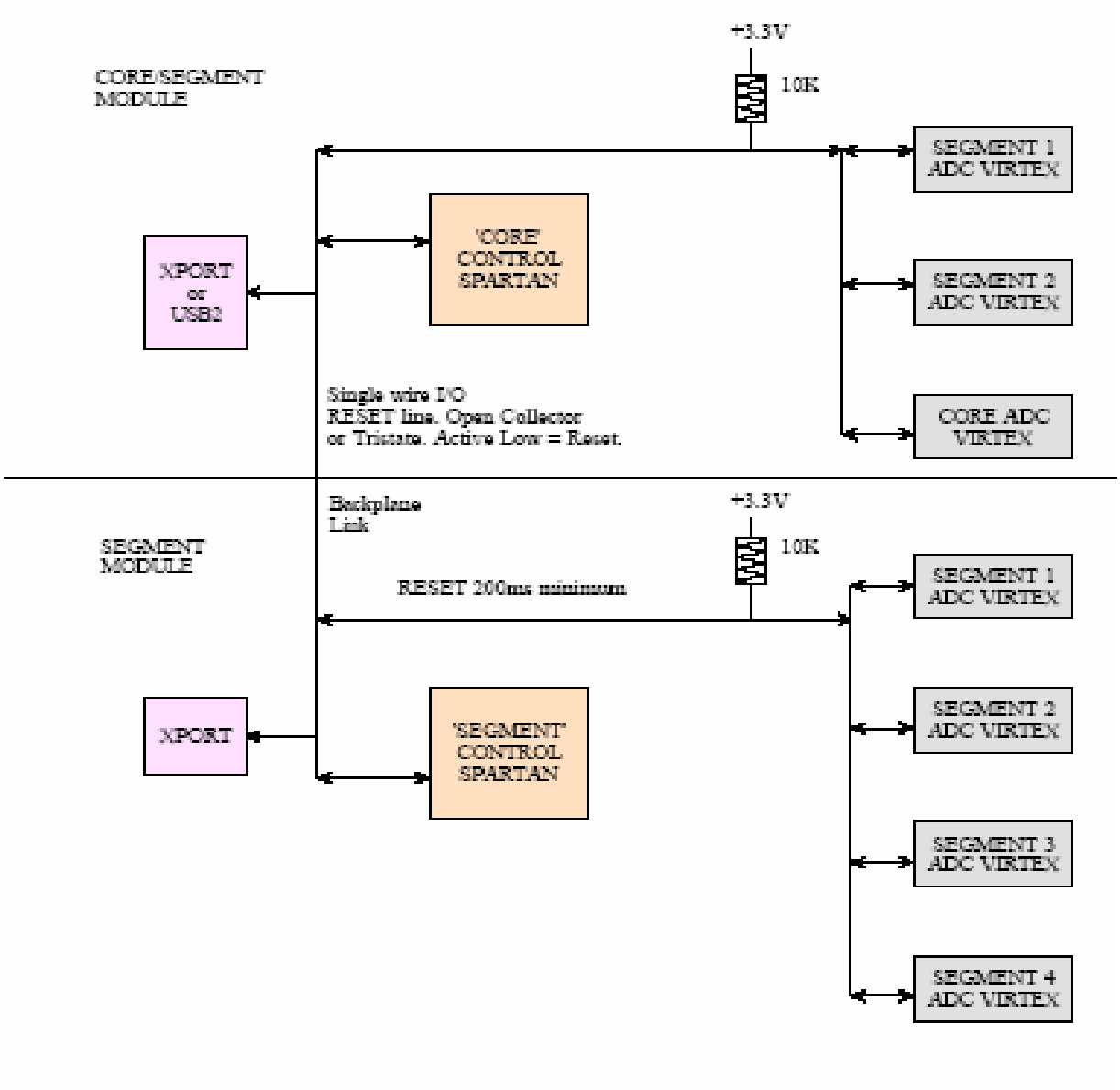
In the above diagram the Tx FRAME signal is generated from the transmitting end together with DATA and CLOCK. When the Rx FRAME signal is detected *LOW* the next DATA word transmission is inhibited until the Rx FRAME returns *HIGH*. The Rx FRAME only inhibits the transfer of complete data bytes and must be asserted during the time of the byte previous to that which is to be inhibited from transmission. It is important to note that the Rx FRAME signal can only operate in this way when the Tx FRAME is asserted *LOW*. Rx FRAME has a different function outside of this time. (See *ACK signals from the Virtex to Spartan* above).
A second example is shown below:-



The timing diagram below (based on the diagram above) shows the relationship of the clock edges to the FRAME signals.



Timeout Reset



This documents has been written in collaboration by:
R.Baumann; P.J.Coleman-Smith; I.H.Lazarus; P.Medina; C.Santos; J.Thornill; D.Wells

What follows is a new concept within the Digitiser and is required to ensure that the unit can recover from any fault conditions without user intervention.

The diagram above shows a common wire that runs between all the Virtex, Spartan and XPORT devices in a Digitiser box. This line is a LVTTL open collector (or tri-state) signal with pull-up resistors in both Segment and Core modules. Any device, be it Virtex or Spartan, can initiate an I/O reset by pulling this line low. In order to reset the XPORT devices the reset must be at least 200ms long. It is envisaged that a timer will be placed on this line to stretch the reset pulse time to this minimum value.
The I/O Reset line must be monitored by all the devices that can drive it and they must respond to a reset input by completely resetting the control bus input/output circuits within themselves. Registers containing downloaded values and settings that have been previously configured will be unchanged. Only the I/O interface for the control bus is to be reset. This is to ensure that should a device hang up mid operation for any unknown reason, the Digitiser can detect this and reset itself so that normal communication and control can be resumed.

IV. INTEGRATION

The integration has to provide solutions to several complicated problems.

It must:

- Allow the Digitiser to be mounted less than 5 meters from the Preamplifier.
- Allow dismounting of the electronics at the same time as the detector.
- Allow for Test, Debug and Maintainability of the electronic part.
- Allow cooling for maximum power dissipation estimated at 400 W.
- Allow testing the channel gain in stand alone mode in the detector workshop.
- Allow a stable temperature for the analog electronic part.

IV-1 System description.

a) The global system from the Preamplifier to the LLP hardware.

The global system is designed in multiples of 6 channels. The Digitiser has to comply with this integration.

The digitiser must be easily dismounted and remounted from the apparatus at the same time as the detector.

The power dissipation requires liquid cooling of the digitiser electronics module. To achieve an acceptable operating temperature more than one cooling plate must be installed to allow a compact mechanical housing. (Some thermal tests have been done at Ires to show this requirement).

A proposal from Liverpool University has been accepted.

The Digitiser will be divided:

- **One Module called CORE MODULE with:**
  - DC supply input and Local Power supply
  - Core FADC and Laser Interface.
  - 2 Boards of 6 channels each Segment FADC and Laser Interface
  - Master Control & Monitoring.
- **One Module called SEGMENT MODULE with:**
  - 4 Boards of 6 channels Segment FADC and Laser Interface.
  - Control & Monitoring.
  - Local Power supply
- **The Mechanical Housing:**
  - Input for water cooling.
  - Back plane PCB for communication between boards.

b) Proposal for the System Integration for AGATA Digitiser units from J.Thornhill

The problems to be overcome:

- The electronics boards must be in close contact with the cool walls of their mounting boxes. The temperature of PCB components must be stable at temperature equilibrium.
- The boxes must be cooled to near room temperature but not to the dew point to avoid condensation.
- It is necessary to connect the Core (top) ADC module to each of the Segment ADC modules below. This connection should be as reliable as possible and should not use ribbon cable. (Segment to segment also possible).
- The electronics modules should be easily removable for maintenance.
- There should be minimal need to interrupt the coolant supply in order to remove electronics modules.

Proposed solution to the above problems:

The diagrams which follow will detail the solution to all of these problems and will also give other advantages in terms of build, maintenance and manufacturability. Taking the section through an electronics module as a starting point, see figure 1 below, we can see that the ideal place to remove heat from the circuit components is through the top and bottom faces of the electronics box. The cooled metal plates will extract the heat through conduction directly from the hot components. It does not rely on conduction through the circuit board nor

air circulation. The PCB with components facing the case wall acts as an excellent screen between the two PCBs, an added advantage.

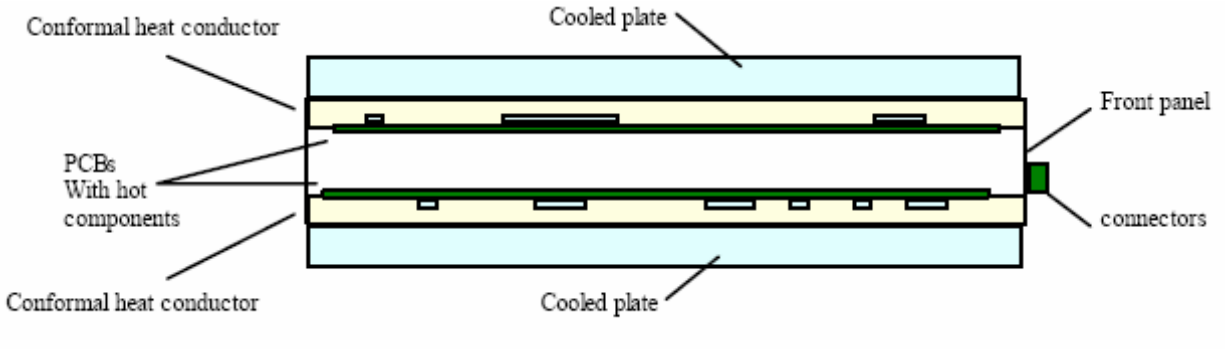
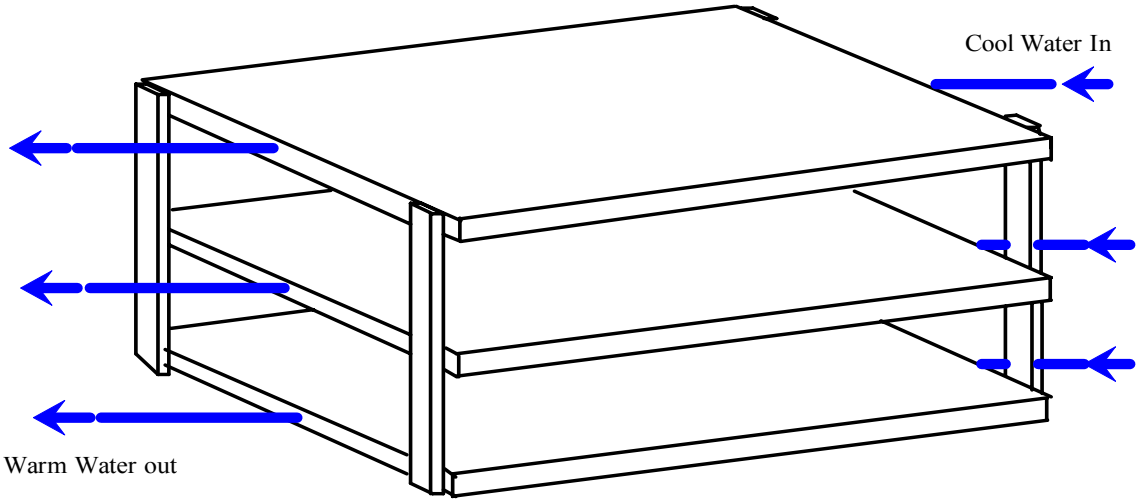


Fig 28 Section through typical electronics module.

Suppose now that the cooled plates are to be cooled using water. It is obviously undesirable to have to disconnect a water supply in order to maintain the electronics. I would therefore propose that the water cooled plates are placed in a 'rack' arrangement to create a water jacket around each electronics module. Furthermore, the electronics modules are connected together using a custom 'back plane' arrangement, which itself can easily be removed from the frame for replacement without disconnecting any water supply. Please see figures 27



Overview of main structure which takes 2 electronics modules (Core and segment modules - (1+12) and (24) = 37 channels). Each electronic module can be removed from this frame without having to disturb the water supply, reducing attendant risks.

.

Fig 29 Overview of main structure which takes 2 electronics modules.

The electronics modules would slide into the rack from the front face and engage with a suitable connector at the rear. This connector would carry differential point to point control and timing signals, control signals, grounds and power supply connections as required. High quality, high frequency connectors should be used and these. Connections within modules are done using internal connectors. The High accuracy 100MHz clock signals will be made externally using SMA connections and short coaxial links to each FADC card.

Good thermal contact to the plates of the cooling block and easy module insertion and extraction is a pre-requisite of the mechanical design. The top and bottom plates will be pulled onto the module external surface by spring tension spread over the outside of the box. It is envisaged that a lever and plate mechanism will be provided to open up the space between the top and centre (or bottom and centre) cooling plates for the removal of a module. This is currently under investigation.

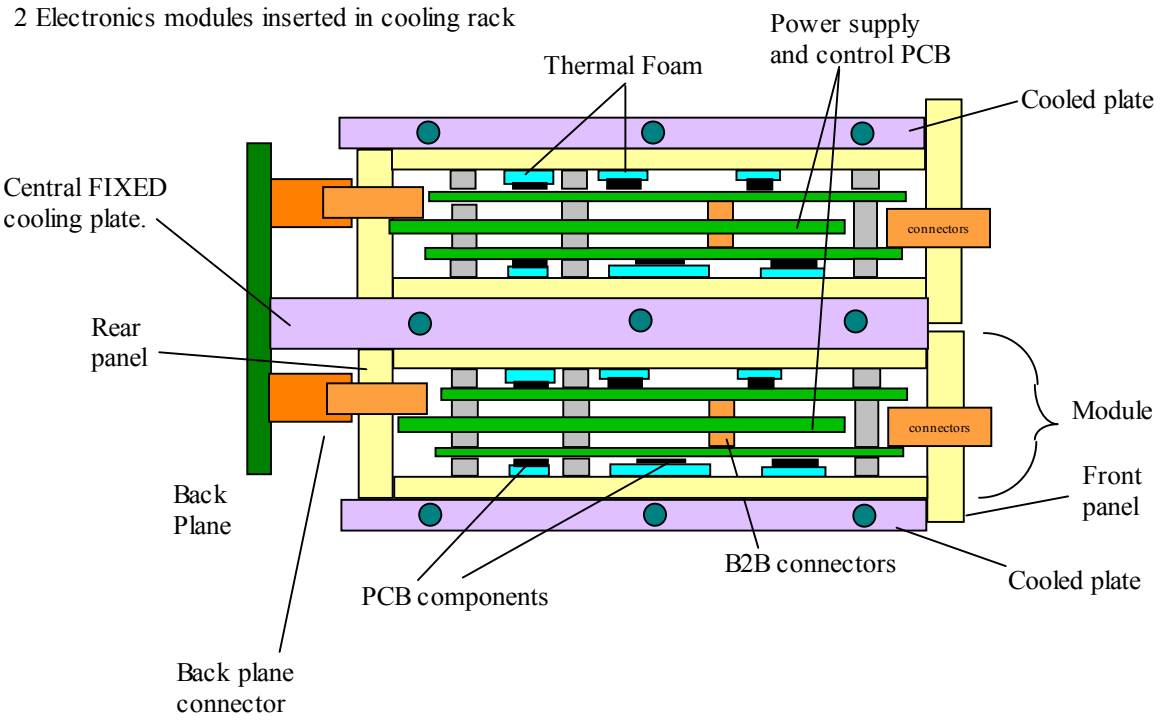


Fig 30 Section through electronics module after insertion in cooling rack.

The modules as shown are rectangular in section and are thus cheap to produce and work with. It should be noted, however, that each module is presently 450mm x 300mm x 30mm. A box containing 2 such modules is likely to be 500mm x 350mm x 160mm. This serves one detector of 37 channels.

Analogue signals enter to the Right Hand side of each module and Digital data (LASER) signals exit from the Left Hand side. Fig 4 shows this. This aids the smooth signal flow from in to out and there are no internal connectors in the analogue to LASER signal path.

This documents has been written in collaboration by:
R.Baumann; P.J.Coleman-Smith; I.H.Lazarus; P.Medina; C.Santos; J.Thornill; D.Wells

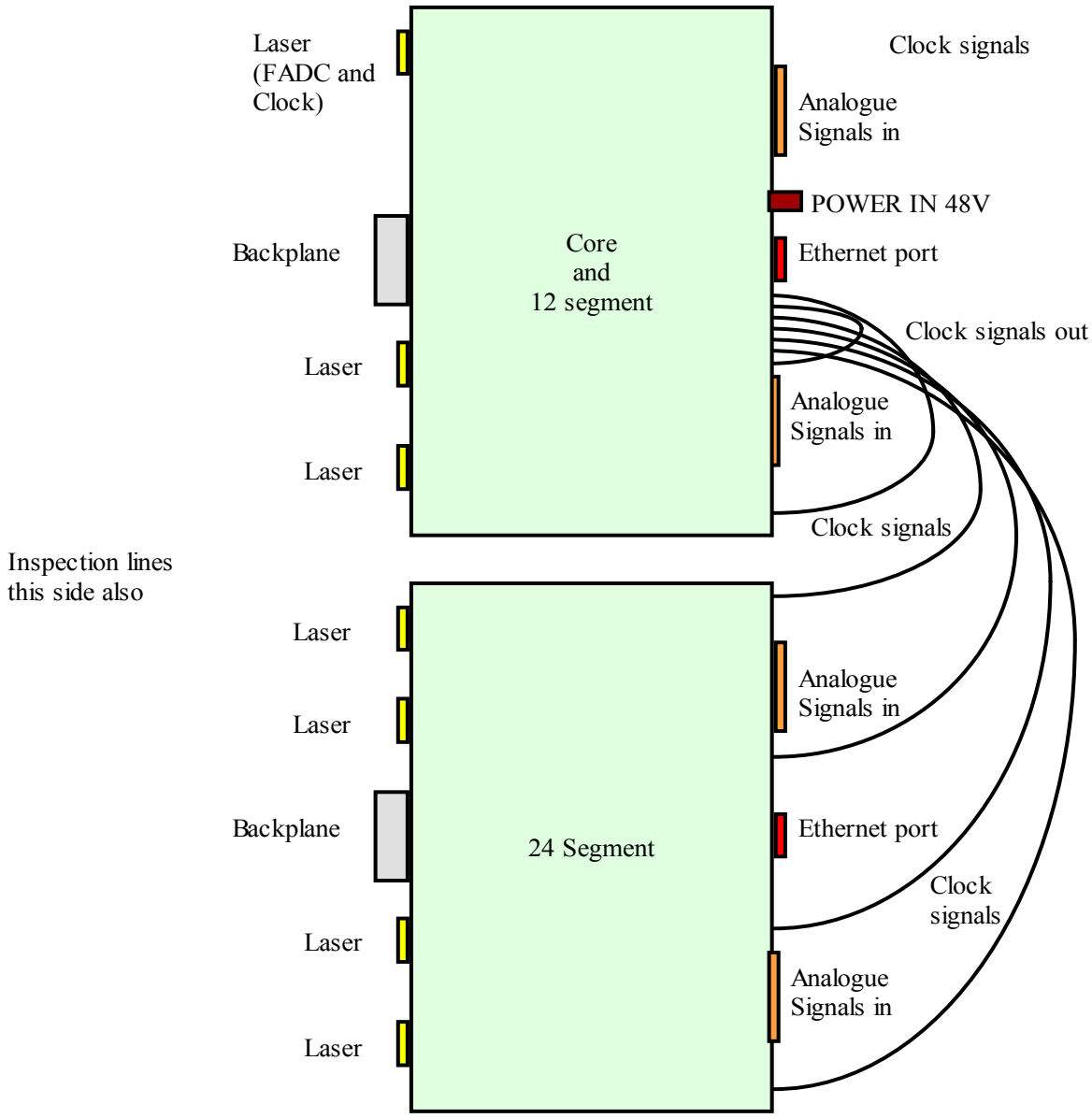


Fig 31 Top view of modules showing interconnects.

In order to prevent undue forces on the rear connector and it preventing the module from resting on the cooling plates correctly, the rear connector in the module which mates with the back plane connector should be free to move slightly (<=0.5mm). This can be achieved by using the natural flexibility in FR4 PCB material as shown in figure 5, or else by avoiding over constraining the area close to the connector.

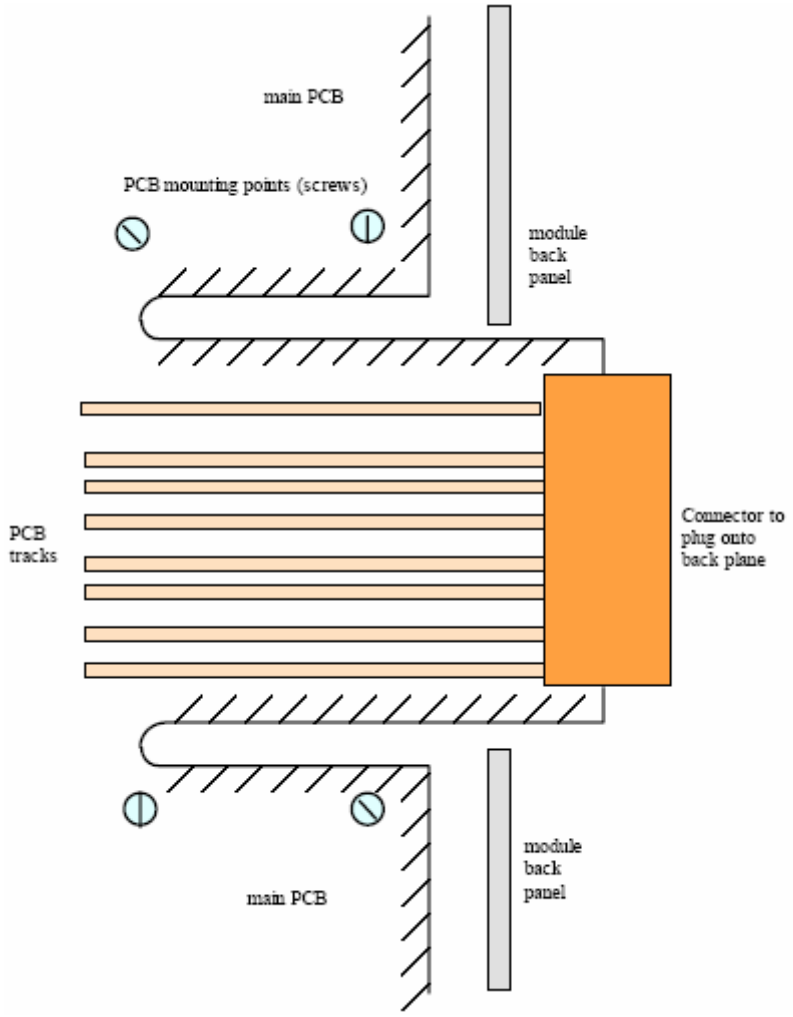


Fig 32 Arrangement to allow connector freedom to move slightly in vertical direction. (+/-0.5mm maximum movement required).

Further investigation will be needed into the deformable thermal material in particular its resilience, behaviour with condensation and water absorption (which must be very low), availability and price.

c) Advantages of this system:

- Robust
- No need to break water supply to remove any faulty module.
- Back plane can be replaced in situ.
- Top and bottom surfaces of electronic modules are in contact with the cool surfaces.
- Any module can be removed without effecting the remaining modules.
- It is not necessary to remove the whole rack unit in order to disconnect cables between the top (core) module and the lower (segment) modules.
- Access to the electronics boards is very easy after the module is removed from the rack.

Tests done on a mock-up rig consisting of one module with cooled plates below and above have shown that this approach is practical. There are still some difficulties to be overcome but thermally the solution works well. Tests done at Liverpool show that with 100W dissipated within the module spread over 8 PCBs (each 12.5W), the coolant temperature rose by 2.5degC and the PCB temperature (at the heat source = resistor) rose by between 17 to 33 degC, depending on thermal material type. The best thermally conductive being the most expensive. Each resistor which covered an area of approximately $2cm^2$ was dissipating 4W. Thus a $1cm^2$ device dissipating 2W would be running at approximately 17degC above the coolant temperature with the best thermal material. Devices with lower power dissipation but still requiring cooling can use lower quality and cheaper materials if required. The temperature remained stable with time and tracked the coolant temperature. The full results do not need to be included here, but the system does function best when the coolant temperature is close to room temperature, since then the coolant is not removing heat from the surrounding atmosphere reducing the cooling system efficiency.

Fig 33 Photography of the first mechanical module

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IV-2 PCB repartition

a) Core module

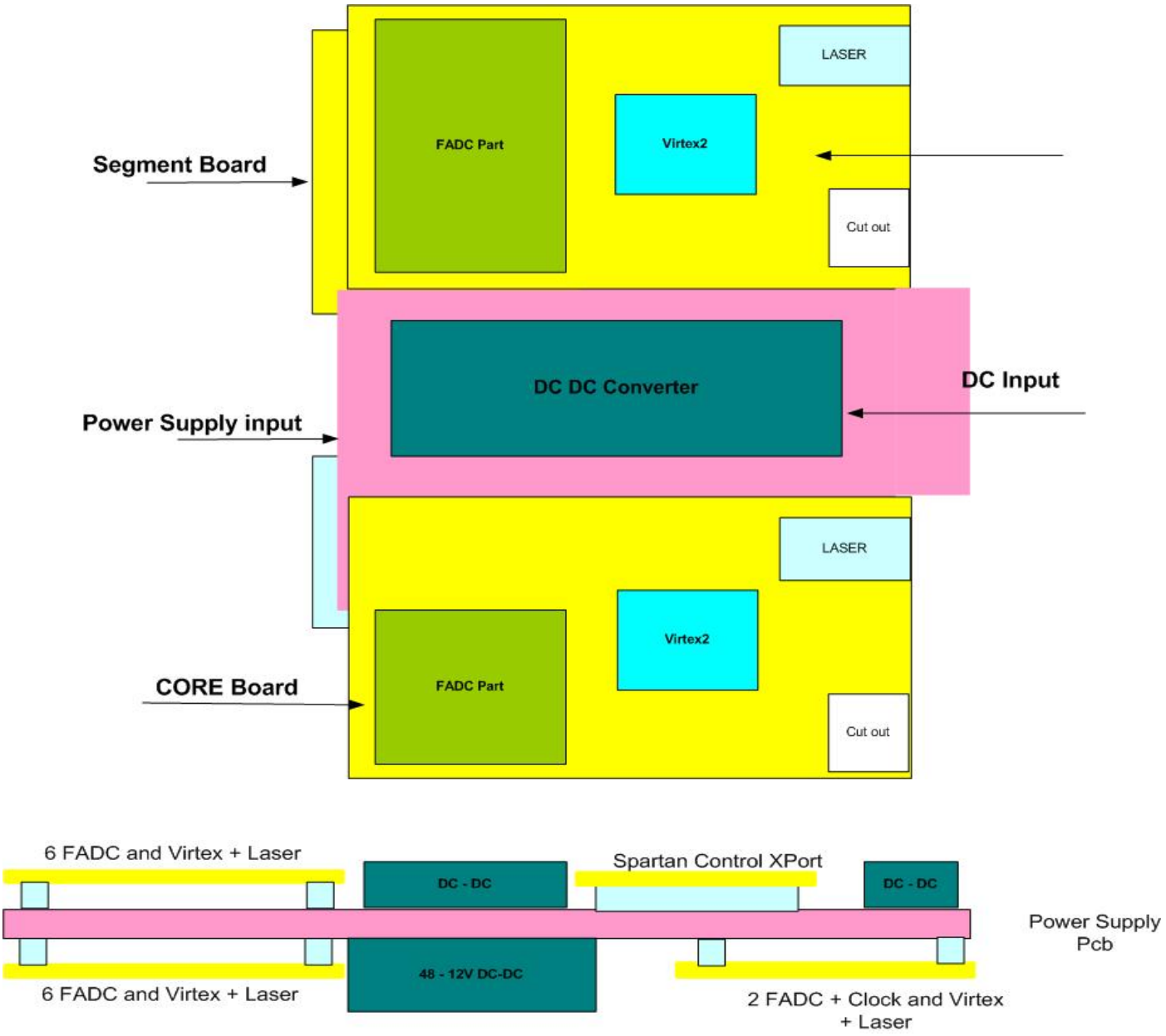

Fig 34 PCB Core module

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b) Segment module

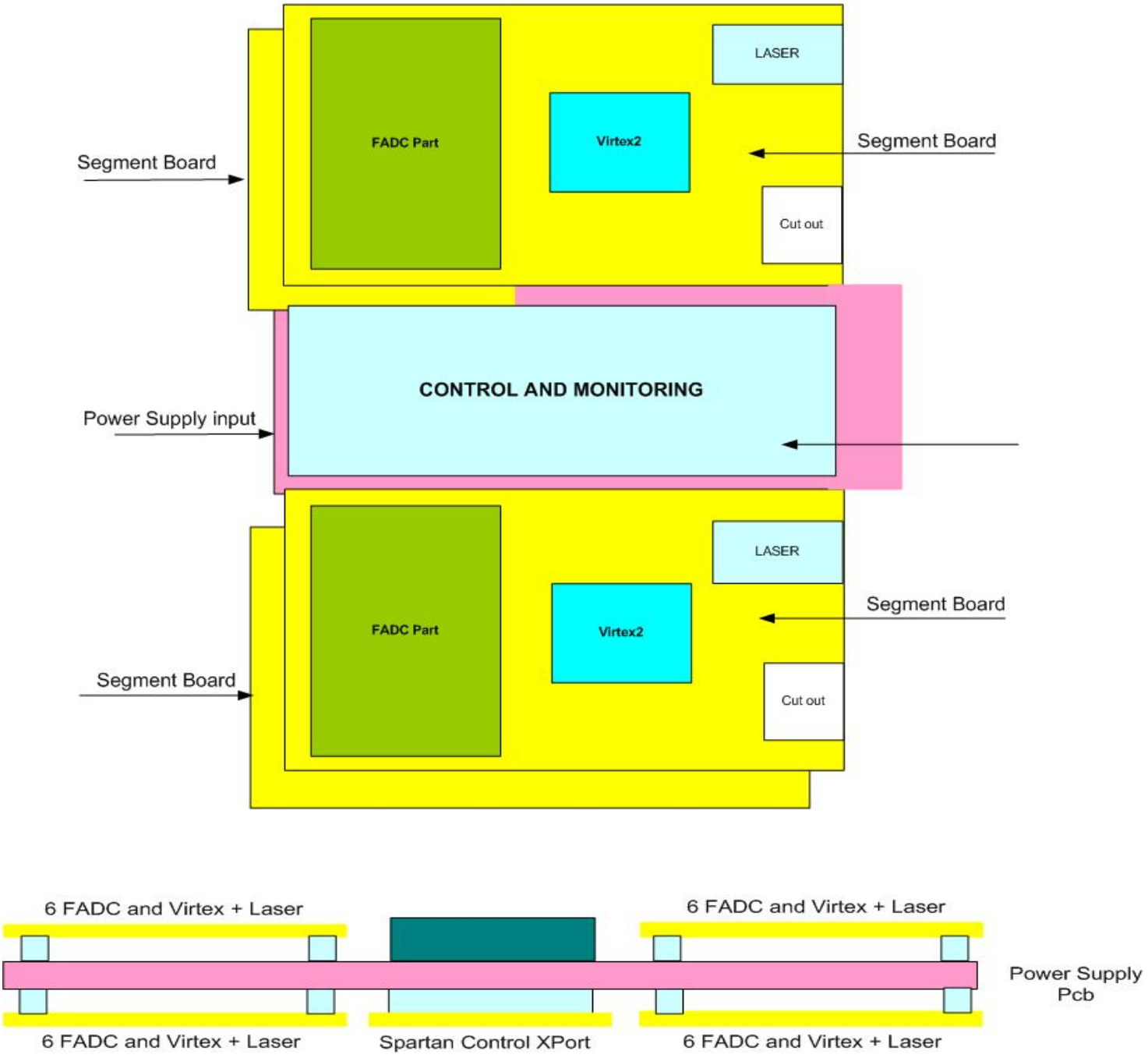

Fig 35 PCB Segment module

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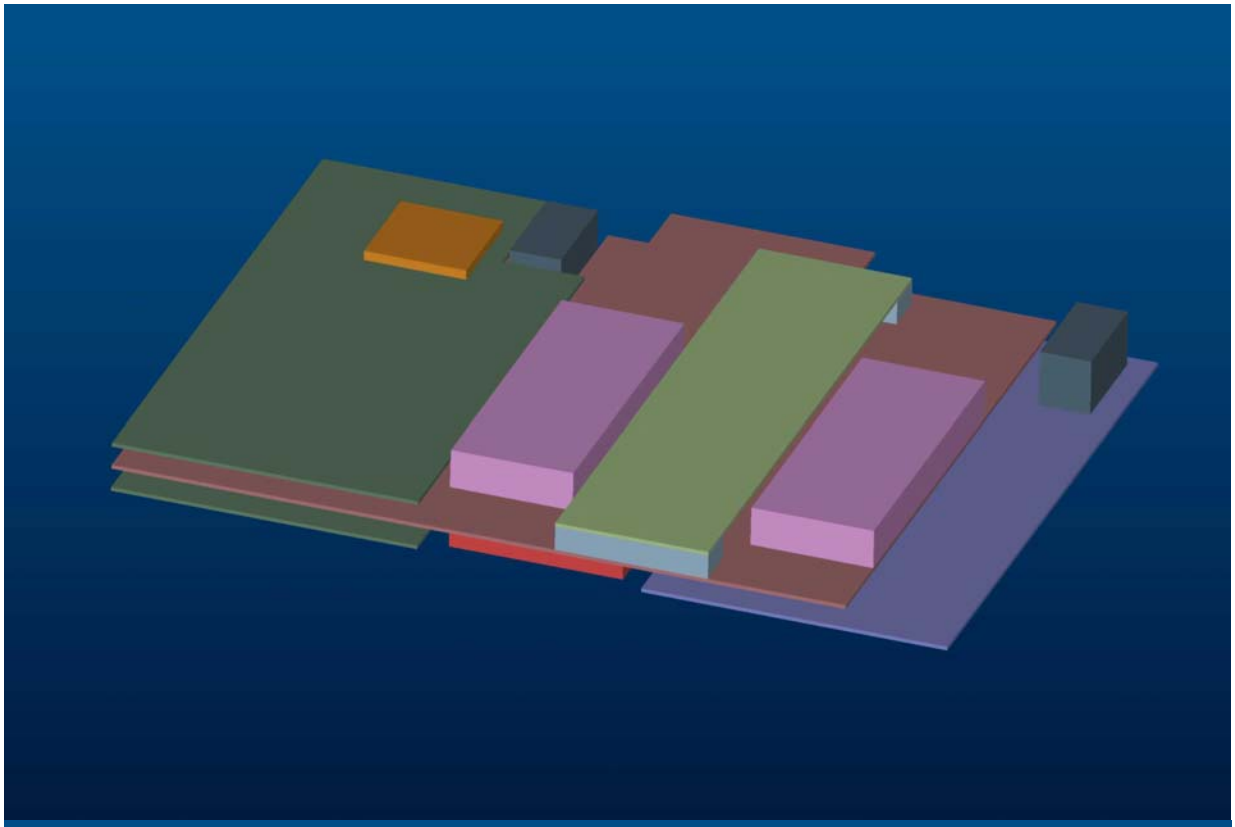
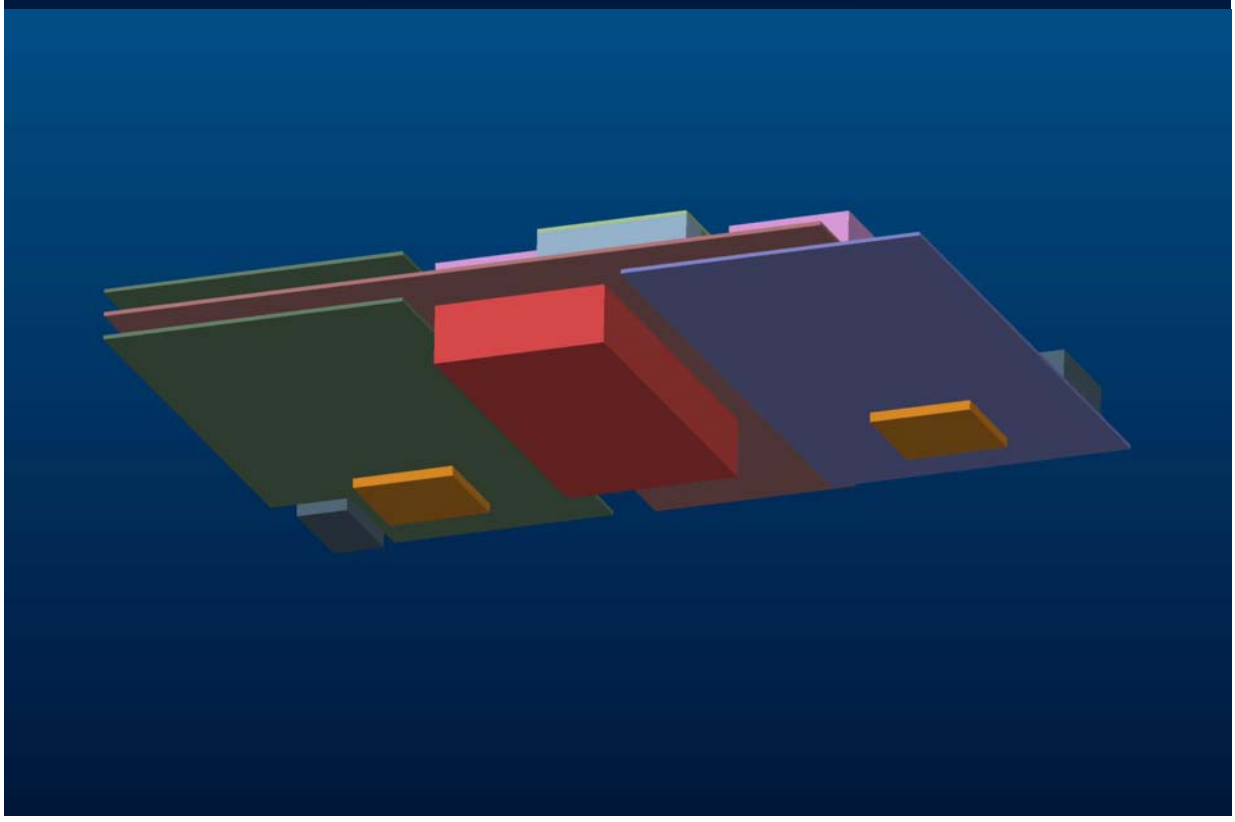
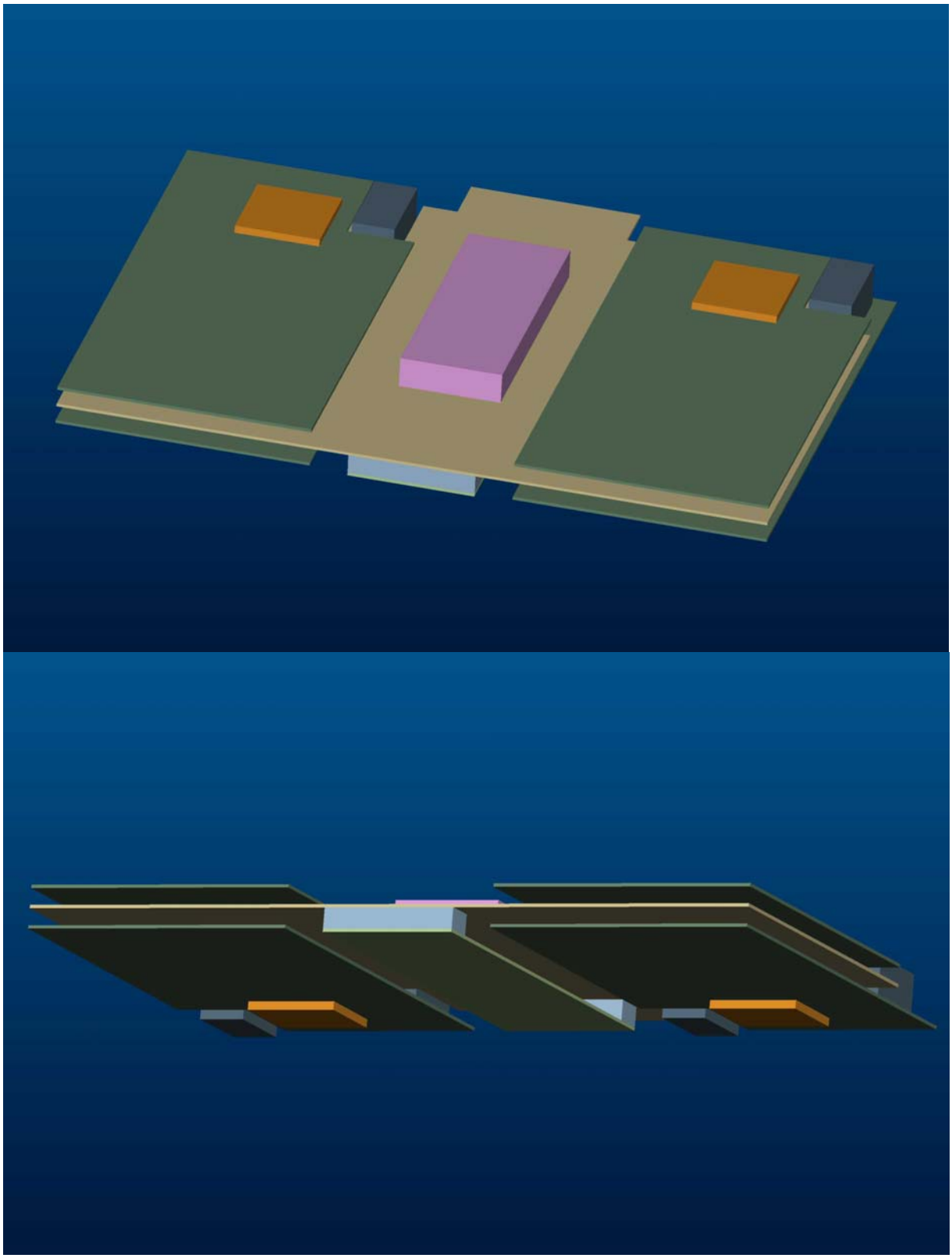
IV-3 Assembly pictures

a) Core Module

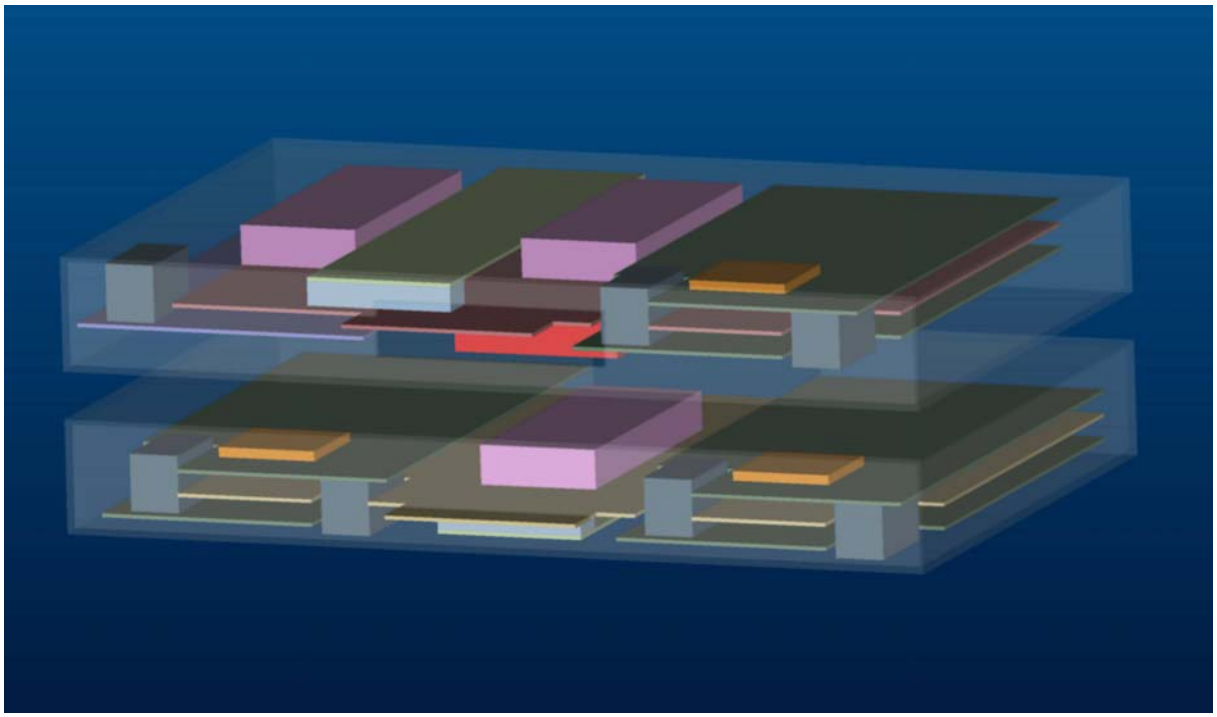




b) Segment Module



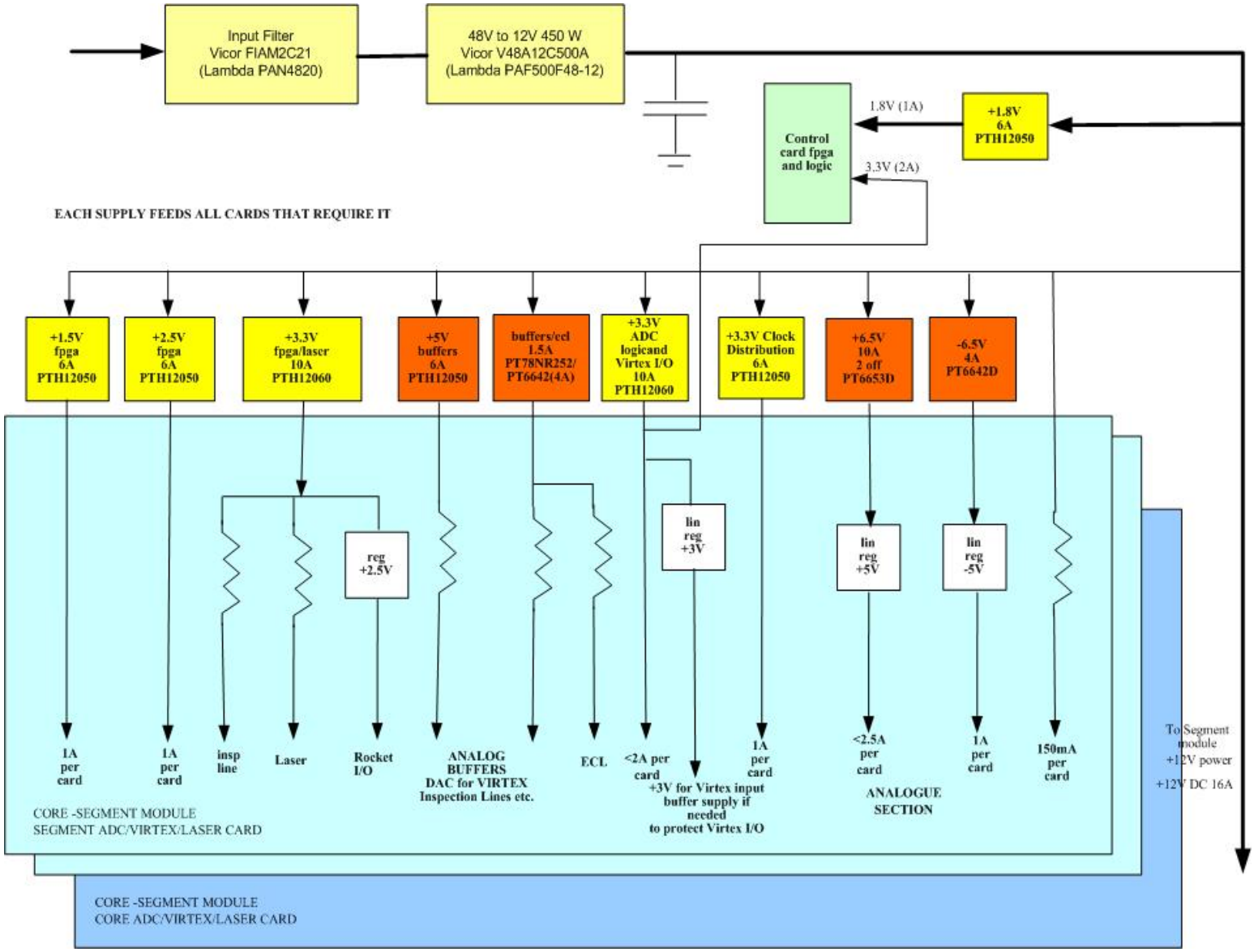
c) Global assembly



V. DC SUPPLY DISTRIBUTION

The DC supply has to be compatible with the integration. Tree distributions is complex to take care about all the different voltage needed by the FPGA and the analog part. To reduce the noise level and the power dissipation it has been decided to use as first module a DC-DC converter from Vicor. Because of the noise due to this type of module an EMI filter will be connected at the input interface. The input voltage will be 48 Volts DC @8 Amps.

V-1 Core DC supply



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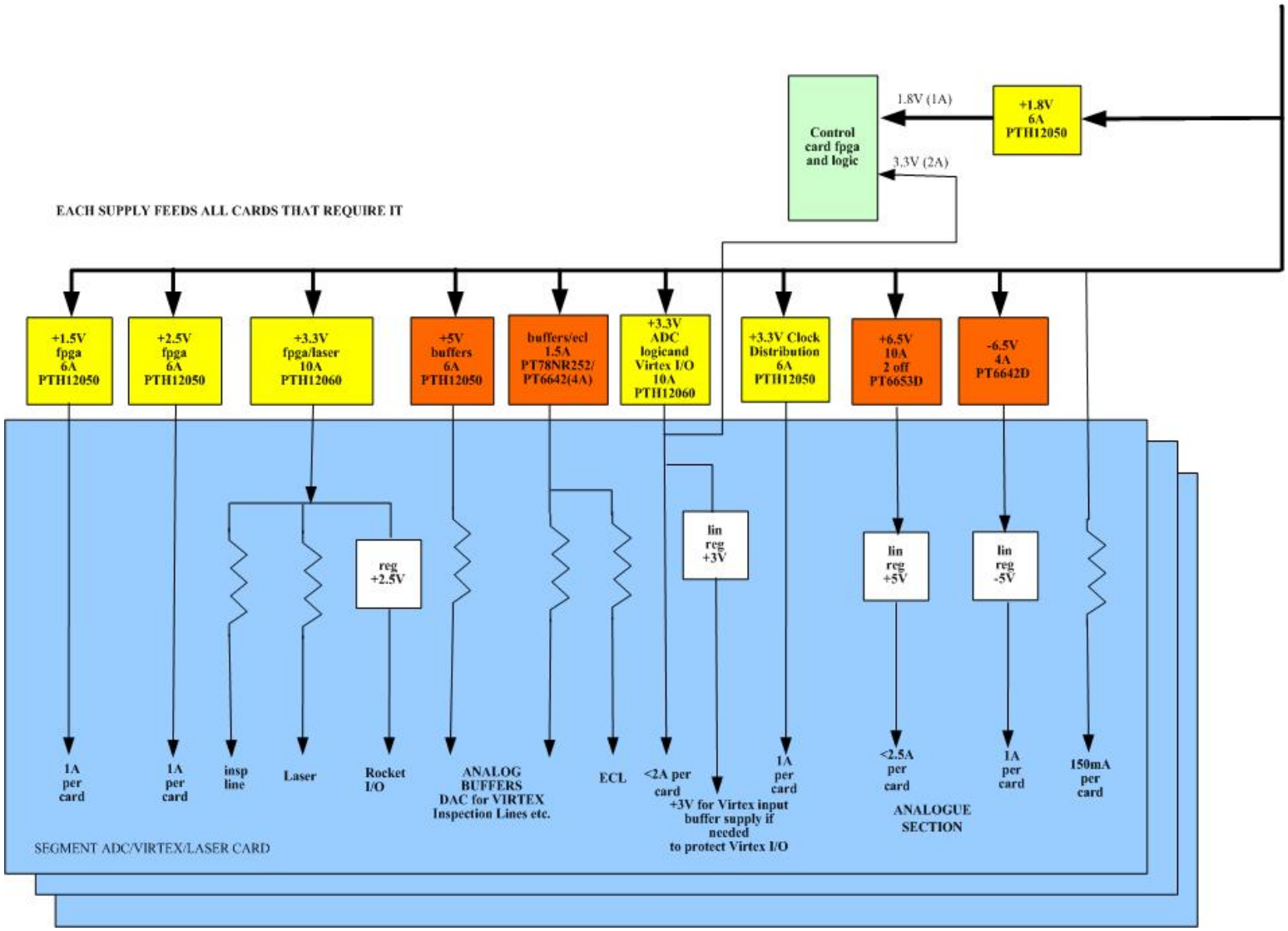
V-2 Segment DC supply.



VI. GLOBAL COST

The global cost is estimate at 30 000 Euros by digitizer.
The first prototype will be around 45 000 Euros

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VII. ANNEXES

1. FADC AD 6645-80 MHz

The FADC is available in 80MHz now and 100MHz is just coming to the market. These comments are based on the 80MHz version, but the plans assume that the 100MHz version will be used and that its performance will be essentially the same as the 80MHz version.

a) Some specifications :

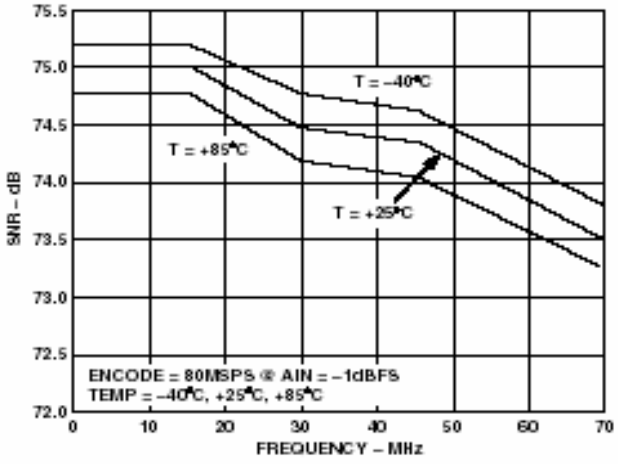
- Resolution 14 bits
- No missing codes
- DNL -1 < 0,25 < 1,5 LSB
- Temperature drift :
- Gain error 48 ppm /1° C (1 channel for full scale)
- SNR:

Parameter (Conditions)		Temp	Test Level	AD6645ASQ-80 Min	Typ	Max	Unit
SNR							
Analog Input	15.5 MHz	25°C	V		75.0		dB
@ –1 dBFS	30.5 MHz	25°C	II	72.5	74.5		dB

- **ENOB:**

15, 5 MHz ENOB = 12, 12 bits
30,5 MHz ENOB = [11,75 12] bits

- **SNR / TEMPERATURE**



TPC 7. Noise vs. Analog Frequency

For the total range of temperature T = [-40°:+85°] the SNR = [74, 7:75, 2] and the ENOB = [12: 12, 2]. The temperature doesn't have a significant effect on the SNR.

From the point of view of SNR it is not necessary to have cooling for this component. To increase the stability of gain the best and simple choice will be to use a heat sink bonded to the PCB. The principle has been presented by Ian at the Liverpool meeting.

b) Switching specifications

- Timing diagram

  Analog device datasheet:

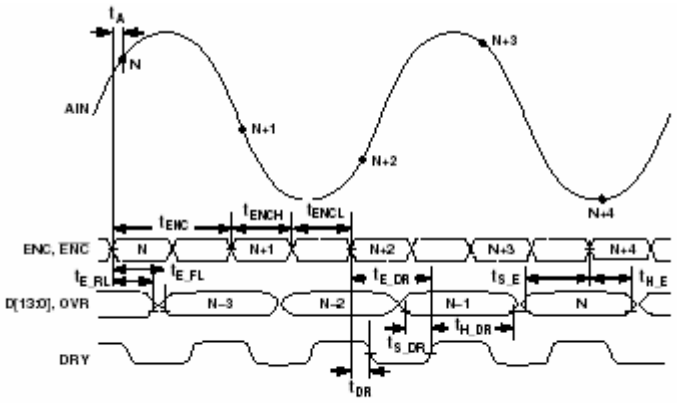


Figure 1. Timing Diagram

Parameter (Conditions)	Name	Temp	Test Level	AD6645ASQ-80 Min	Typ	Max	Unit
ENCODE Input Parameters[1]							
Encode Period[1] @ 80 MSPS	t_{ENC}	Full	V		12.5		ns
Encode Pulsewidth High[2] @ 80 MSPS	t_{ENCH}	Full	V		6.25		ns
Encode Pulsewidth Low @ 80 MSPS	t_{ENCL}	Full	V		6.25		ns
ENCODE/DataReady							
Encode Rising to DataReady Falling	t_{DR}	Full	V	1.0	2.0	3.1	ns
Encode Rising to DataReady Rising	t_{E_DR}	Full	V		$t_{ENCH} + t_{DR}$		ns
@ 80 MSPS (50% Duty Cycle)		Full	V	7.3	8.3	9.4	ns
ENCODE/DATA (D13:0), OVR							
ENC to DATA Falling Low	t_{E_FL}	Full	V	2.4	4.7	7.0	ns
ENC to DATA Rising Low	t_{E_RL}	Full	V	1.4	3.0	4.7	ns
ENCODE to DATA Delay (Hold Time)[3]	t_{H_E}	Full	V	1.4	3.0	4.7	ns
ENCODE to DATA Delay (Setup Time)[4]	t_{S_E}	Full	V		$t_{ENC} - t_{E\_FL}$		ns
Encode = 80 MSPS (50% Duty Cycle)		Full	V	5.3	7.6	10.0	ns
DataReady (DRY[5])/DATA, OVR							
DataReady to DATA Delay (Hold Time)[2]	t_{H_DR}	Full	V		Note 6		ns
Encode = 80 MSPS (50% Duty Cycle)				6.6	7.2	7.9	
DataReady to DATA Delay (Setup Time)[2]	t_{S_DR}	Full	V		Note 6		ns
Encode = 80 MSPS (50% Duty Cycle)				2.1	3.6	5.1	

The timing diagram in correspondence with the parameters limits shows that the Data are ready in regards with the DRY signal and not ENC/ENC.

The data bus must be synchronous with the DRY signal (Data Ready Signal)
The time skew between different components could be enough big to create some synchronisation problems. This is why each transceiver must use DRY for its own clock.

c) Clock jitter

Analog devices datasheet says:

Jitter Considerations

The signal-to-noise ratio (SNR) for an ADC can be predicted. When normalized to ADC codes, the above equation accurately predicts the SNR based on three terms. These are jitter, average DNL error, and thermal noise. Each of these terms contributes to the noise within the converter.

F_{ANALOG} = analog input frequency
$t_{j\,RMS}$ = rms jitter of the encode (rms sum of encode source and internal encode circuitry)
ϵ = average DNL of the ADC (typically 0.41 LSB)
n = number of bits in the ADC
$V_{NOISE\,RMS}$ = V rms thermal noise referred to the analog input of the ADC (typically 0.9 LSB rms)

For a 14-bit analog-to-digital converter, like the AD6645, aperture jitter can greatly affect the SNR performance as the analog frequency is increased. The chart below shows a family of curves that demonstrate the expected SNR performance of the AD6645 as jitter increases. The chart is derived from the above equation.

$$SNR = 1.76 - 20\log\left[\left(2\pi \times F_{ANALOG} \times t_{j\,rms}\right)^2 + \left(\frac{1+\varepsilon}{2^n}\right)^2 + \left(\frac{2\times\sqrt{2}\times V_{NOISE\,rms}}{2^n}\right)^2\right]^{\frac{1}{2}}$$

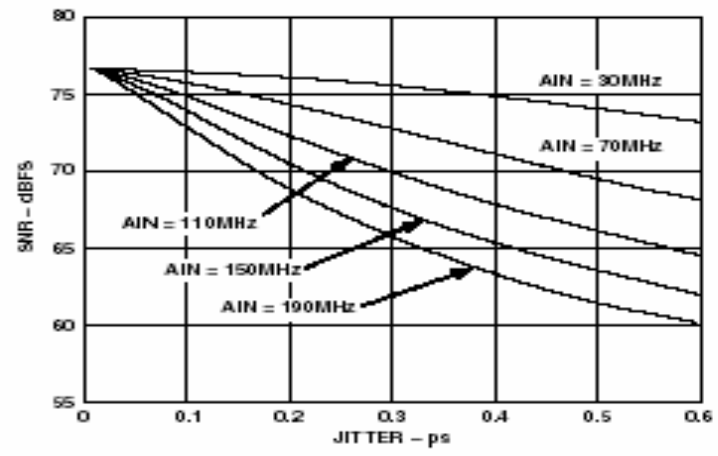


Figure 12. Jitter vs. SNR

The figure 12 shows clearly the effect of jitter. If we want the SNR as good as possible then the clock must be as good as possible.
This is why the FADC clock must be built with specific components related to this specific application. (Digital PLL). **If we want at less the ENOB greater than 11 for an analogue input signal bandwidth equal to 30 MHz we must have a jitter less than 1.5 ps**

d) Layout

- **Digital outputs**

Analog devices datasheet says:

Digital Outputs

Care must be taken when designing the data receivers for the AD6645. It is recommended that the digital outputs drive a series resistor followed by a gate such as the 74LCX574. To minimize capacitive loading, there should only be one gate on each output pin. An example of this is shown in the evaluation board schematic shown in Figure 13. The digital outputs of the AD6645 have a constant output slew rate of 1 V/ns. A typical CMOS gate combined with a PCB trace will have a load of approximately 10 pF. Therefore, as each bit switches 10 mA $(10\ pF \times 1V \div 1\ ns)$ of dynamic current per bit will flow in or out of the device. A full-scale transition can cause up to 140 mA (14 bits × 10 mA/bit) of current to flow through the output stages. The series resistors should be placed as close to the AD6645 as possible to limit the amount of current that can flow into the output stage. These switching currents are confined between ground and the DV_{CC} pin. Standard TTL gates should be avoided since they can appreciably add to the dynamic switching currents of the AD6645. It should be noted that extra capacitive loading will increase output timing and invalidate timing specifications. Digital output timing is guaranteed for output loads up to 10 pF.

Because of the Serial Transfer we must put a serialiser at another part of the PCB. The distance will be high so we must avoid the capacitive loading using serial resistors and IC like 74CLX574. Of course it will create a new delay and it is important to delay the control clock into the transceiver.

e) Grounding

Analog device datasheet:

For optimum performance, it is highly recommended that a common ground be utilized between the analog and digital power planes. The primary concern with splitting grounds is that dynamic

more time to settle between samples. In general, splitting the analog and digital grounds can frequently contribute to undesirable EMI-RFI and should therefore be avoided.

To repeat (Analogy Devices' advice)

"FOR OPTIMAL PERFORMANCE, IS IT HIGHLY RECOMMENDED THAT A COMMON GROUND BE UTILIZED BETWEEN THE ANALOG AND DIGITAL POWER PLANS."

"IN GENERAL, SPLITTING THE ANALOG AND DIGITAL GROUNDS CAN FREQUENTLY CONTRIBUTE TO UNDESIRABLE EMI-RFI AND SHOULD THEREFORE BE AVOIDED."

The layout will use a common ground plane for both the analogue and digital part.

2. FIRST PCB DESIGN FOR FADC PART

a) Description

Explanations about the Digitiser Agata_Segment PCB
Layers

The PCB has 10 layers

- L1 = TOP = Conductors
- L2 = GND = Plane
- L3 = IN1 = Conductors
- L4 = AVCC5_F = Filtered Analog +5V Shapes (1/Channel) = Plane
- L5 = AVEE5_F = Filtered Analog -5V Shapes (1/Channel) = Shapes + Conductors
- L6 = AVCC5 = Analog +5V = Plane
- L7 = AVEE5 = Analog -5V = Plane
- L8 = IN2 = Conductors
- L9 = VCC3V3&5 = Digital 3V3 + Filtered Digital 3V3 Shapes + 5V Shape = Plane
- L10 = Bottom = Conductors

The Agata_Segment_4L.pdf file = L1 + L3 + L8 + L10

Ground shapes will be added only at the end on all the layers.

Input Connector

An MDR 26 Connector is foreseen.
It is not present on the PCB because it doesn't exist for the moment in the Cadence basis.

Survey Module

It replaces a differential input module next to the spare channel.

Mechanical adjustment

Some modification of component placement has to be done for the mechanical and the cooling adjustment

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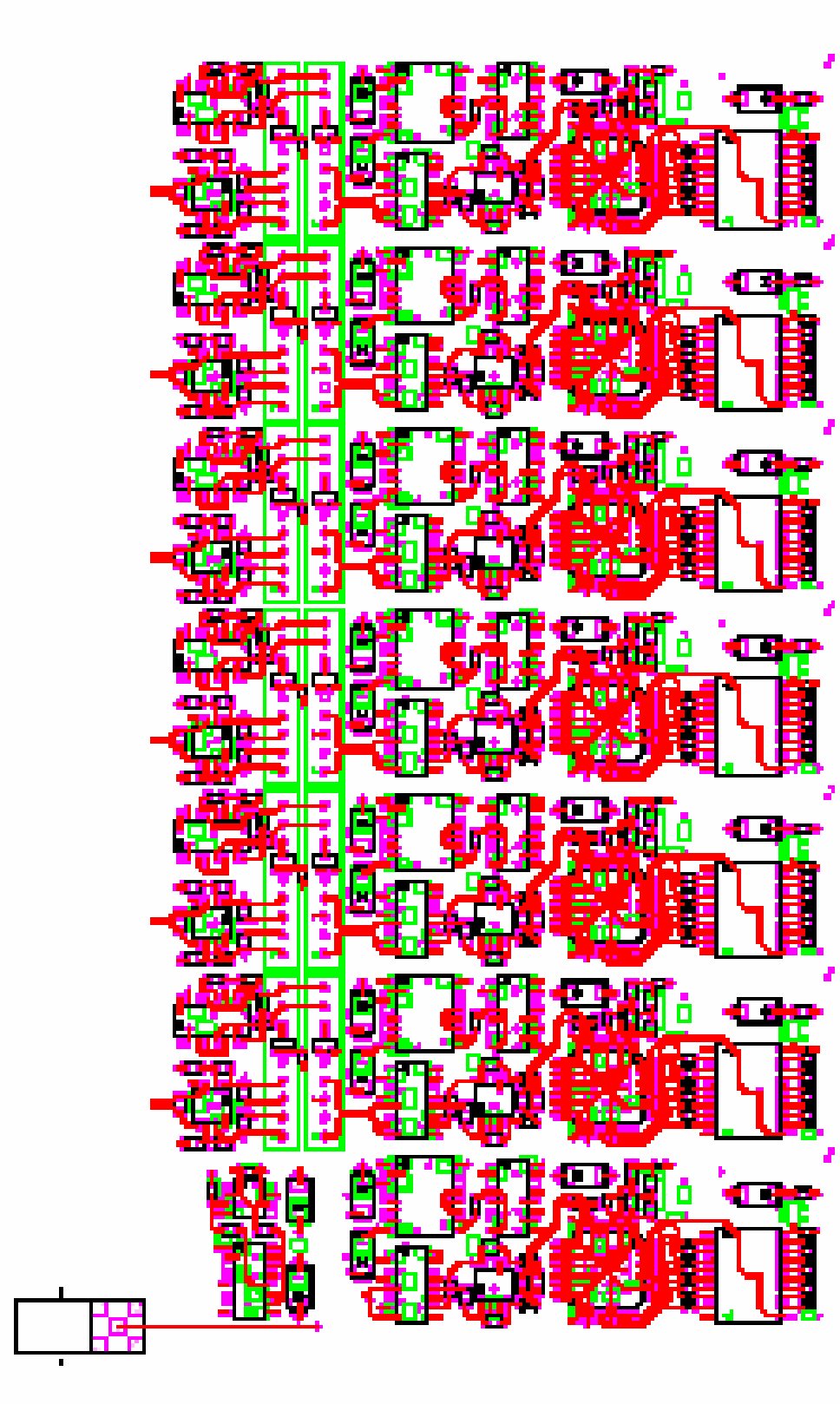
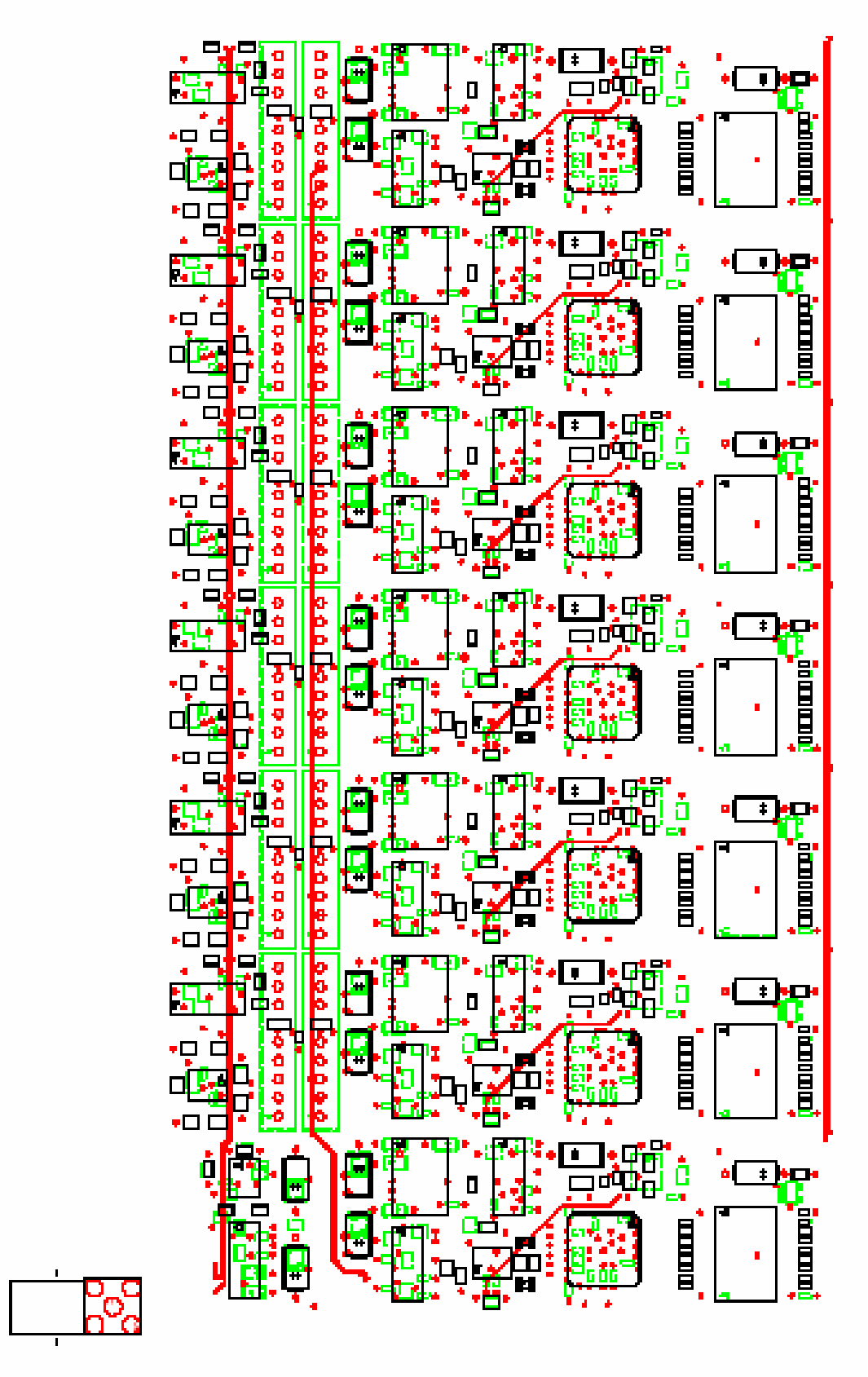
b) L1



c) L3



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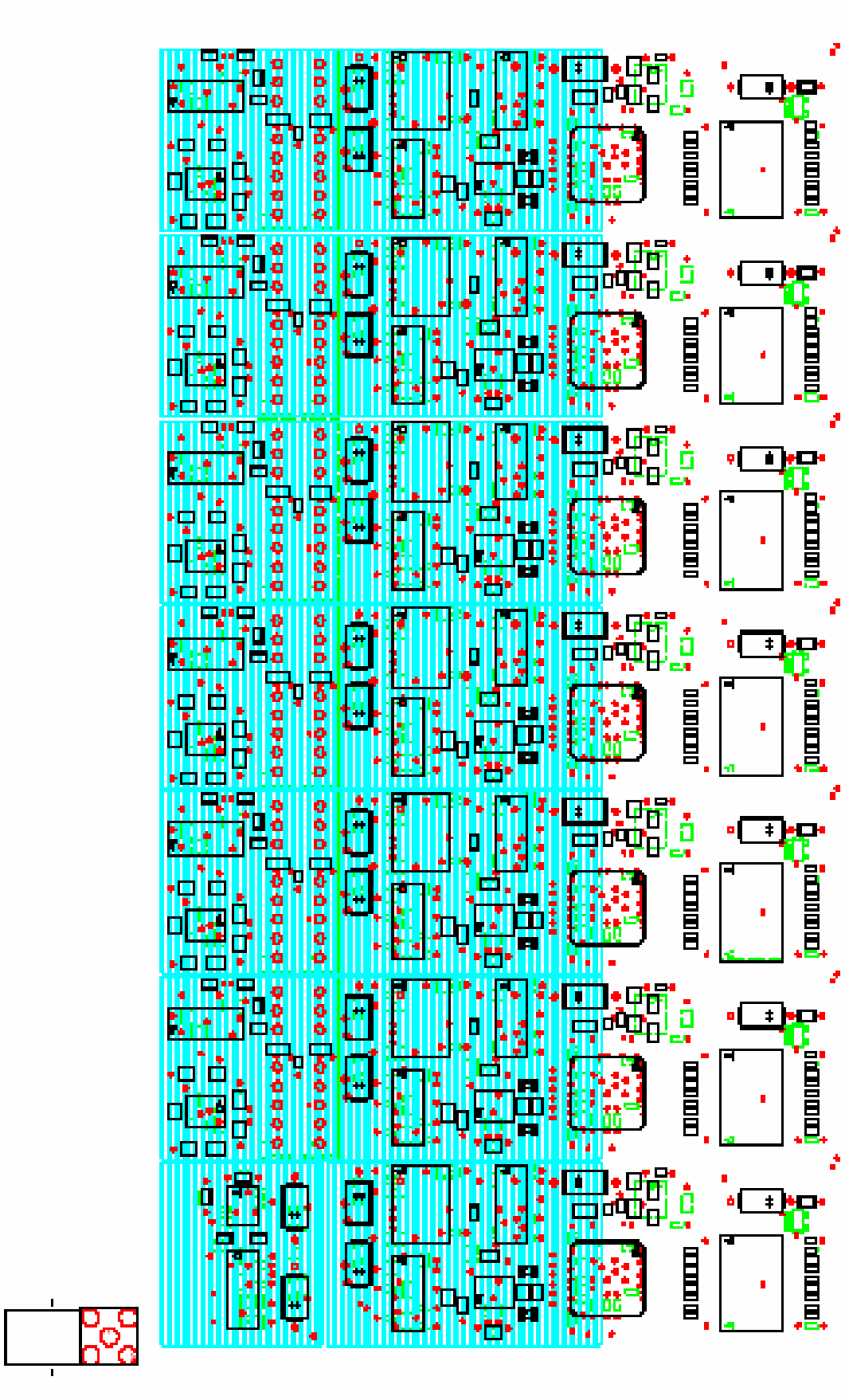
d) L2



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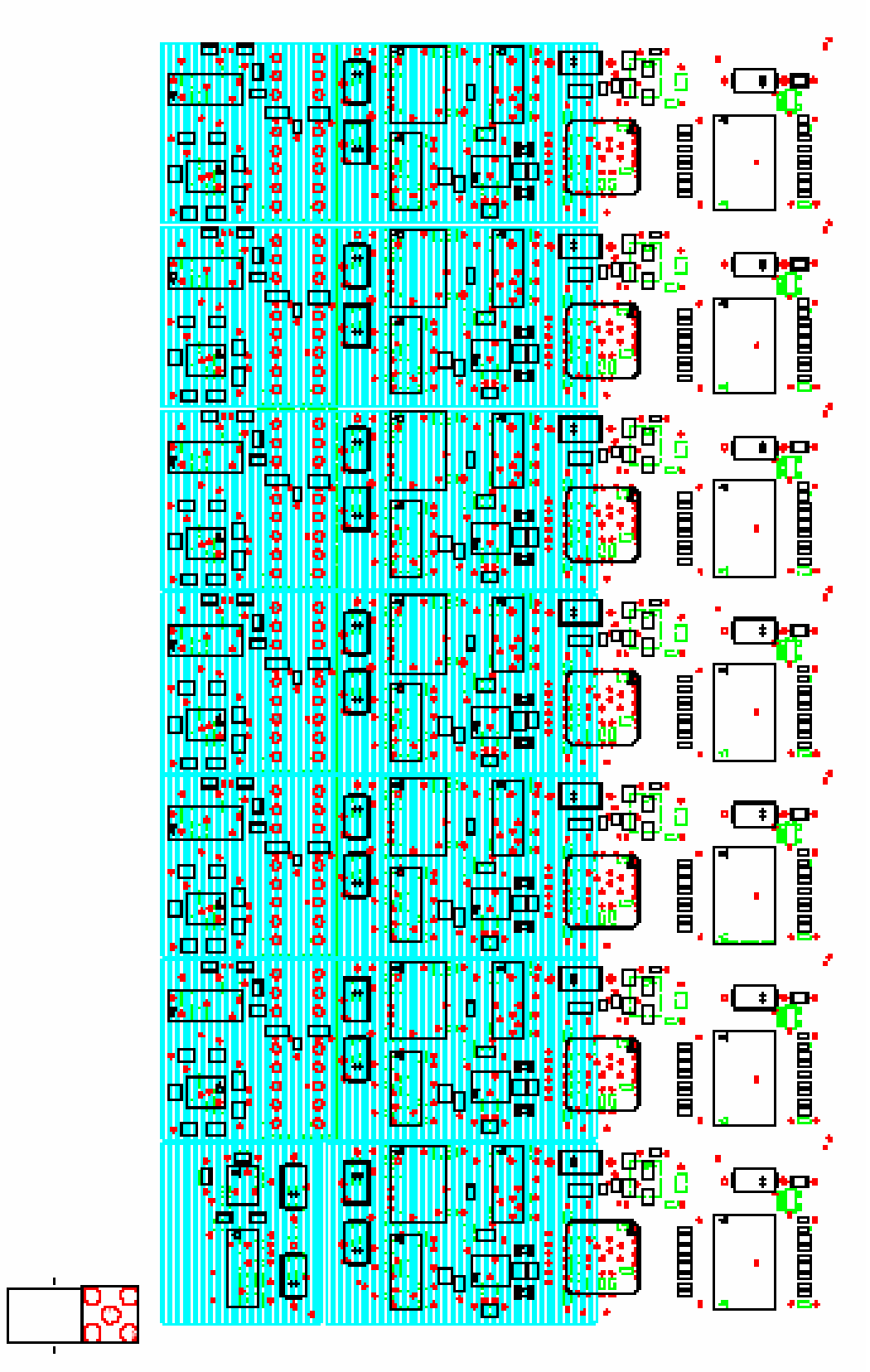
e) L4



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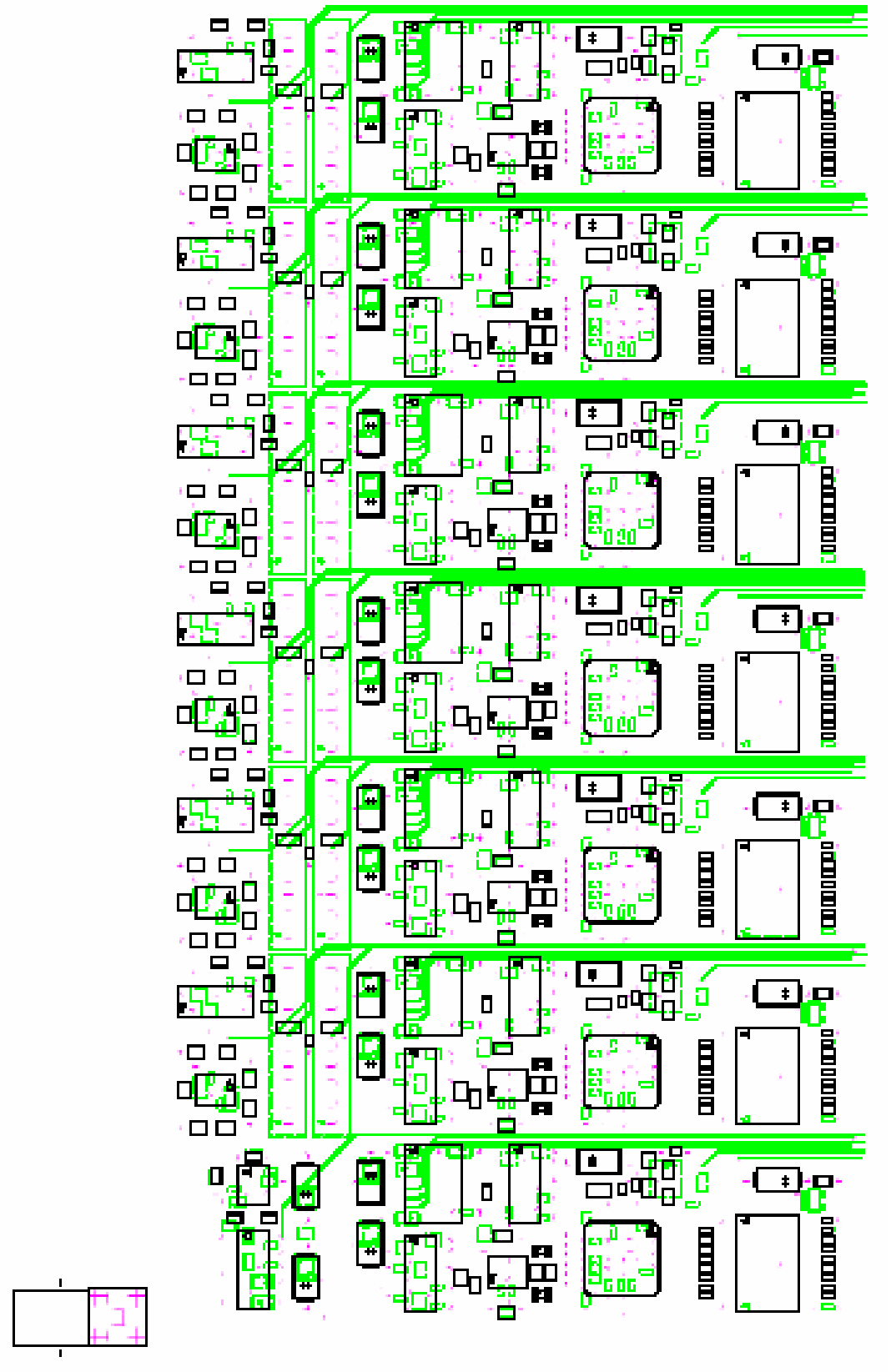
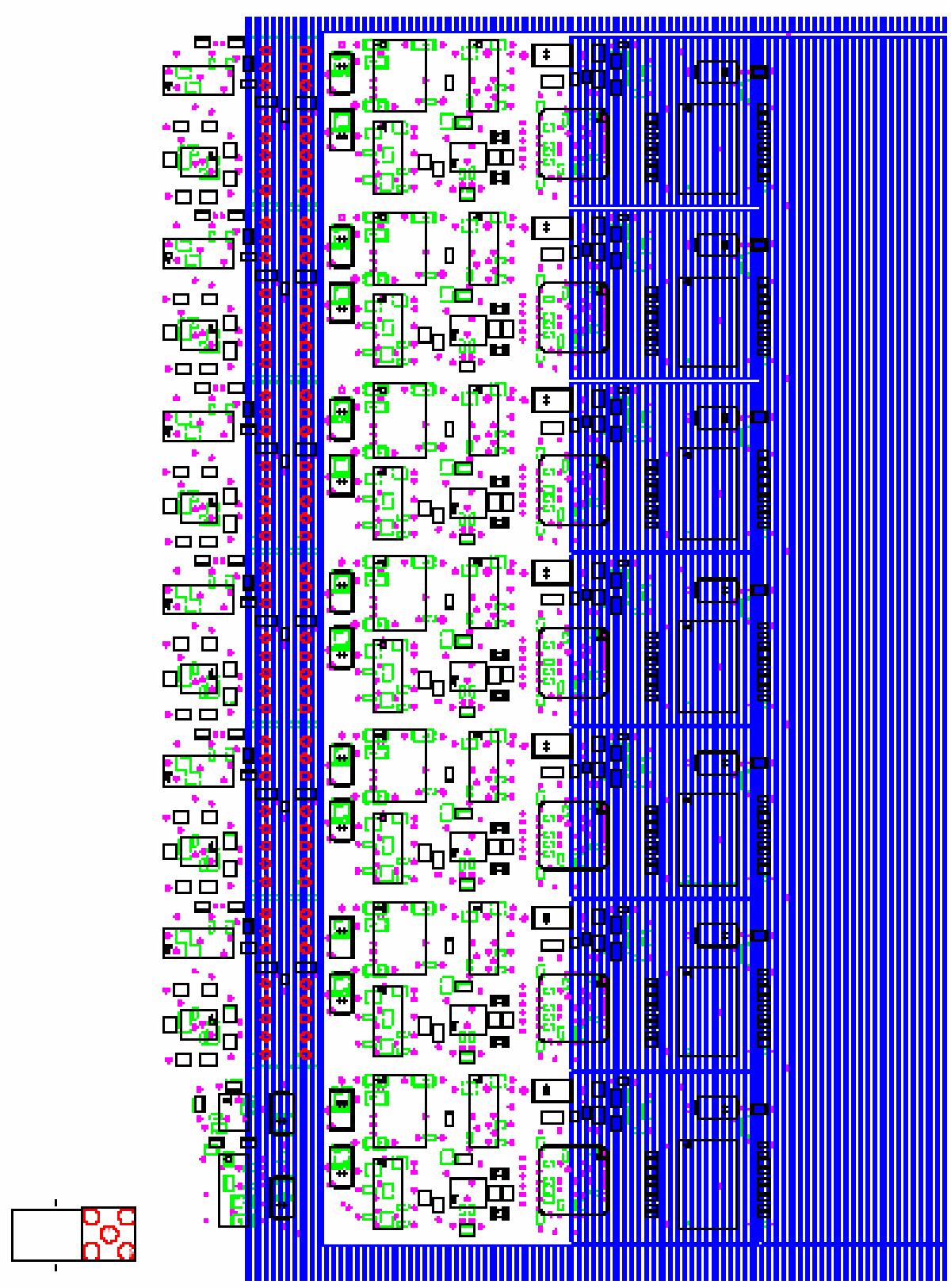
f) L8



g) L9



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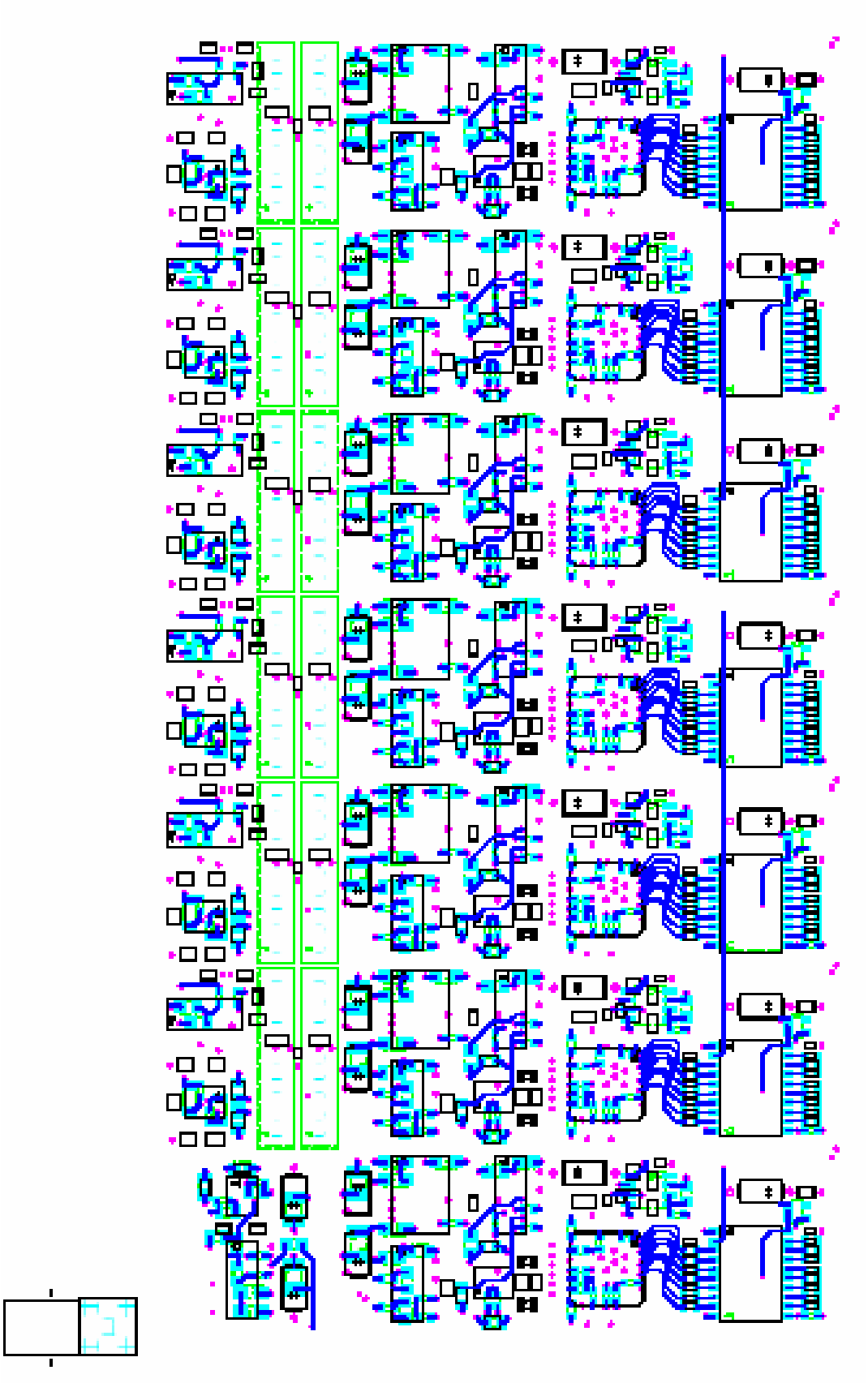
h) L10



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