R3B Si Recoil Readout

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Overview

- *Design Philosophy*
- *Status*
- *Plans*

R3B Si Tracker FEE/DAQ philosophy

1. *Use timestamps, not hard-wired triggers (in or out)*

   Why?

   a) *Eliminating trigger connections removes cable reliability problems and grounding/isolation problems between sub-systems.*
   b) *Adds possibilities when making software triggers e.g. to look back in time*
   c) *Reduces or eliminates dead time (but not pileup)*

2. *Modularity-*

   Why?

   a) *Easier to maintain and upgrade.*
   b) *Easier to re-use (e.g. EXL).*

3. *Front end ASICs*

   Why?

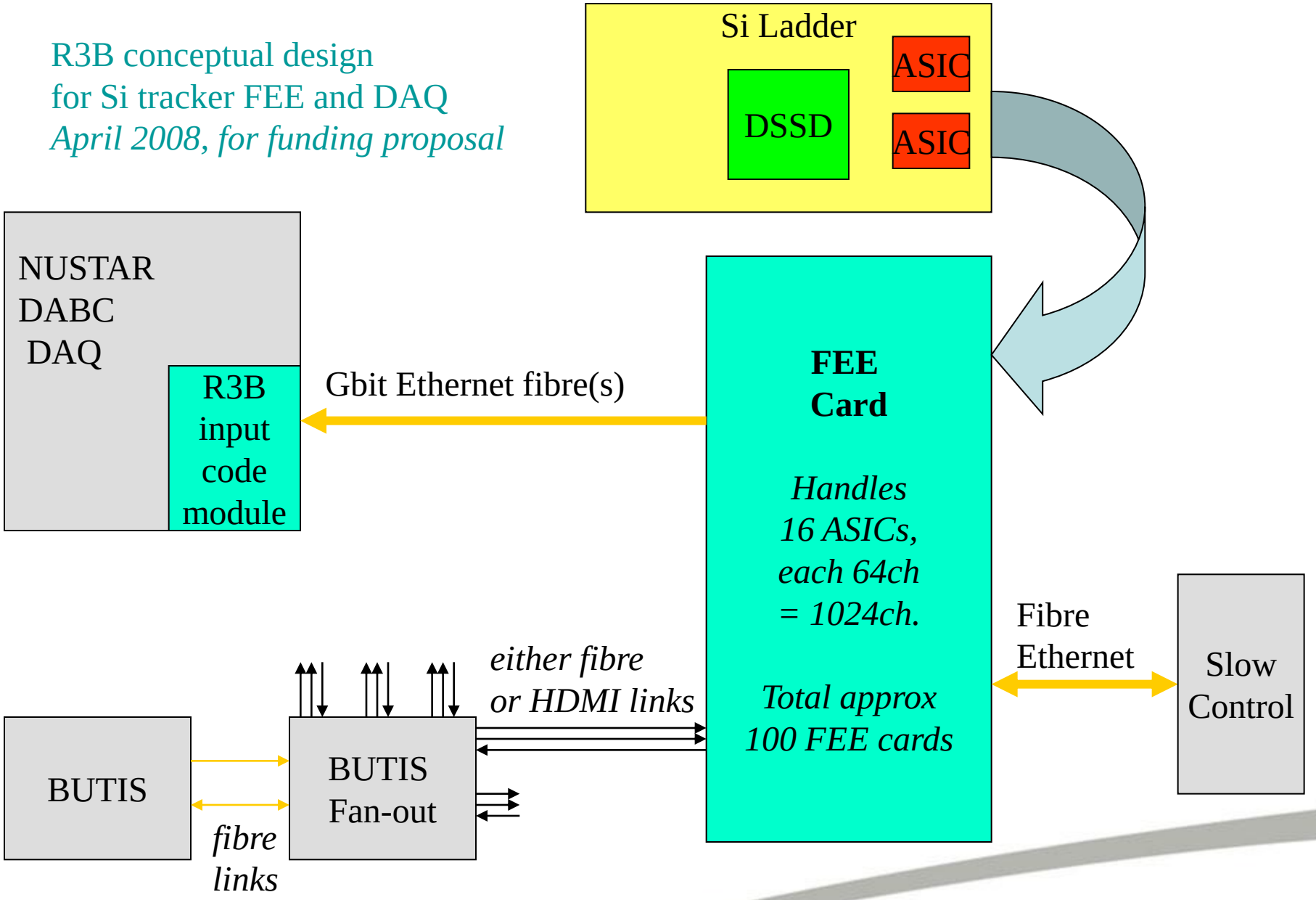
   a) *Large channel count- need to minimise electronics size, power.*
   b) *reduce connections*
   c) *buffer data as close to detectors as possible to improve SNR.*

R3B Si Tracker FEE and DAQ

Outline spec:

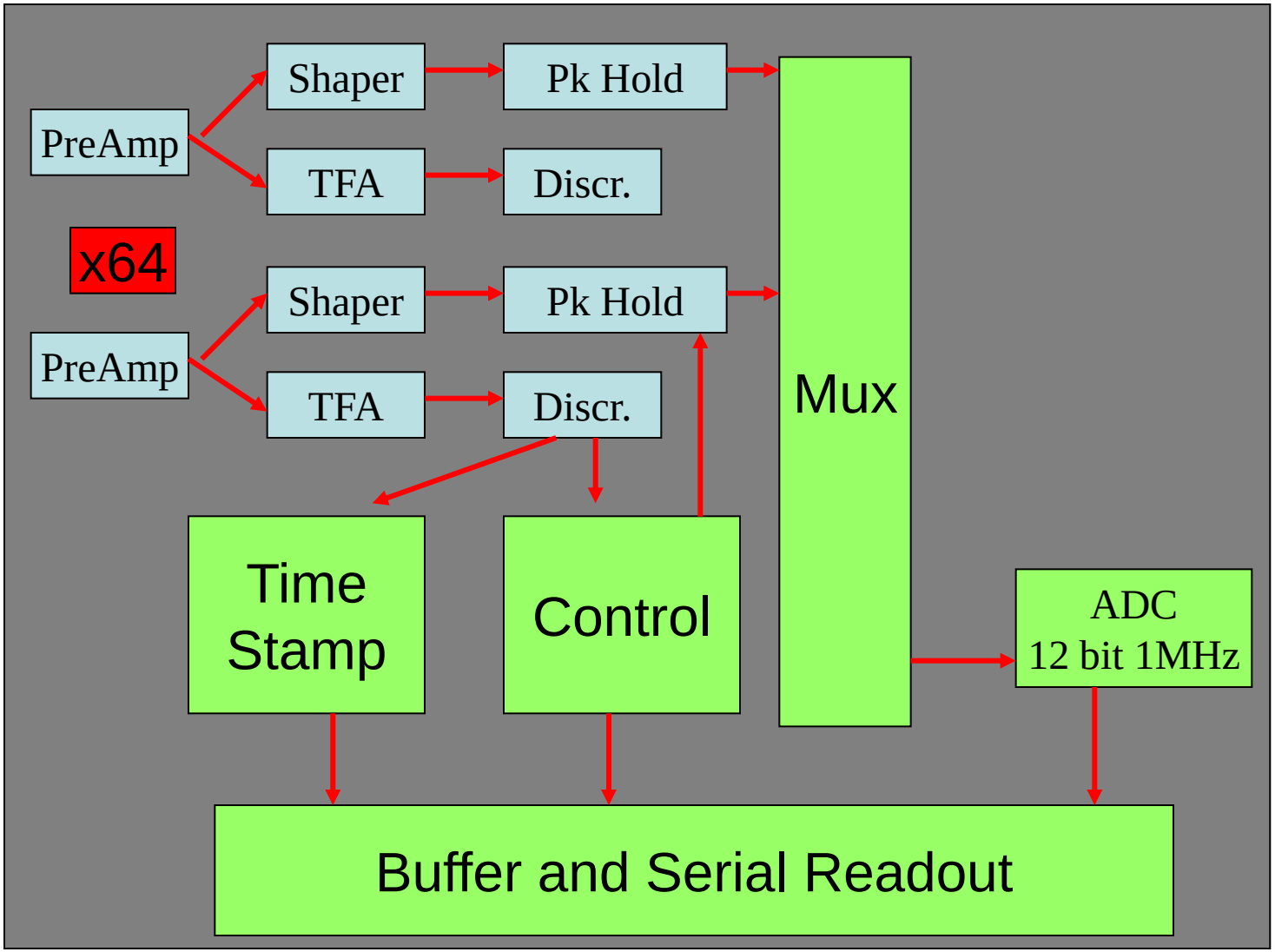
- *Caveat- Si not yet fully simulated so all numbers are provisional based on initial design proposal:*
- 100k channels of Si
- ASICs and Si mounted on ladders
- Cables from ASICs to FEE card
- FEE cards handle about 16 ASICs (each ASIC 64 channels) = 1024

R3B conceptual design
for Si tracker FEE and DAQ
April 2008, for funding proposal

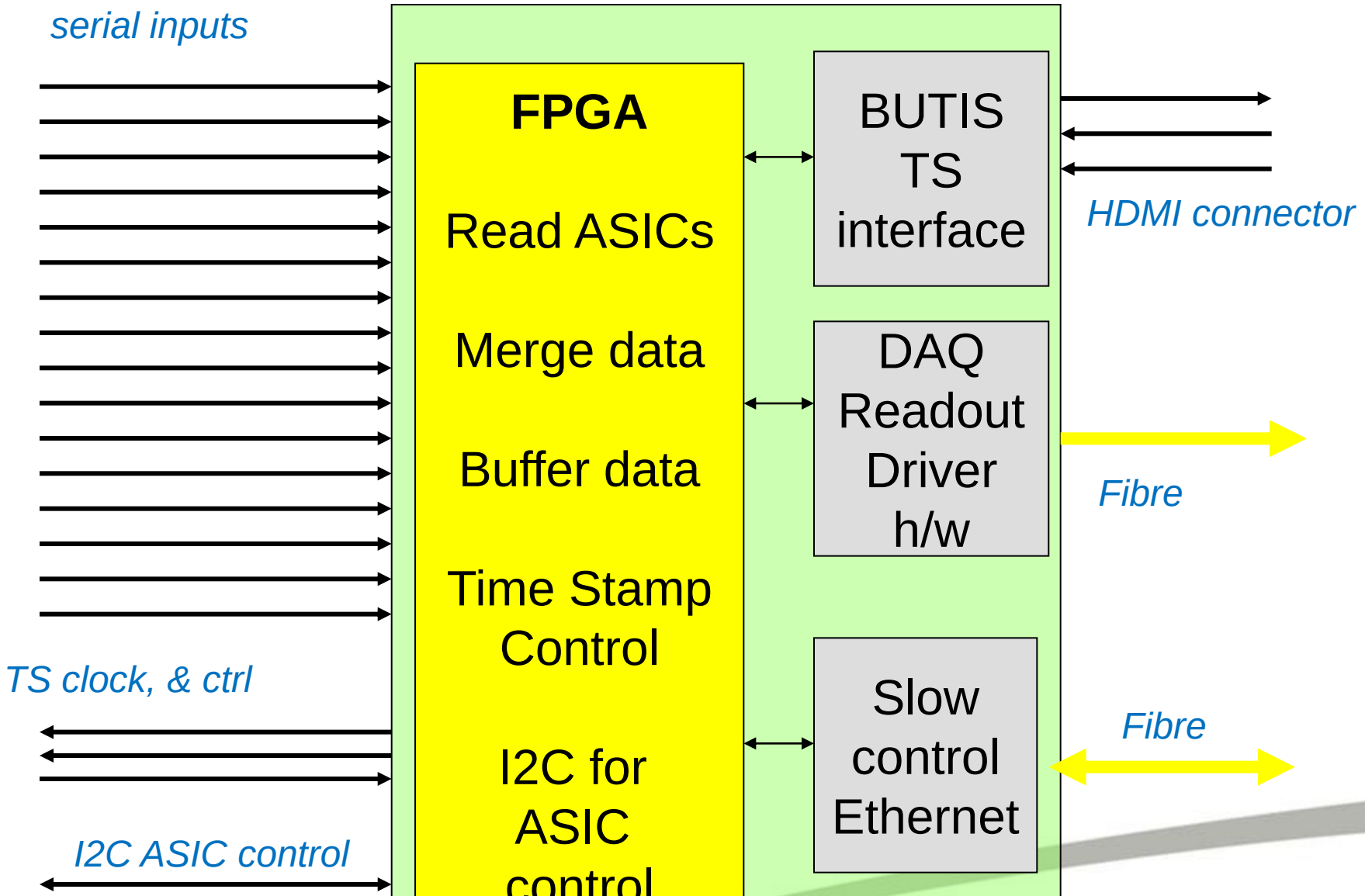


ASIC features:

- Time Stamp
- Zero Suppress
- On chip ADC



R3B FEE card proposal



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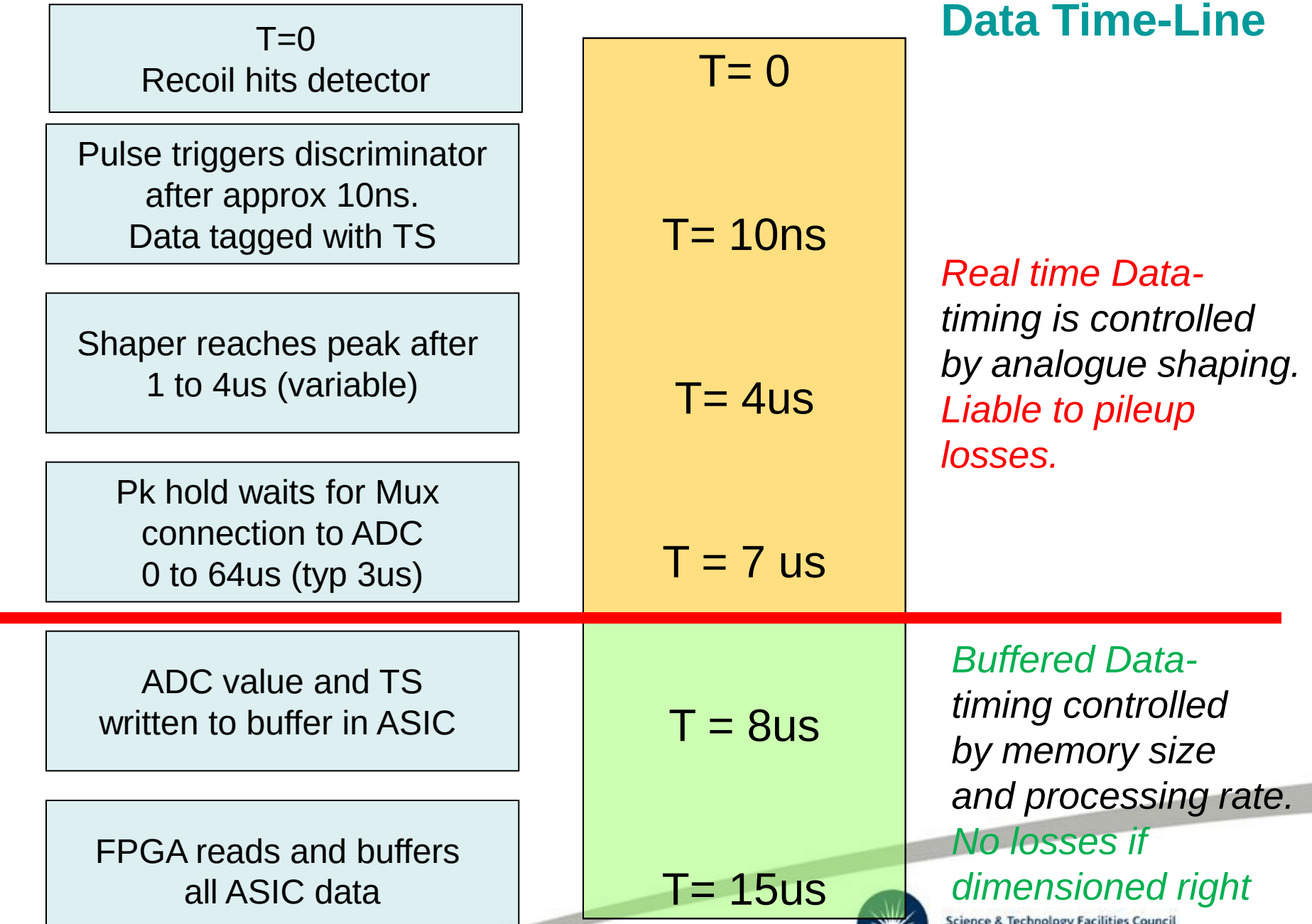
Data Time-Line



Real time Data- *timing is controlled by analogue shaping.* *Liable to pileup losses.*

Buffered Data- *timing controlled by memory size and processing rate.* *No losses if dimensioned right*

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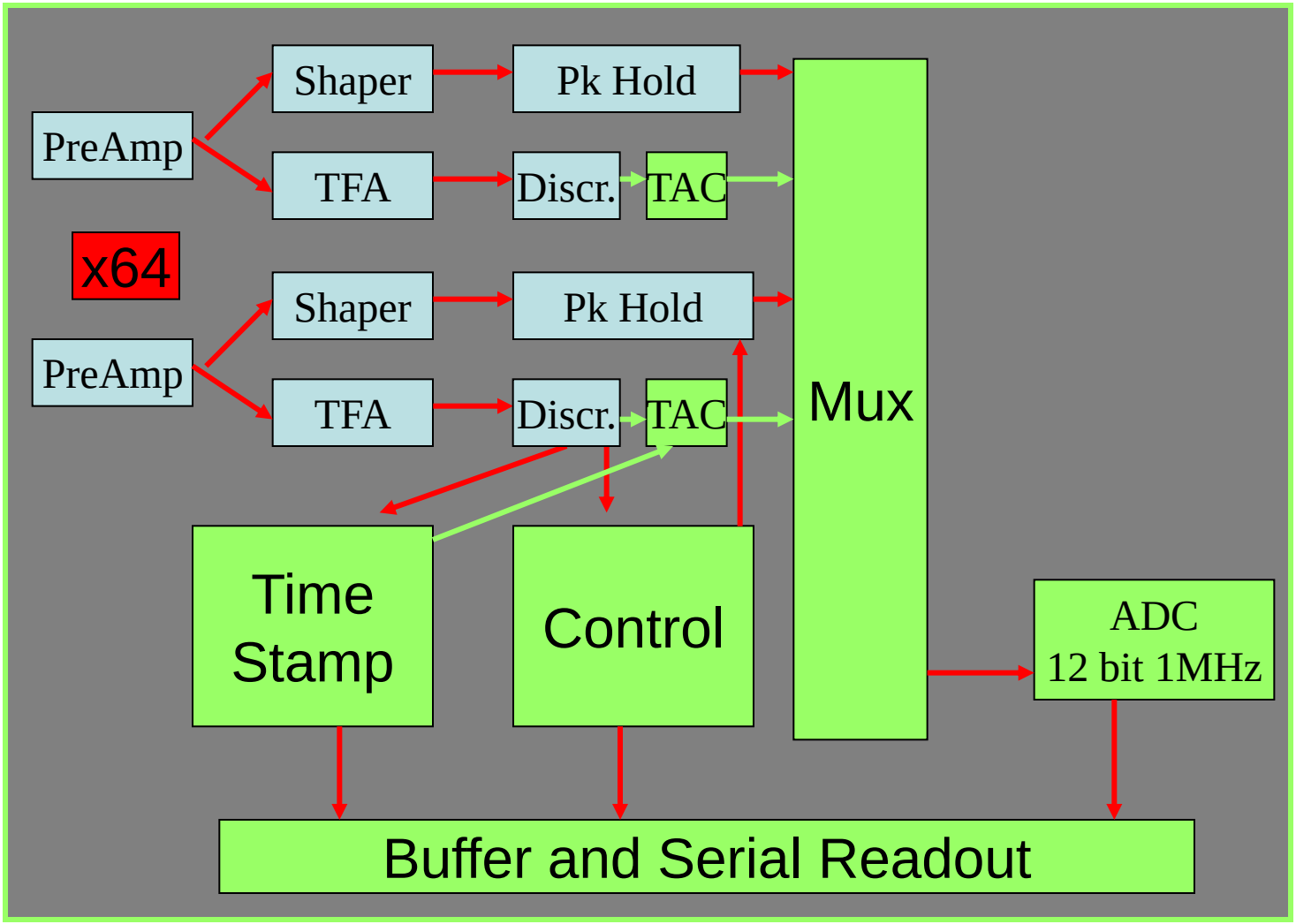
Impact of proposals on other R3B FEE/DAQ

- No hardware cross triggering.
  - Use time stamps and software triggering
  - There is no easy way to get access to discriminators inside the Si ASICs to make a timing start/stop signal- much easier to use time stamps. *(Making a time-aligned 100,000 channel analogue multiplicity or logic OR is non-trivial)*
  - For sub-TS ToF: if necessary, can add TAC/TDC to ASIC, measuring from discriminator to next TS clock pulse for fine timing. (Some or all channels?)

ASIC features:

- Time Stamp
- Zero Suppress
- On chip ADC
- TAC or TDC's?



R3B Si Tracker ASIC Proposal with TAC/TDC

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Impact of proposals on other R3B FEE/DAQ

- Rate reduction (hardware trigger).
  - Ideally, don't do it; design FEE for full data rate and DAQ to process it all. (If we can afford it!)
  - Optionally could buffer data in FEE (or DAQ input stage) and select data for collection using TS range (typically based on TS from beam trackers or beam timing). c.f. GREAT software trigger.
  - Make accept/reject decisions based on full data in DAQ, not subsystems or FEE cards with partial data.
  - Implication is that other sub-systems should also follow the time stamped DAQ philosophy.

Status of work in UK

- Funding and timescale.
  - Money for R3B has been allocated from FY 2010/11 for 5 years.
  - Start work in April 2010 (System specification & detector simulation)
  - Prototypes of individual parts due 2012
  - Assemble all prototype parts for test 2013
- Work
  - FEE and ASIC will be designed by STFC DL and RAL
  - The first step in UK work will be full simulations of the Si to be sure that we design the DAQ and ASIC to match the real final system geometry and channel count.
  - Work done already on AIDA FEE (DeSpec)- so R3B will benefit from that experience (we will re-use parts of our hardware and VHDL where possible)

R3B Si Tracker

- FEE and ASIC will be designed by STFC Daresbury and RAL
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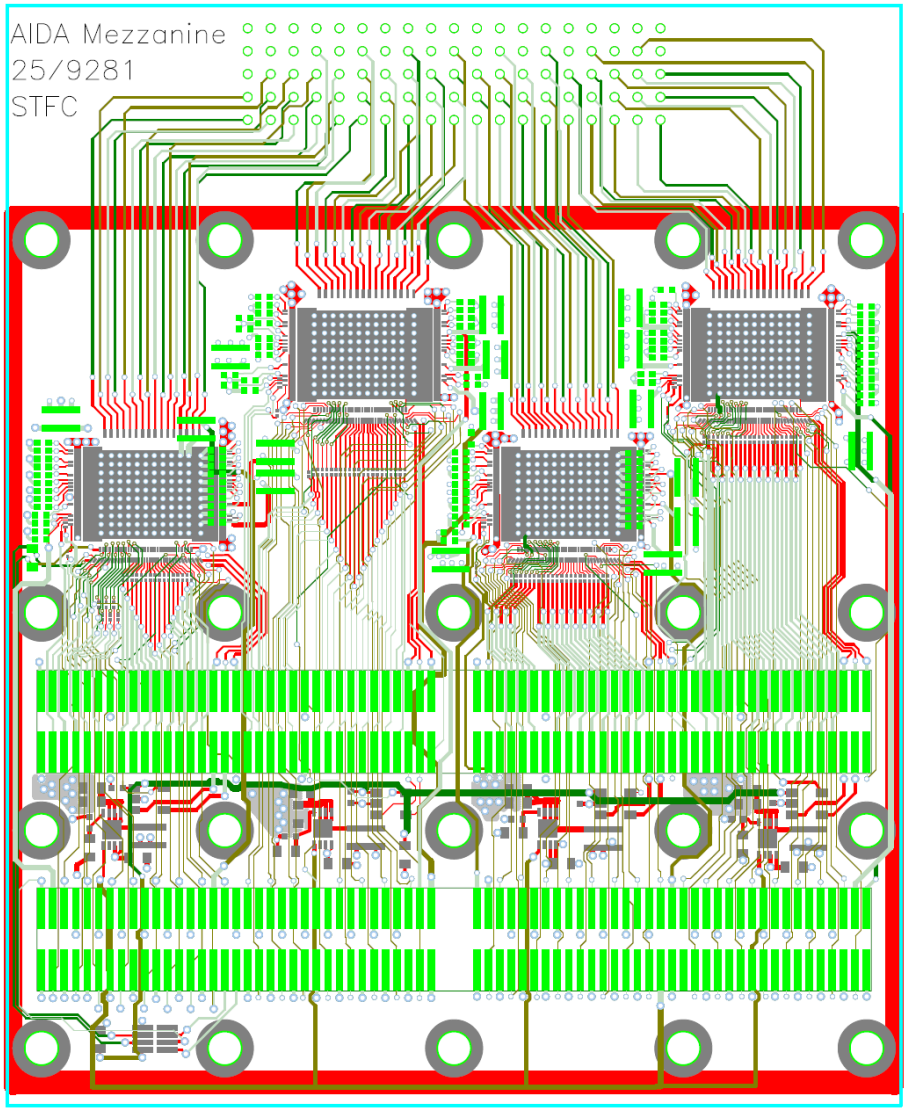
- Assemble all prototype parts for test 2013

Related work in UK

- AIDA.
  - Recoil decay tagging electronics for DeSpec
  - See talk on Monday at EXL meeting by Phil Woods
- Summary
  - ASIC designed and tested for DSSDs.
    - Quick recovery from overload (<10us)
    - 2 ranges (20GeV HE and switchable 20MeV or 1GeV LE)
    - No in-ASIC timestamps;all discriminators are connected to FEE
    - 16 channels per ASIC
  - FEE cards
    - 4 ASICs (64chan) per card
    - 64x sampling ADC, 4x 16bit ADC
    - Flexible timestamp port (BUTIS/white rabbit, GREAT, simple clock)
    - Gbit Ethernet readout
    - Ethernet slow control

Prototype AIDA Mezzanine Routing



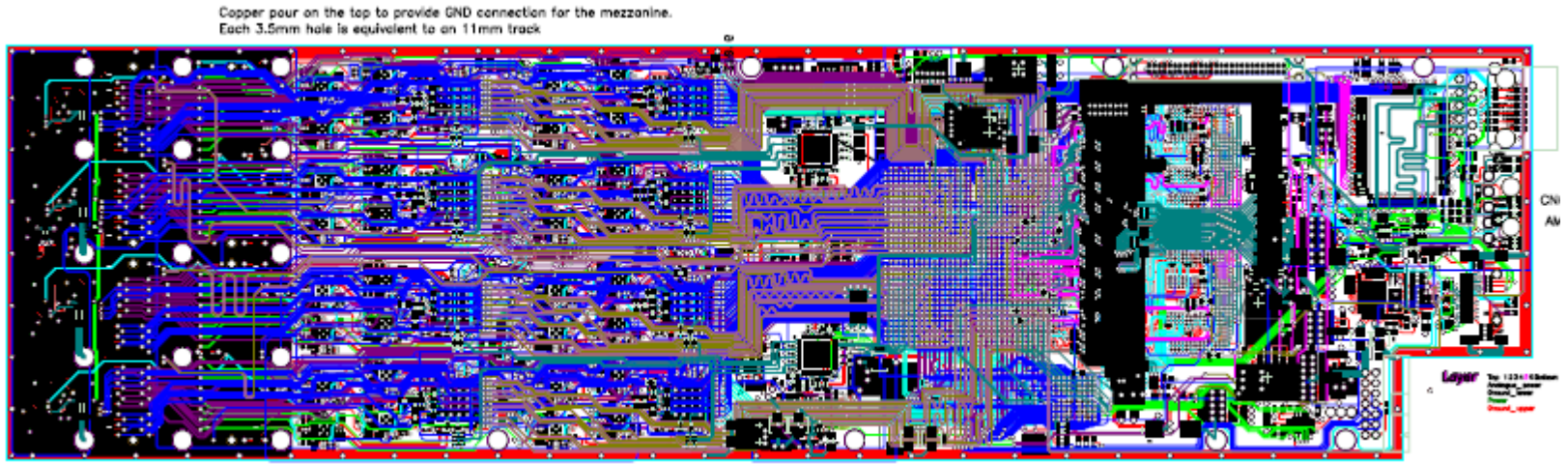
- 4x AIDA ASICs
  64 channels
- One mezzanine (4 ASICs) per FEE card

Prototype AIDA FEE card Routing

Digital readout

FPGA, Memory, Gbit

Multiplex readout



Connectors for Mezzanine

Clock distribution

Power Supplies

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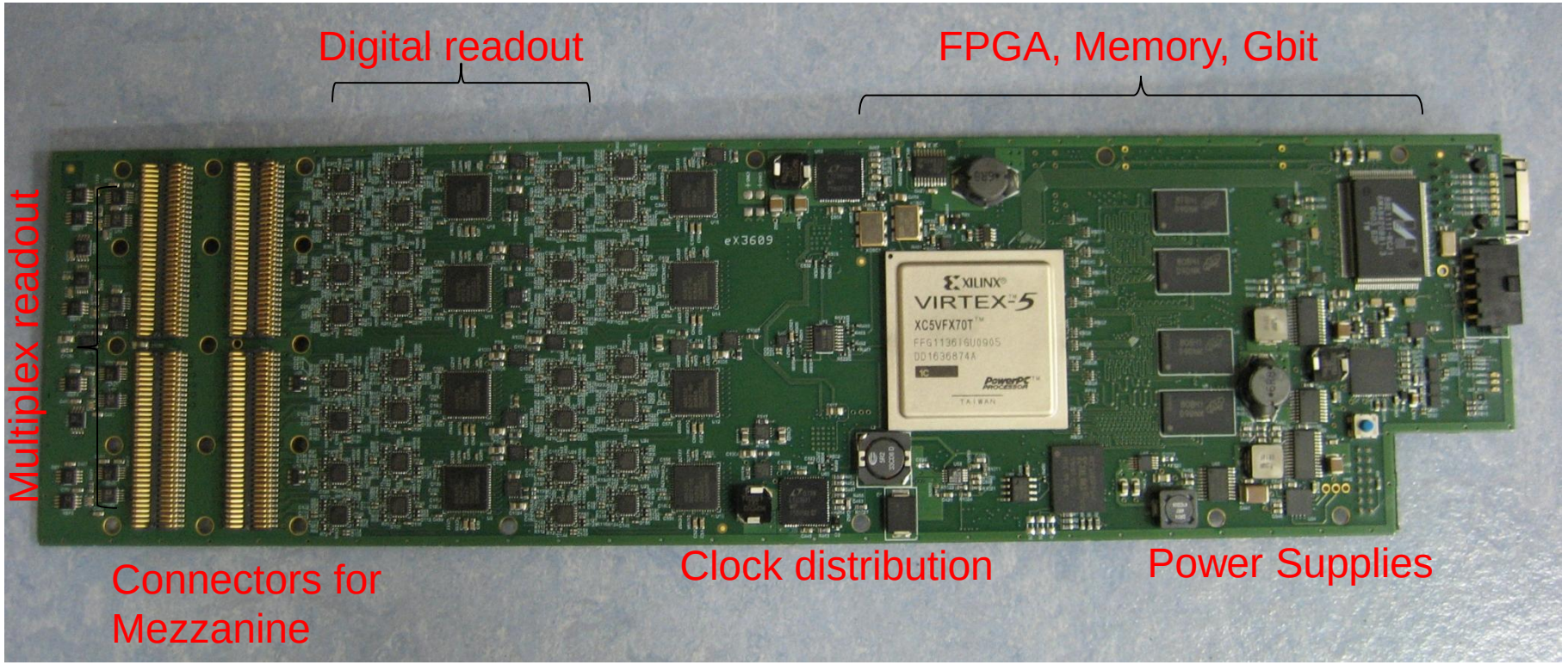
Prototype AIDA FEE card



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