A new Si tracking detector for R^3B experiment at FAIR

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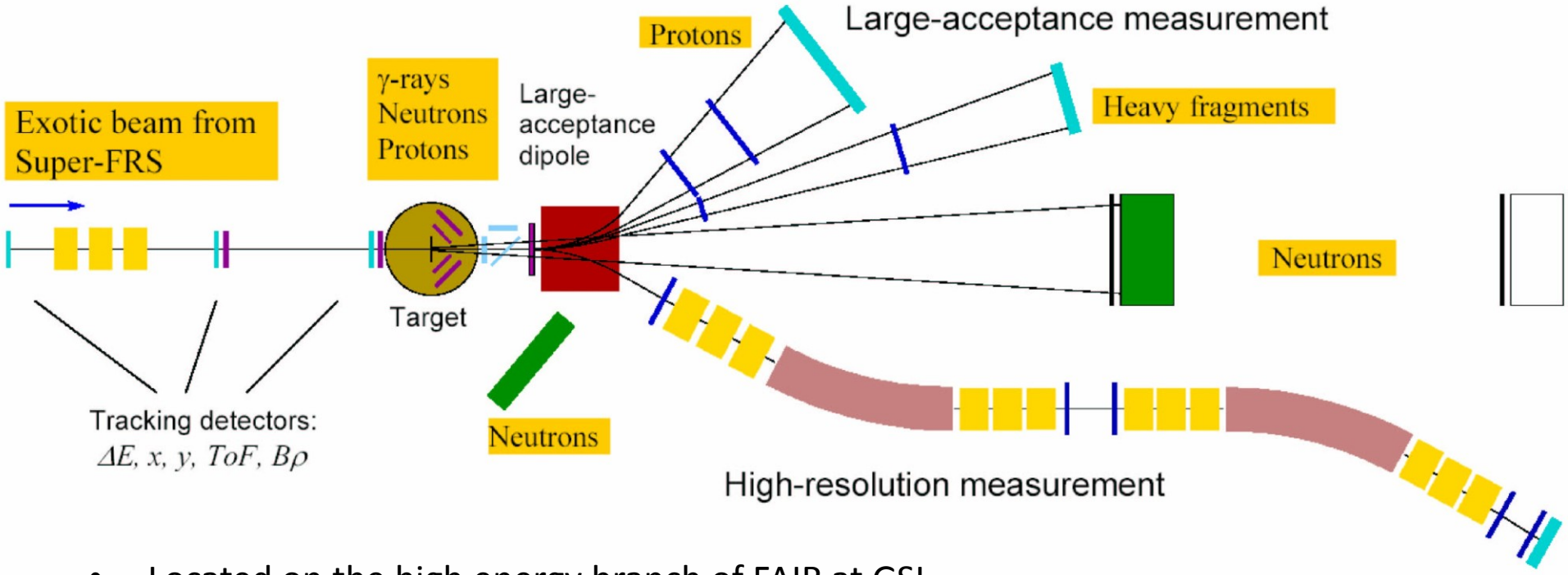
Overview

- Overview of R^3B project
- Design constraints from simulations
- Design and electronics of the Si tracker
  - Mechanical design of detector and target
  - Electronics
  - Overall fit into the R3B experiment
- Simulations of (p,2p) including Calorimeter
- Summary

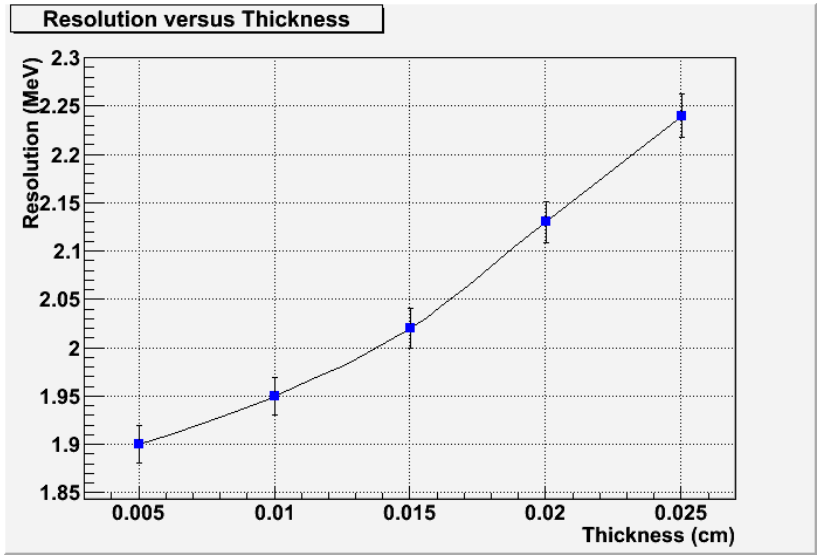
R^3B experiment

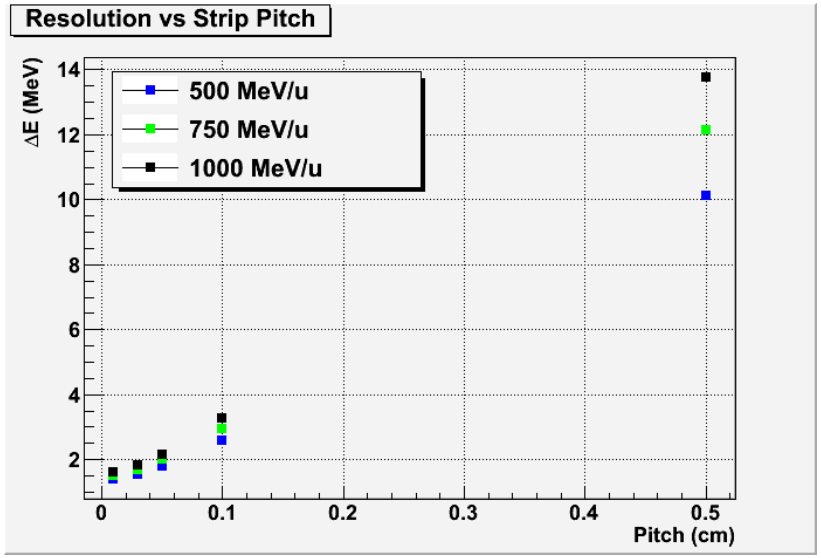


- Located on the high energy branch of FAIR at GSI.
- Detection of all reaction channels.
  - Study of nuclear and astro-physical reactions
- Main reactions of interest are quasi-free scattering reactions with hydrogen target
  - (p,2p), (p,pn), (p,pα), etc

Design constraints for Si detector

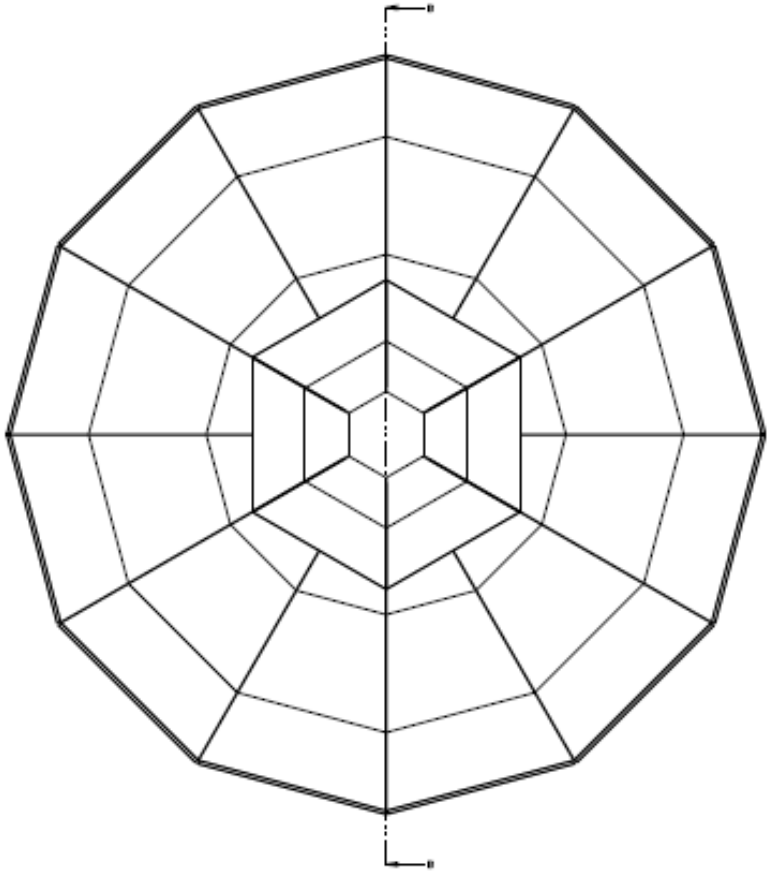
- Must detect protons at most forward angles
- Inner layer as thin as possible
- At least 3 layers
  - Strip redundancy
- Inner layer as close to target as possible
  - Accurate determination of reaction vertex
- No shielding between detector and target





“Lampshade” design

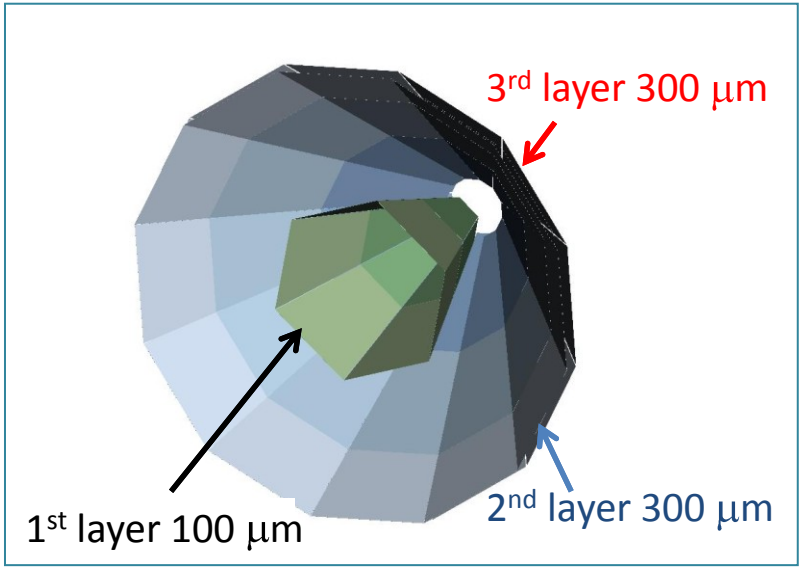
View from beam direction

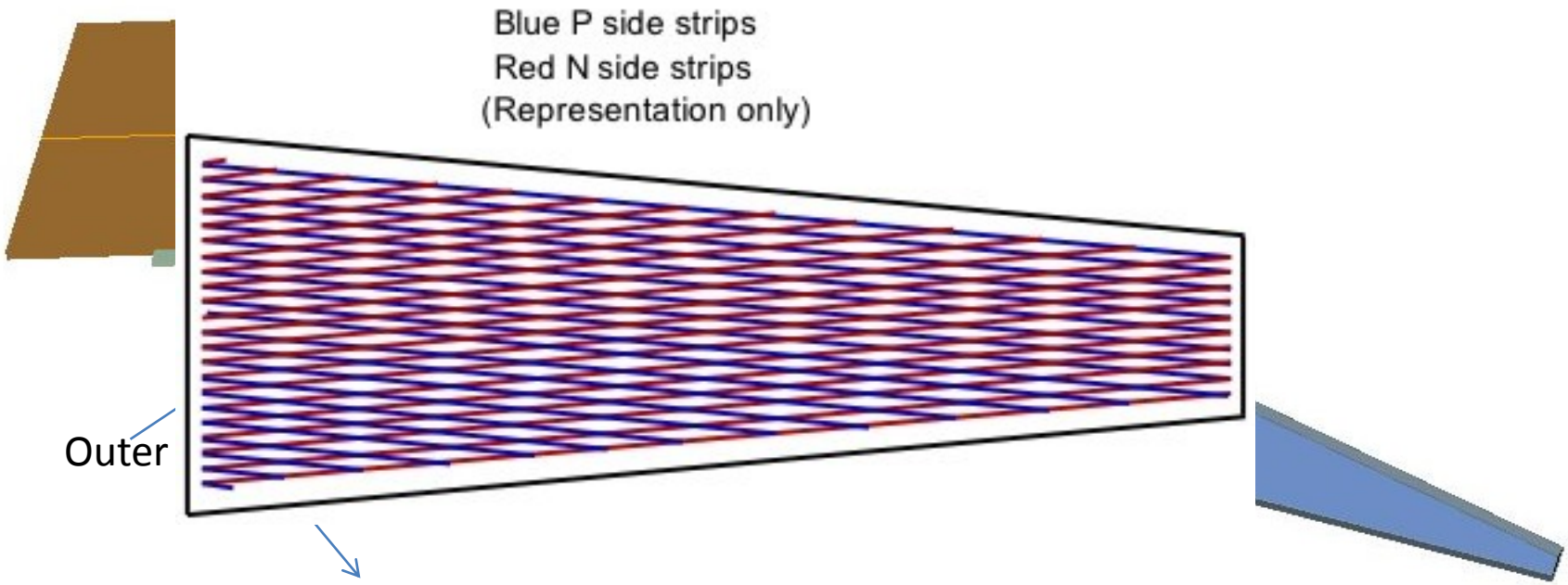


The inner detector module (green) has 6 detector modules, each with 2 silicon wafers.

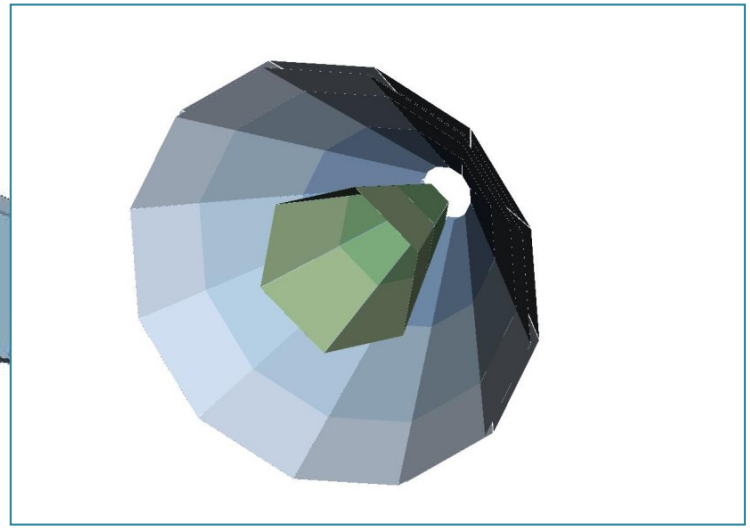
The outer detectors (blue) are formed from 2 layers of 12 detector modules, each with 3 silicon wafers.

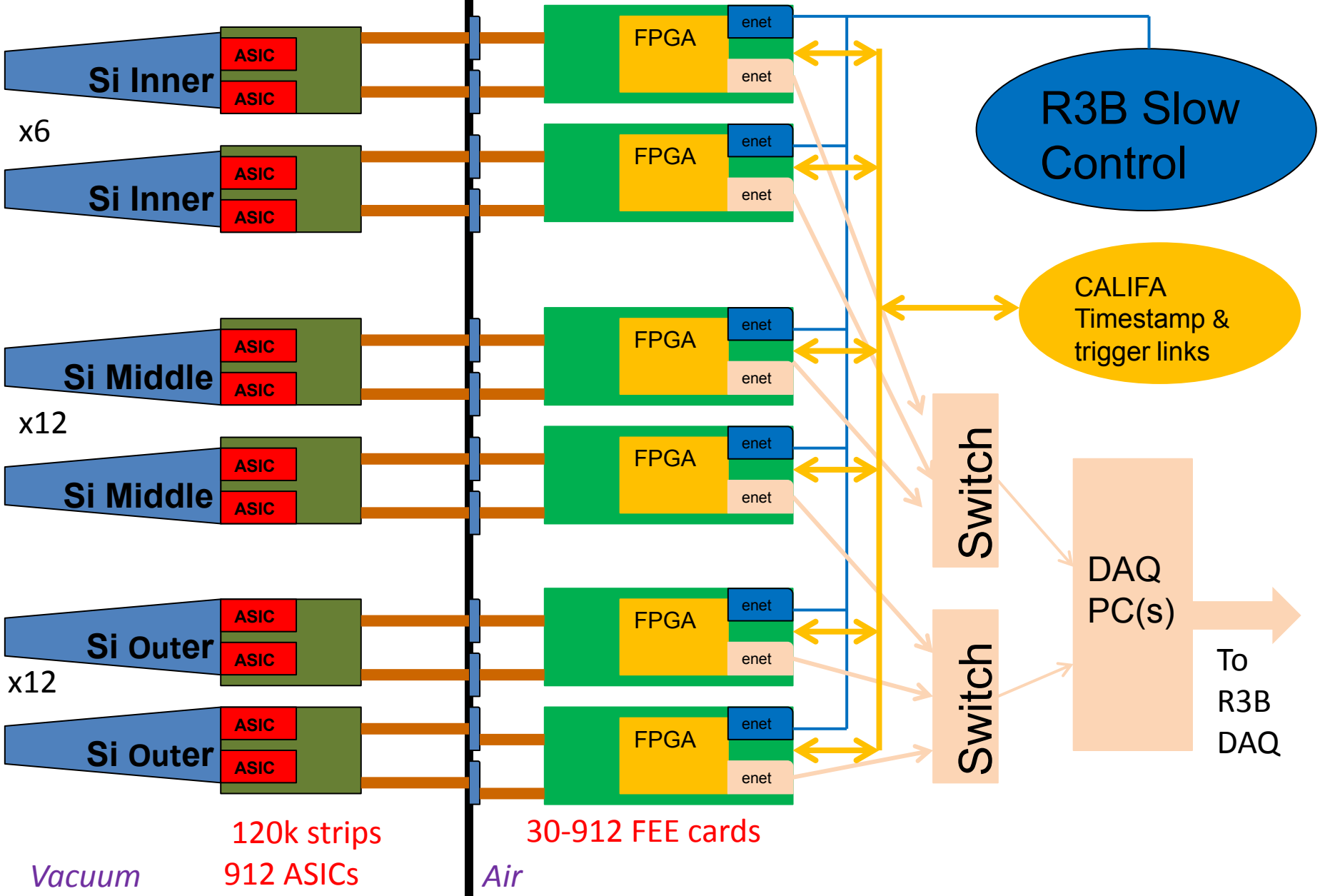
Manufacturing masks are shared between one of the outer and inner detector modules slices to reduce costs.



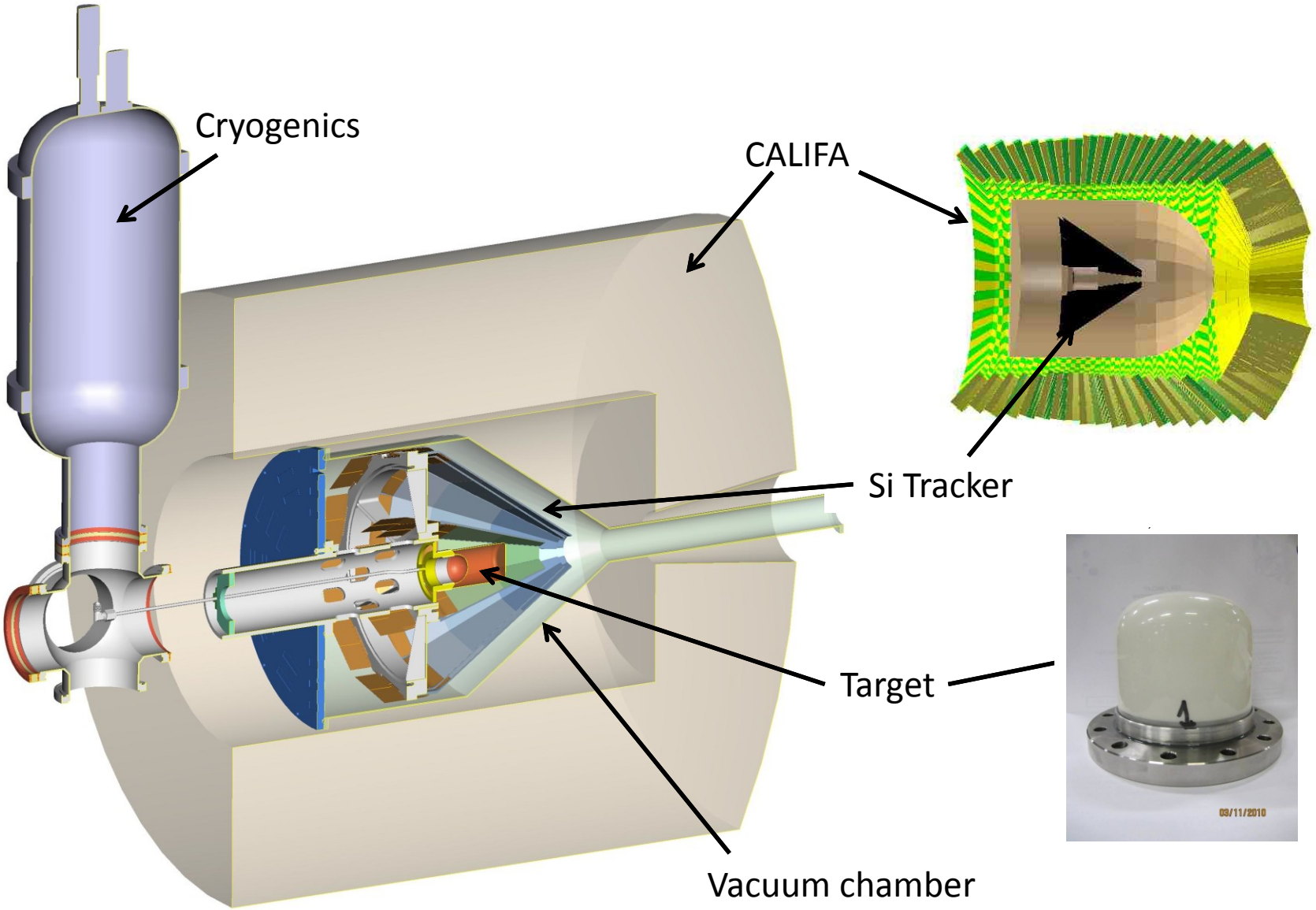


- Strips are stereoscopic rather than perpendicular strips
  - Reduced capacitance due to non-metalisation
  - Diamond shaped pixels
  - 50μm pitch
- Inner layer
  - Max distance from beam axis = 69 mm
  - Tilt angle = 14°
- Outer layers
  - Max distance from beam axis = 194/196 mm
  - Tilt angle = 33°

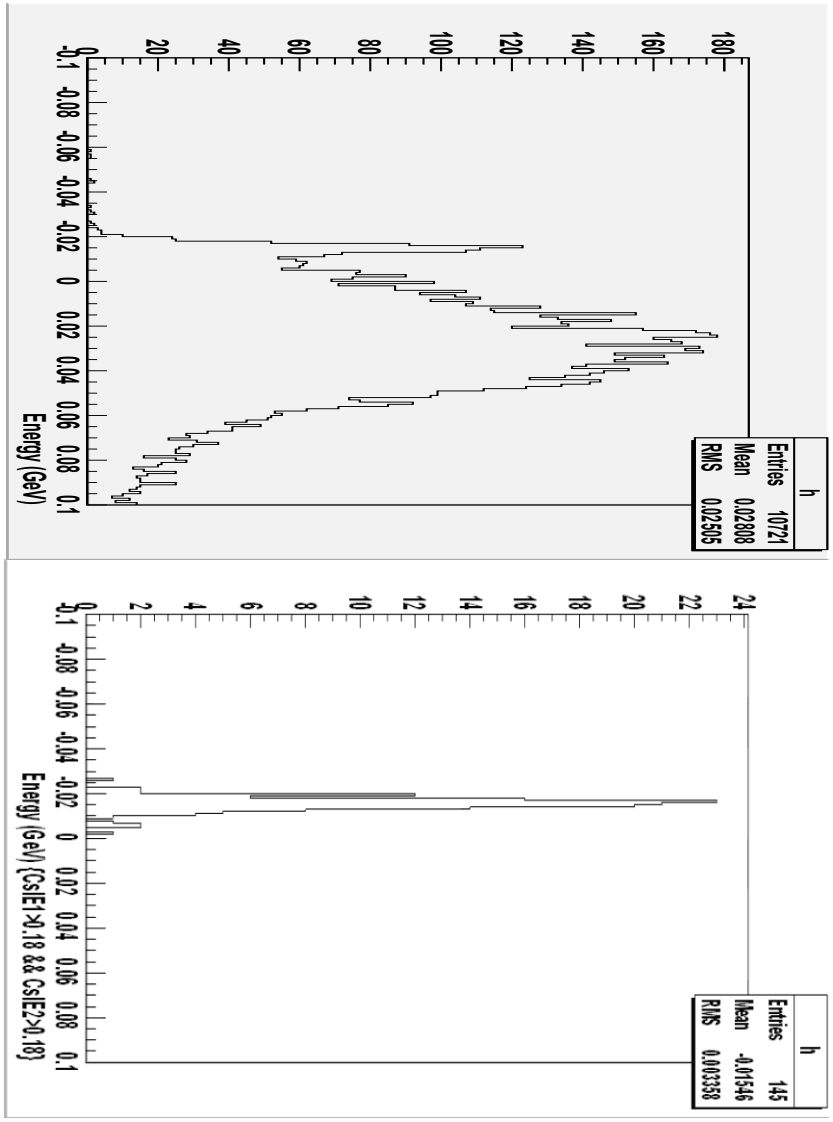



Si Inner
ASIC
ASIC
x6
Si Inner
ASIC
ASIC
Si Middle
ASIC
ASIC
x12
Si Middle
ASIC
ASIC
Si Outer
ASIC
ASIC
x12
Si Outer
ASIC
ASIC
FPGA
enet
enet
FPGA
enet
enet
FPGA
enet
enet
FPGA
enet
enet
FPGA
enet
enet
FPGA
enet
enet
R3B Slow Control
CALIFA Timestamp & trigger links
Switch
Switch
DAQ PC(s)
To R3B DAQ
120k strips
912 ASICs
30-912 FEE cards
Vacuum
Air

Mechanical Design

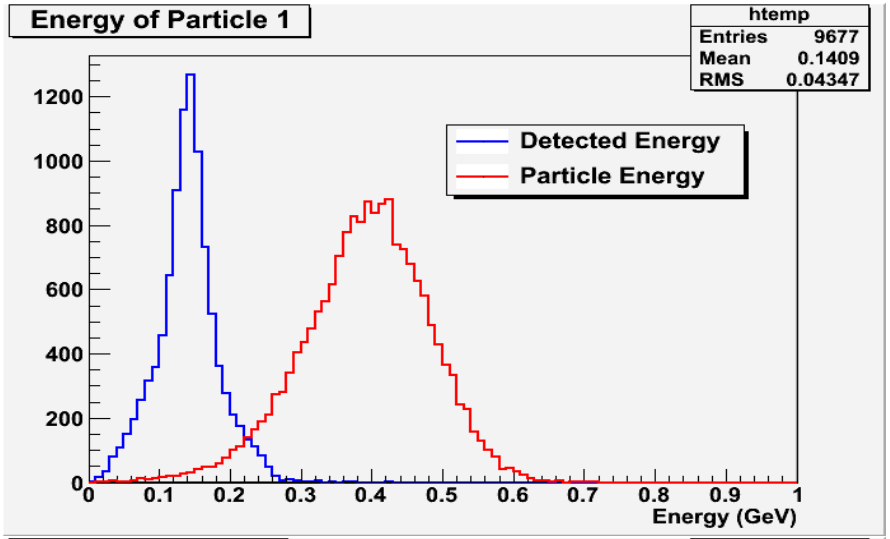


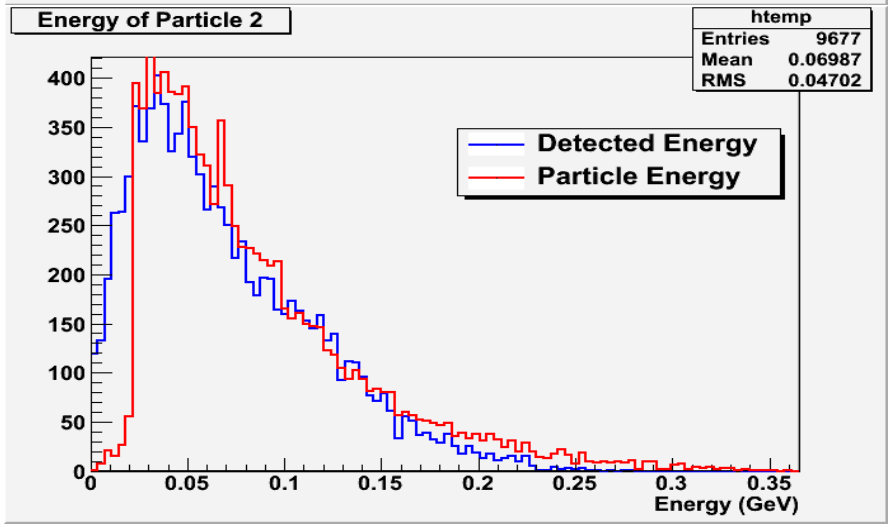
Lampshade resolutions with CALIFA



- Separation energy calculated by Si + CsI energies.
- Background from protons punching through CALIFA.
- Gate on highest energy CsI energies to cut out background
- ΔEsep = 2.8 MeV
- Eff(m>=2) = 71%

Background Contribution





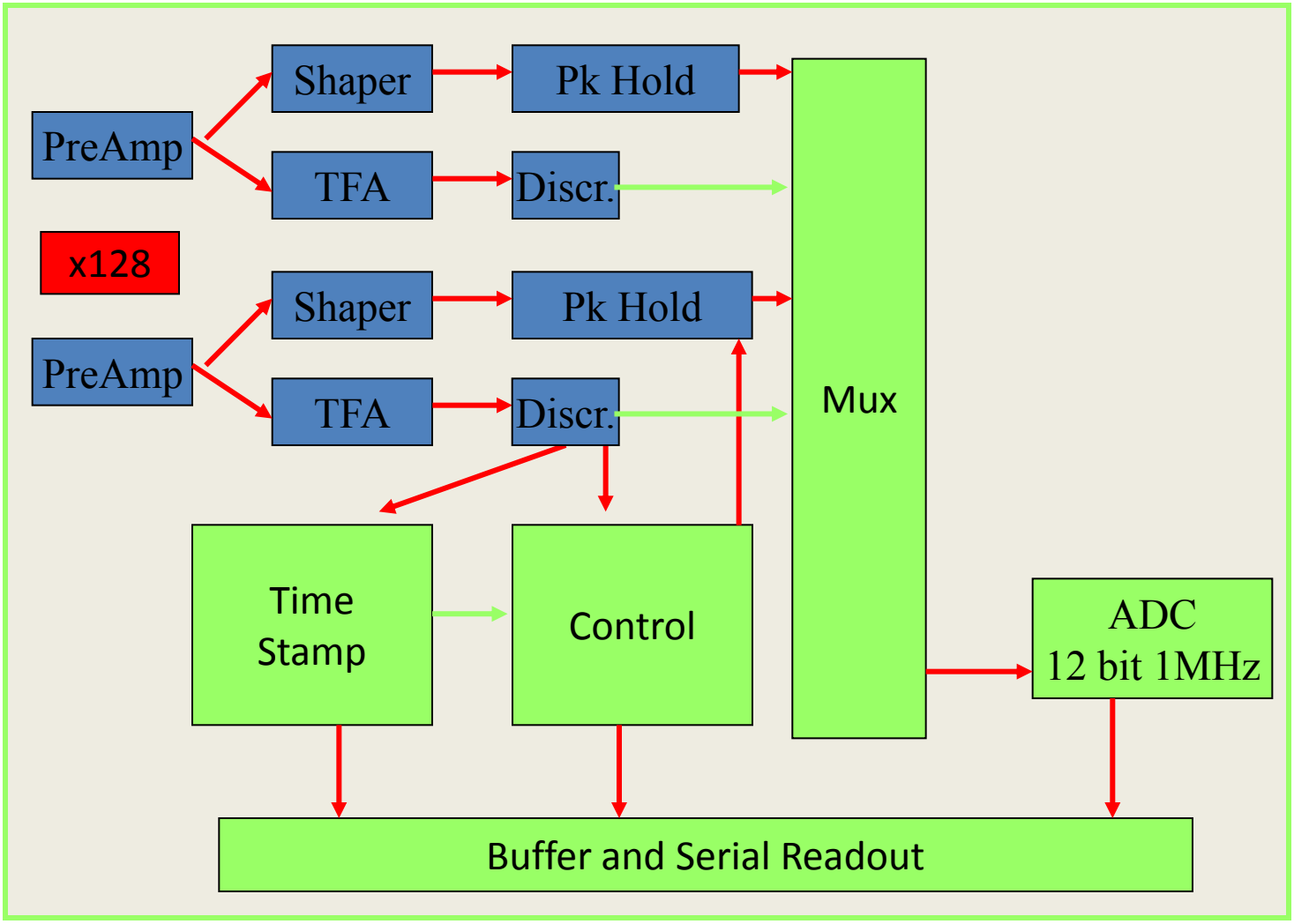
- Energy profile of particle 1 does not look like detected energies, whereas particle 2 does.
- Detected energies dominated by CsI energy peak at 0.15 GeV.
- Proton punch through ~275 MeV
- Recovery of events needed or use non-punch through protons/fragment to determine Q-value.

Summary

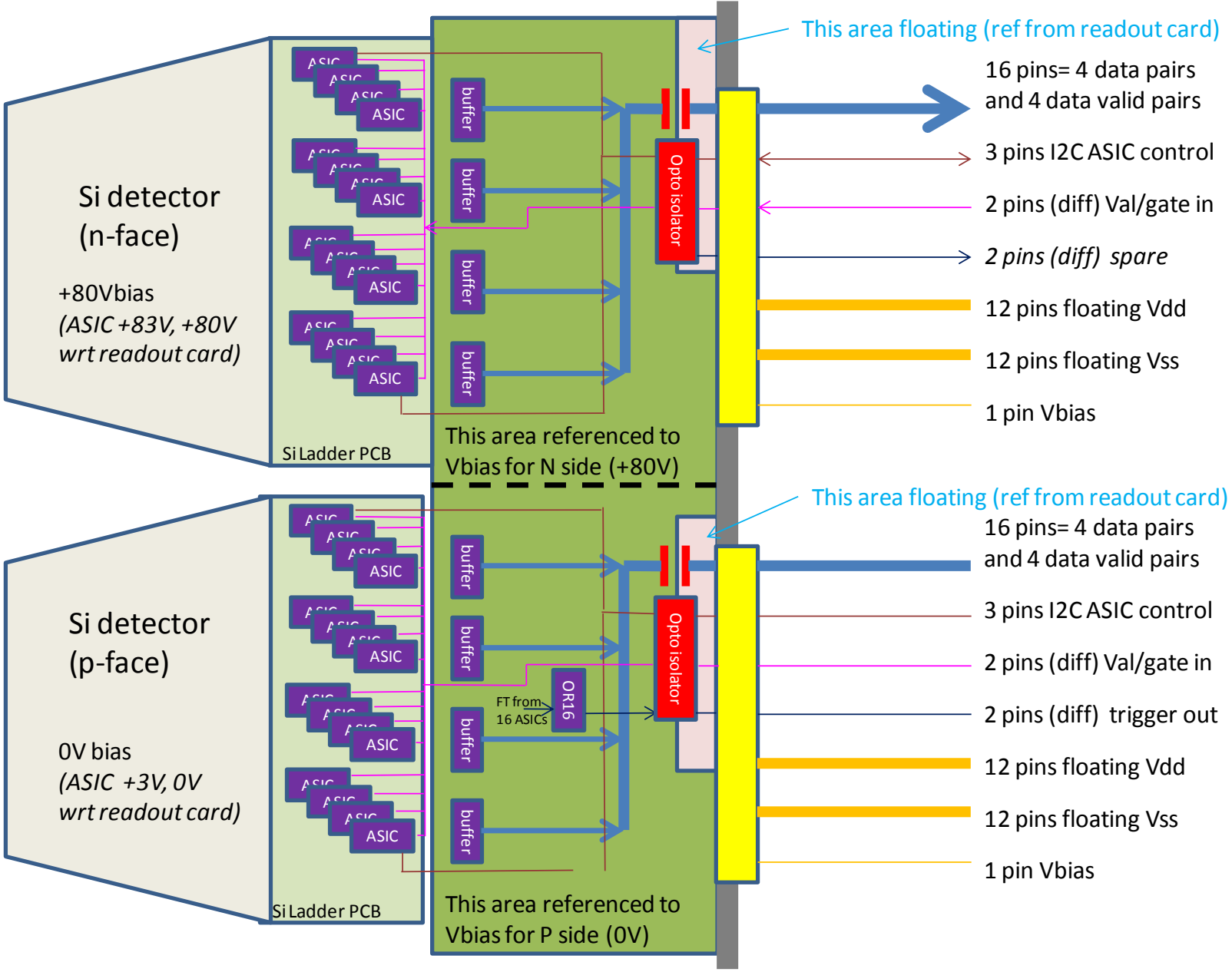
- New Si tracking detector for R^3B designed and near start of prototyping phase.
- Simulations of (p,2p) and elastic scattering used to inform design of new detector
  - Good separation energy and position resolution
  - Resolution and efficiency, however, dominated by calorimeter
- Electronics design nearing competition
  - Stand alone or integrated into R^3B DAQ
- All deadlines being met for completion in 2015

ASIC features:

- Time Stamp
- Zero Suppress
- On chip ADC
- NO TAC (we have found no ToF requirement)



R3B Si Tracker ASIC new proposal without TAC


Si detector
(n-face)
+80Vbias
(ASIC +83V, +80V
wrt readout card)
ASIC
buffer
Opto isolator
Si Ladder PCB
This area referenced to
Vbias for N side (+80V)
This area floating (ref from readout card)
16 pins= 4 data pairs
and 4 data valid pairs
3 pins I2C ASIC control
2 pins (diff) Val/gate in
2 pins (diff) spare
12 pins floating Vdd
12 pins floating Vss
1 pin Vbias
Si detector
(p-face)
0V bias
(ASIC +3V, 0V
wrt readout card)
FT from
16 ASICs
OR16
Si Ladder PCB
This area referenced to
Vbias for P side (0V)
This area floating (ref from readout card)
16 pins= 4 data pairs
and 4 data valid pairs
3 pins I2C ASIC control
2 pins (diff) Val/gate in
2 pins (diff) trigger out
12 pins floating Vdd
12 pins floating Vss
1 pin Vbias