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AGATA Electronics

Overview of talk

- AGATA at LNL
- Electronics needed for gamma ray tracking
- System overview
- Digitisers
- Pre-processing
- GTS
- Results
- Software
- Connecting other experiments to AGATA
- International collaboration

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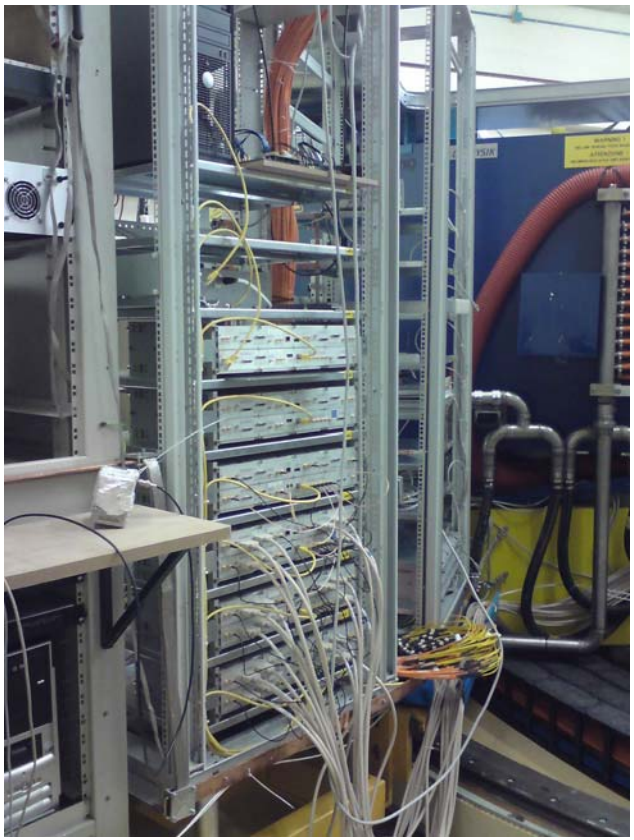

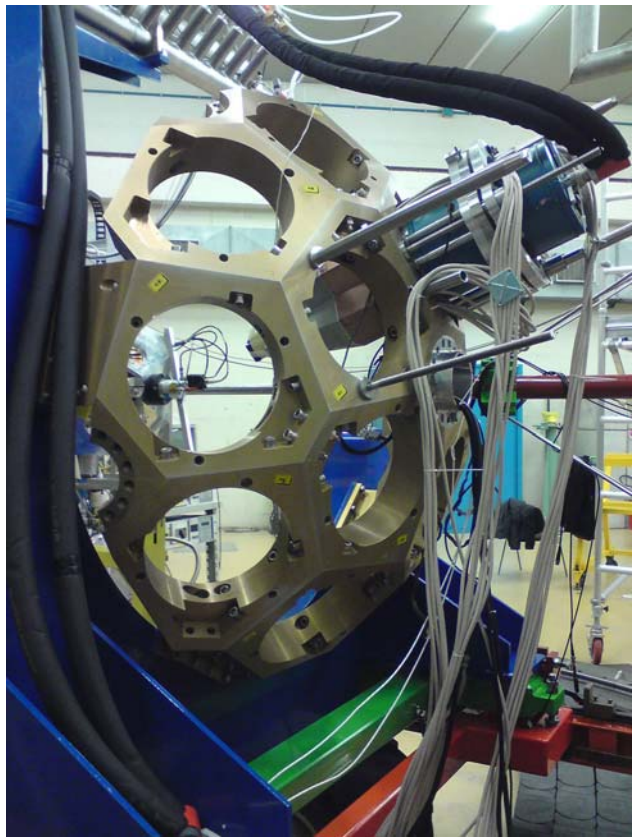

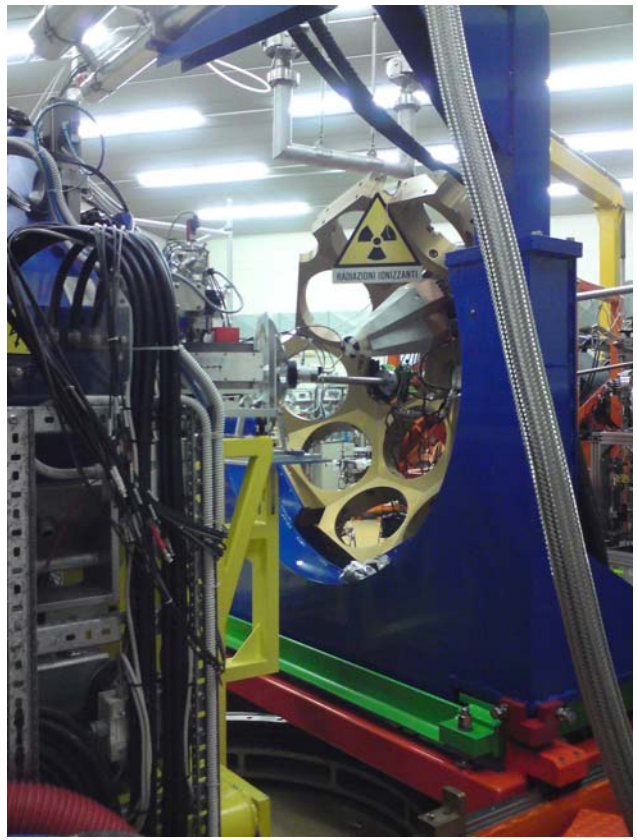

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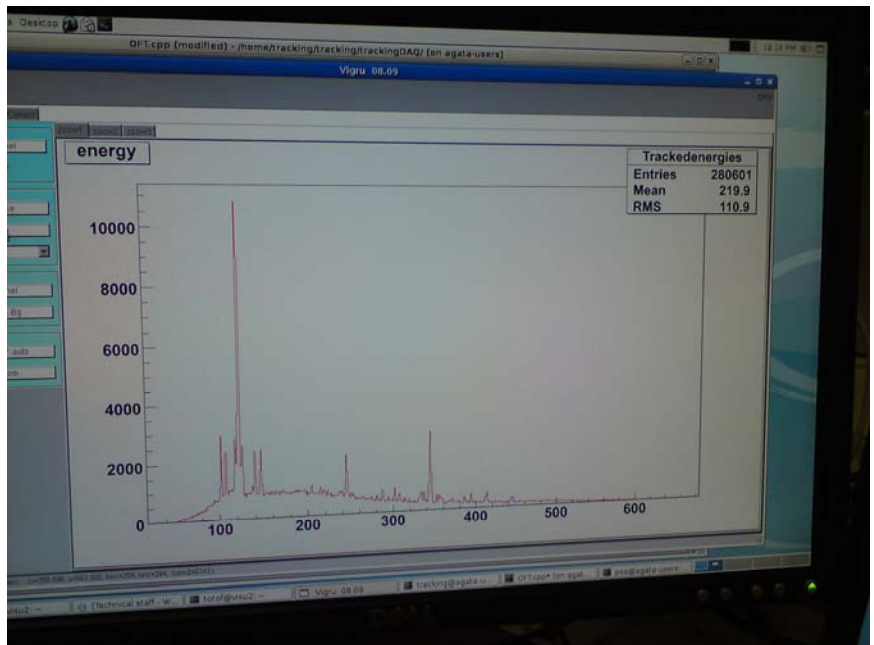

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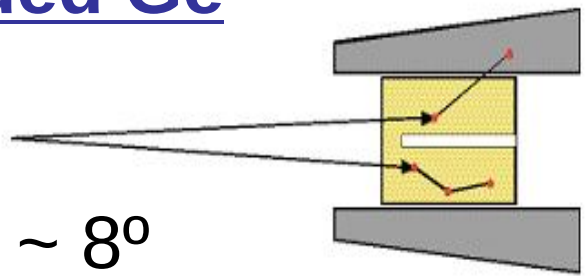
Idea of γ-ray tracking

Compton Shielded Ge

ε_{ph} ~ 10%

N_{det} ~ 100

Ω ~40%



θ ~ 8°

large opening angle means poor energy resolution at high recoil velocity.

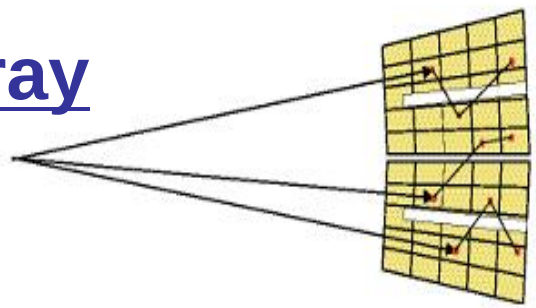
Previously we had to waste scattered gammas. Technology is available now to track them..

Ge Tracking Array

ε_{ph} ~ 50%

N_{det} ~ 100

Ω ~80%



θ ~ 1°

Combination of:

- segmented detectors
- digital electronics
- pulse processing
- tracking the γ-rays

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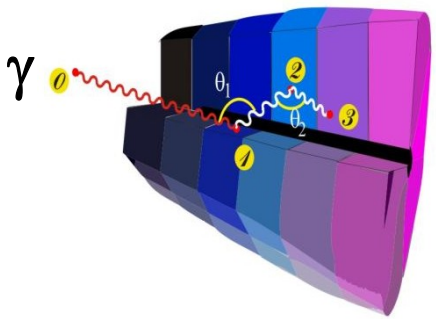
Ingredients of γ-Tracking

1

Highly segmented HPGe detectors



2

Digital electronics to record and process segment signals

3

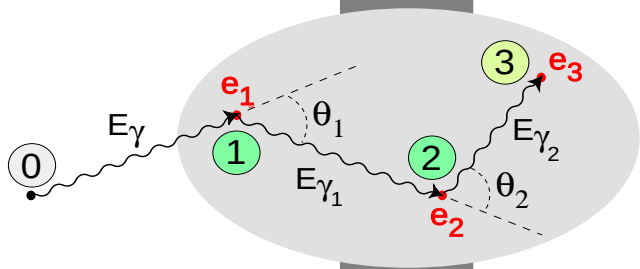
Pulse Shape Analysis to decompose recorded waves

4

Identified interaction

$(x,y,z,E,t)_i$

Reconstruction of tracks e.g. by evaluation of permutations of interaction points



reconstructed γ-rays

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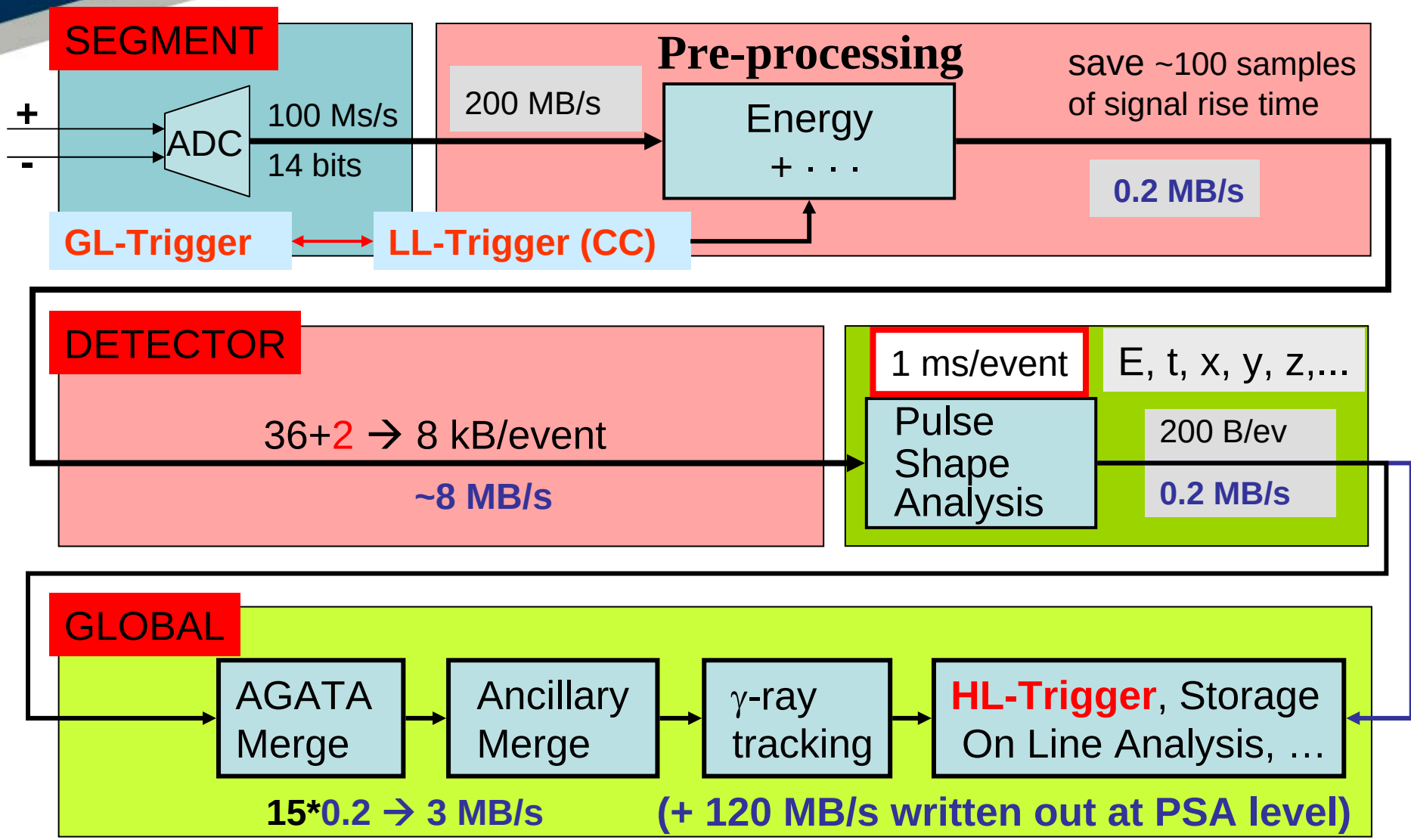
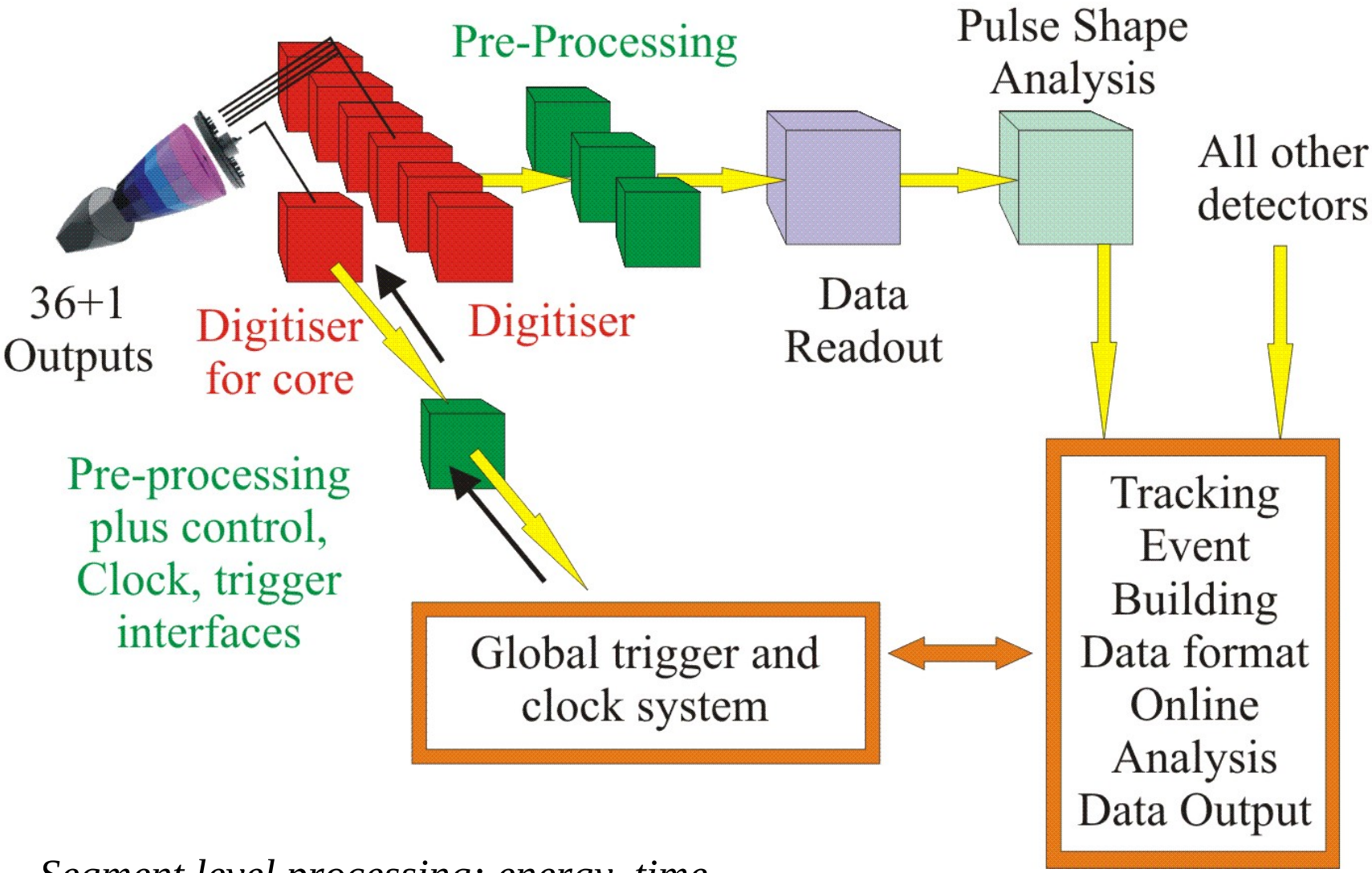
Initial Data rates for Demonstrator

15 detectors, 10 kHz singles, GL-trigger, Ancillary → **1 kHz into PSA**



Initially traces will be recorded for off-line validation

Schematic of the Digital Electronics and Data Acquisition System for AGATA



Segment level processing: energy, time
Detector level processing: trigger, time, PSA
Global level processing: event building, tracking, software trigger, data storage

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AGATA Digitiser

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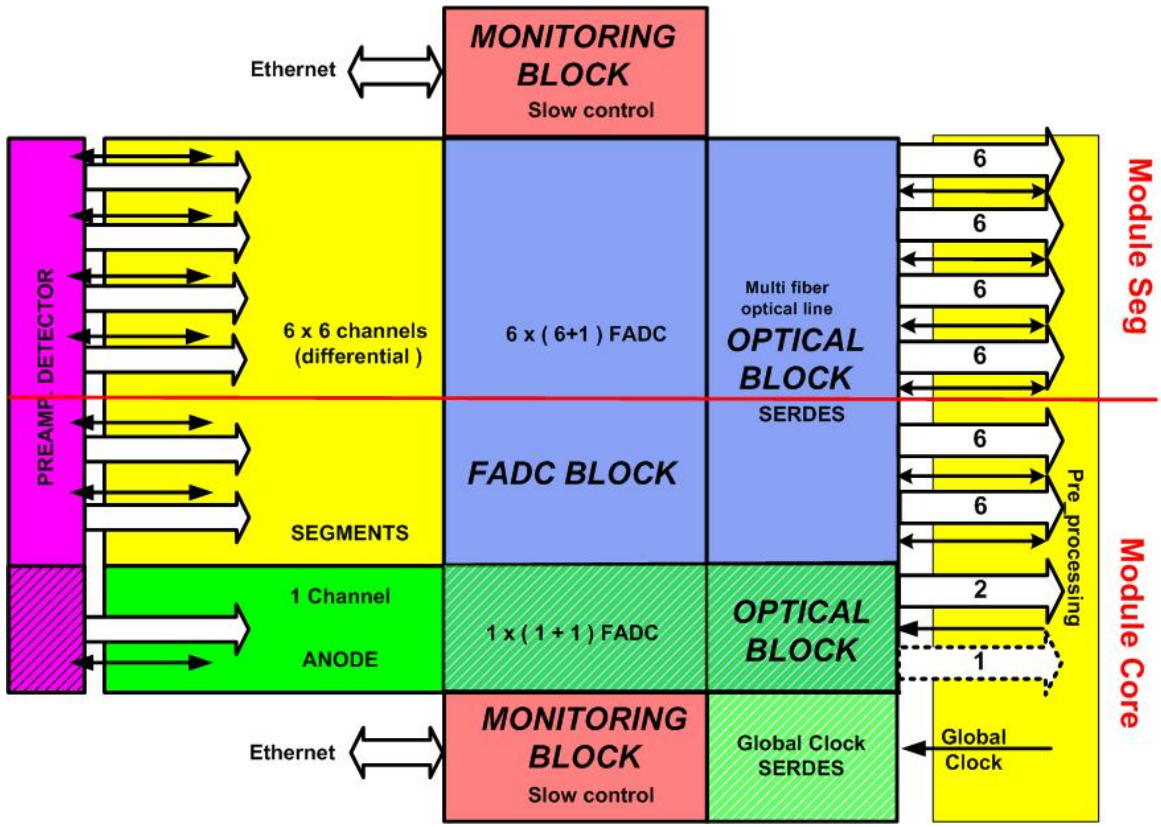
Digitiser Block Diagram

- **44 Channels 100 MHz/14 bits.**
- **38 Optical lines 2Gbits/s.**
- **400 W Power.**
- **Cooling by water.**
- **Specific Mechanical Housing.**
- **Ethernet for Slow Control.**



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AGATA Digitiser Module

36 segments, 1 core, 7 spare= 44 channels
each channel 100 MHz, 14 bits
(Strasbourg - Daresbury – Liverpool)

- Mounted close to the Detector *5-10 m*
- Power Dissipation around 220W
- Water Cooling required
- Testing in Liverpool (December 2006)
- Production in progress (for 18 modules)

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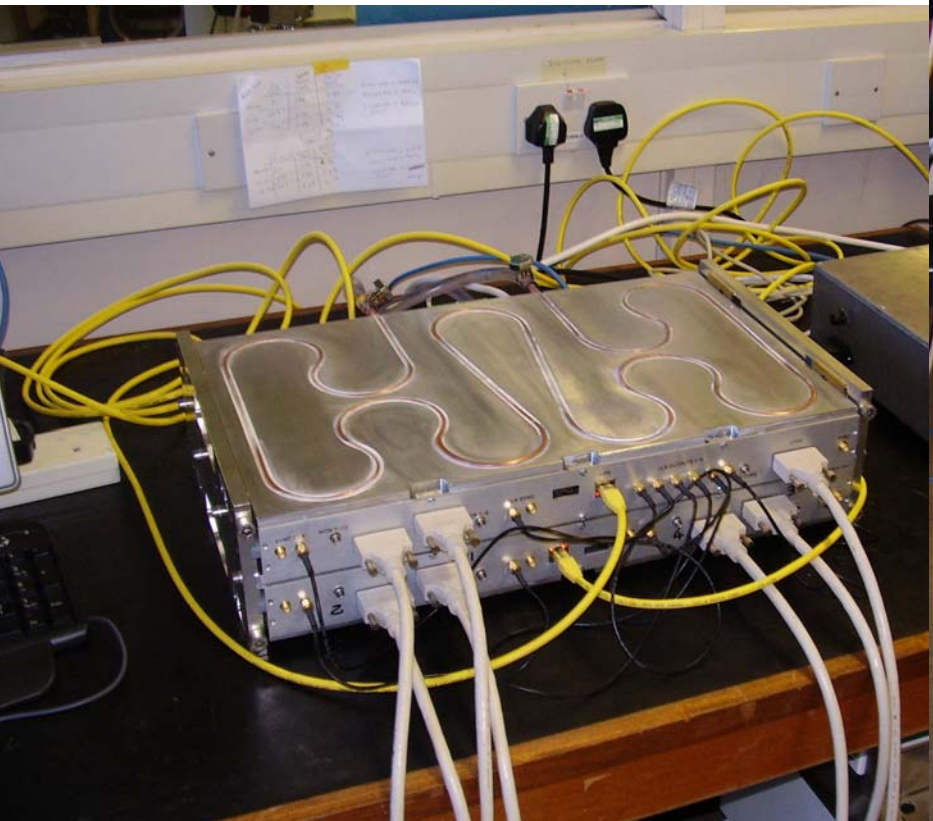
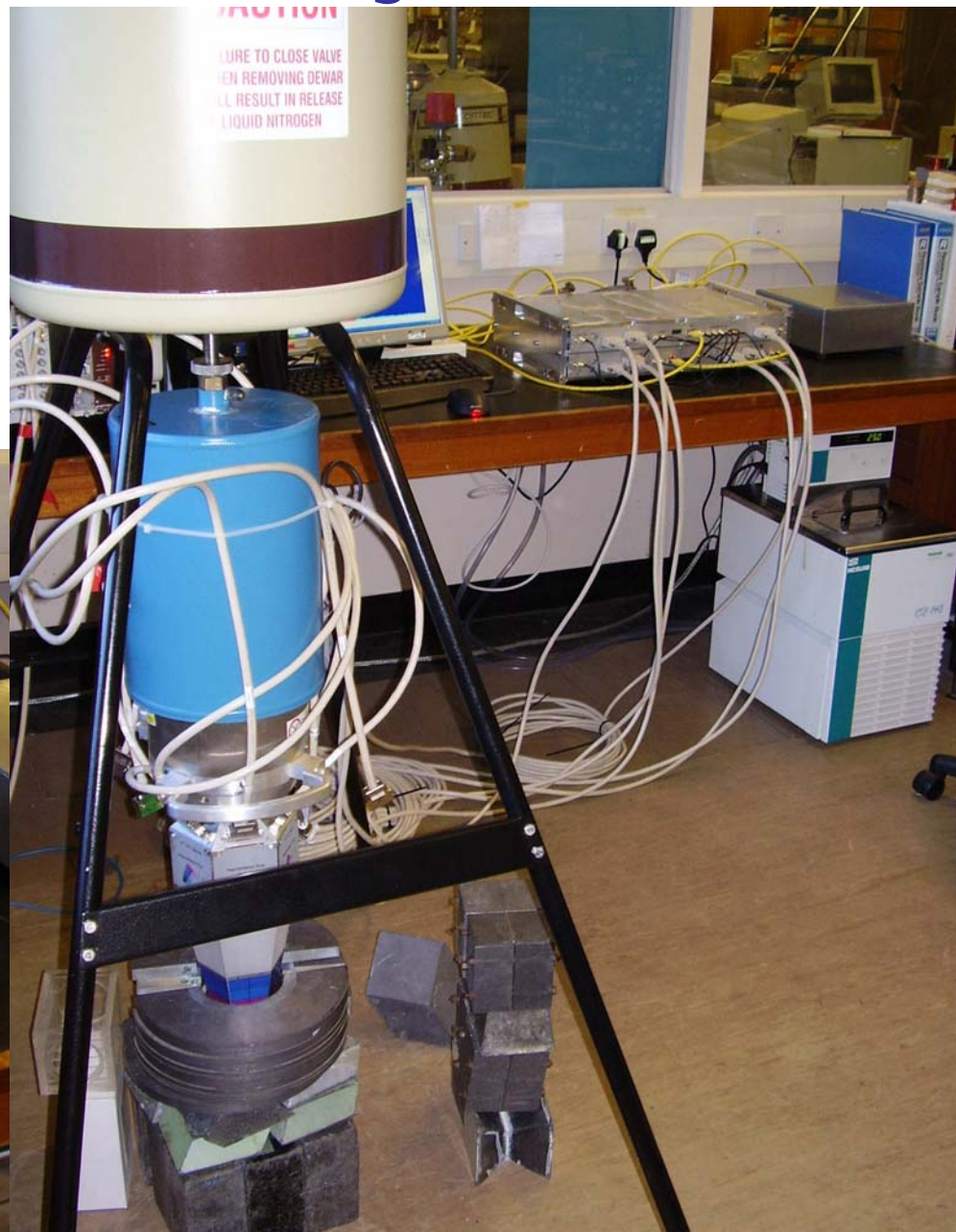
Digitiser & detector





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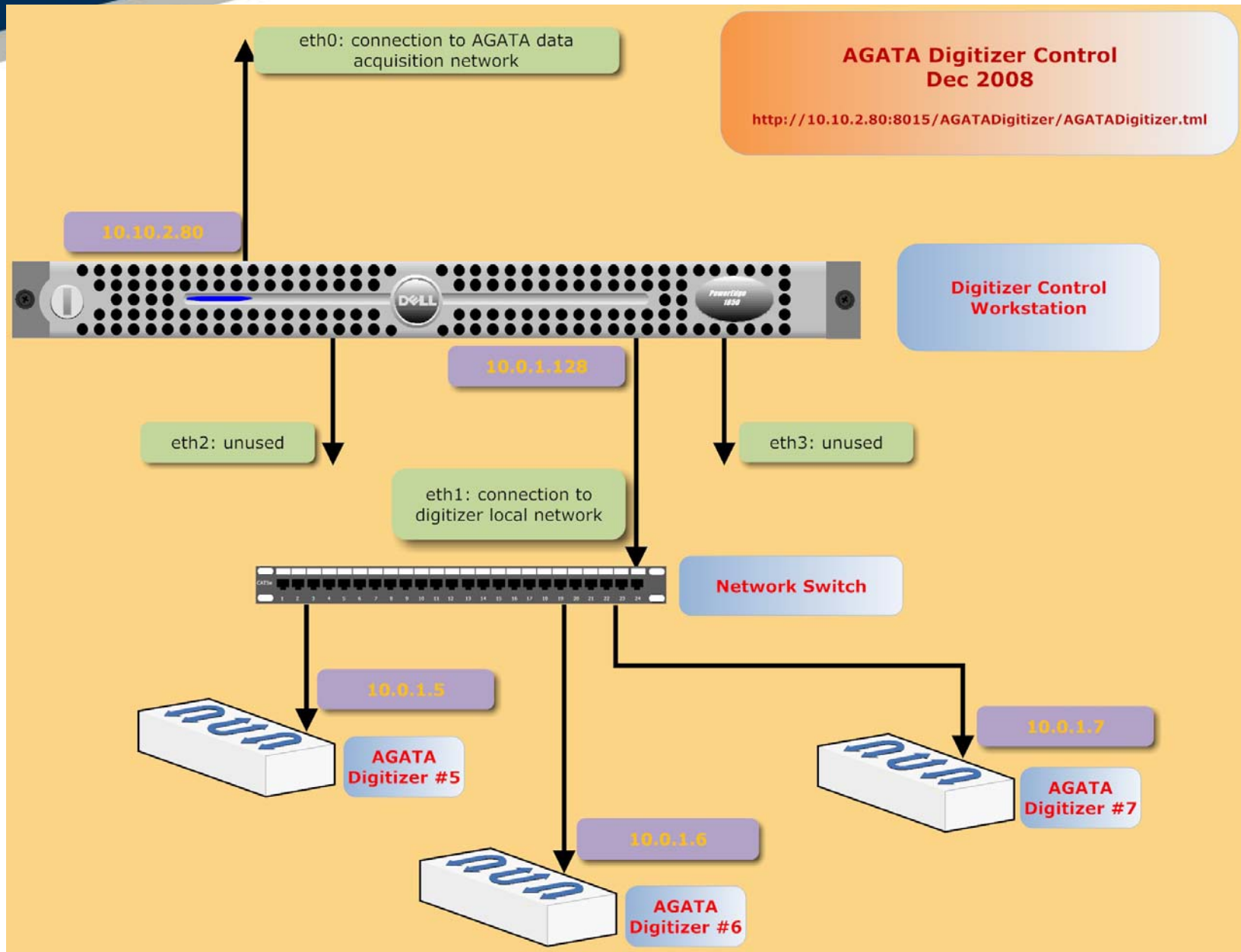
Digitiser Slow Control



AGATA Digitizer: Control

Select Hardware

Digitizer 6 | FPGA: Core: Main Board | Select | Probe Digitizer Hardware | Read PROM

Select Detector/Crystal/Segment

Detector 00 | Crystal G | Segment I | Select

Restore all digitizer offsets from the DataBase | Save all digitizer offsets to the DataBase

Setup

SetUp Current FPGA | SetUp Current Digitizer | SetUp All Digitizers

Check Current Digitizer | Check All Digitizers

```
Segment: Virtex for Segment ADC card 4
Segment: Virtex for Segment ADC card 3
Segment: Virtex for Segment ADC card 2
Segment: Virtex for Segment ADC card 1
Segment: Main Board
Core: Virtex for Segment ADC card 2
Core: Virtex for Segment ADC card 1
Core: Virtex for core ADCs
Core: Main Board
Found Digitizer 6 which consists of:
found it
probing for Segment ADC card #4
```

Empty Log Window | Send Log Window to ELog | Reload | Reset | Show Variables | Hide Log Window | Enable Logging

Core Preamp Pulser Control | Data Communications Control | Temperature Monitoring | Digitizer Diagnostics

Hardware Configuration

Last Updated: February 17, 2009 12:03:44

Digitiser Upgrade

- Upgrade control card to run web server inside the digitiser.
- Other possible work:
  - Change 14bit ADC to 16bits (if input signal is good via MDR is good enough to see improvement)
  - Squeeze into small packaging (if we can do so without compromising the analogue input performance)

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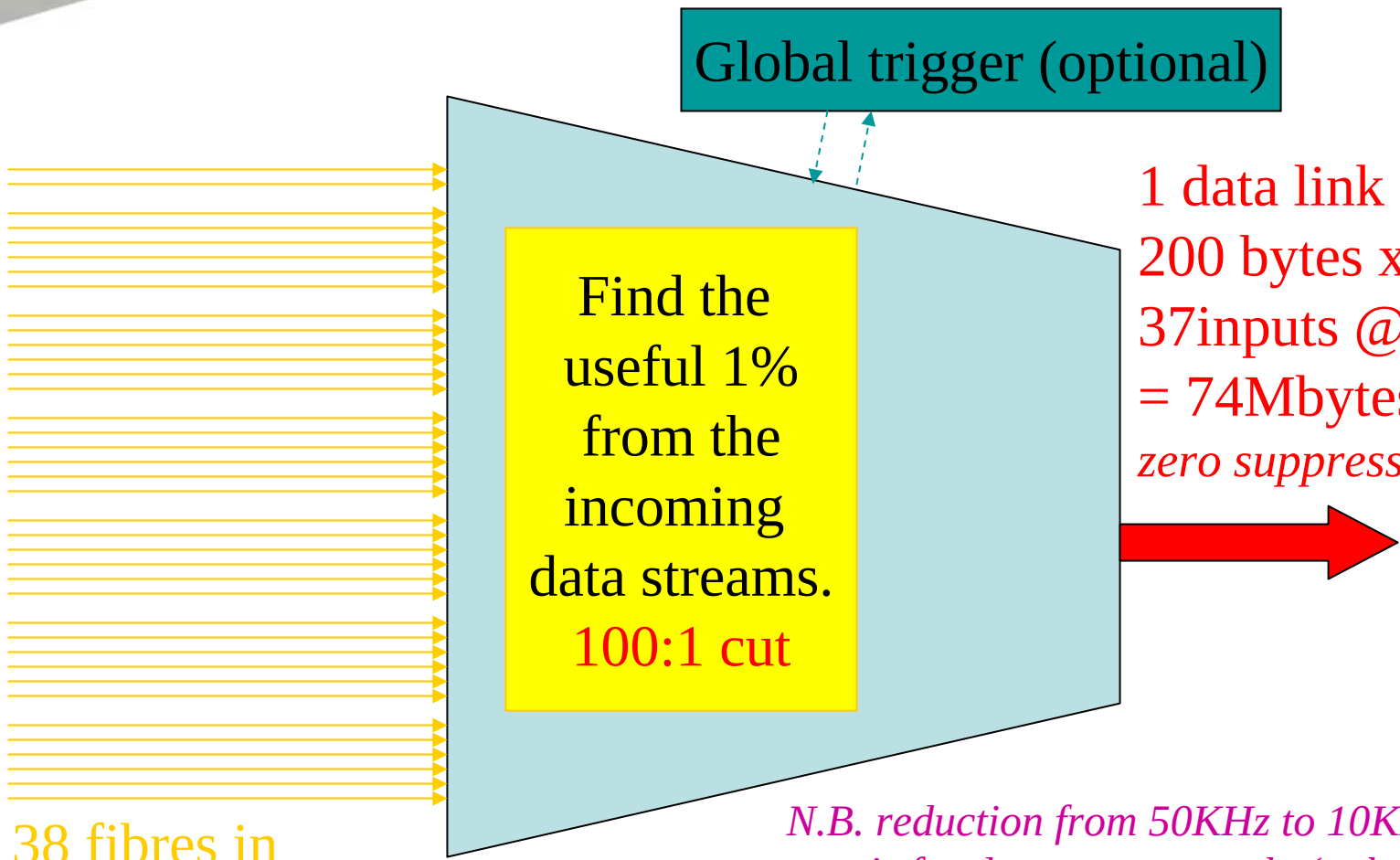
What does pre-processing do?



38 fibres in
(Core low/high gain + 36 segs).
= 38 x 2Gbps (7.6 Gbytes/sec)

N.B. reduction from 50KHz to 10KHz singles rate is for demonstrator only (to help PSA). Preprocessor output rate for full AGATA will be higher- 35 or 50KHz.

What does pre-processing do?

- Deserialises data from the digitiser
- Extracts all useful parameters which can be calculated on a per-channel basis in real time.
  - *Energy*
  - *Digitiser input offset control,*
  - *Time Over Threshold (preamp saturation = Pion energy)*
  - *Trigger (core only)*
  - *Timestamps the data when a local core trigger is found*
- Passes on these parameters, with leading edge of the digitised trace, to PSA.

What does pre-processing do?

- Interfaces with Global Trigger via GTS mezzanine to reduce data rate if necessary
- Sends GTS clock and clock synch to digitiser
- Concentrates and buffers data ready for transfer to PSA
- Prepares data for PSA (could perform zero suppression if needed)

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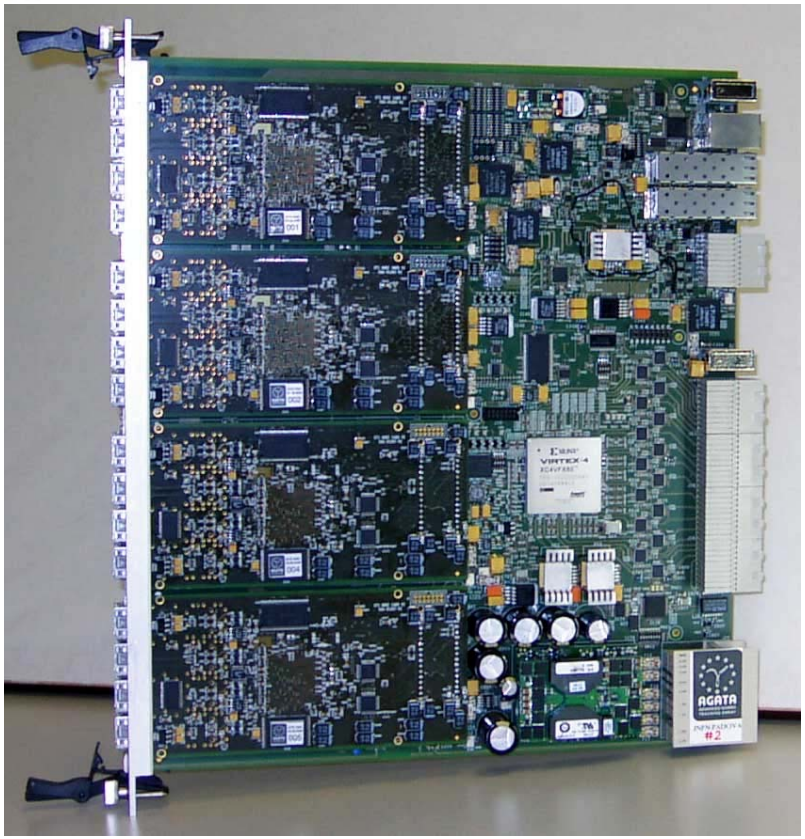
Pre-Processing hardware



Carrier (ATCA format)

Mezzanines (PMC format)

Photos- INFN Padova and CSNSM Orsay

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Pre-Processing people

Damiano	Bortolato
Marco	Bellato
Xavier	Lafay
Andrea	Triossi

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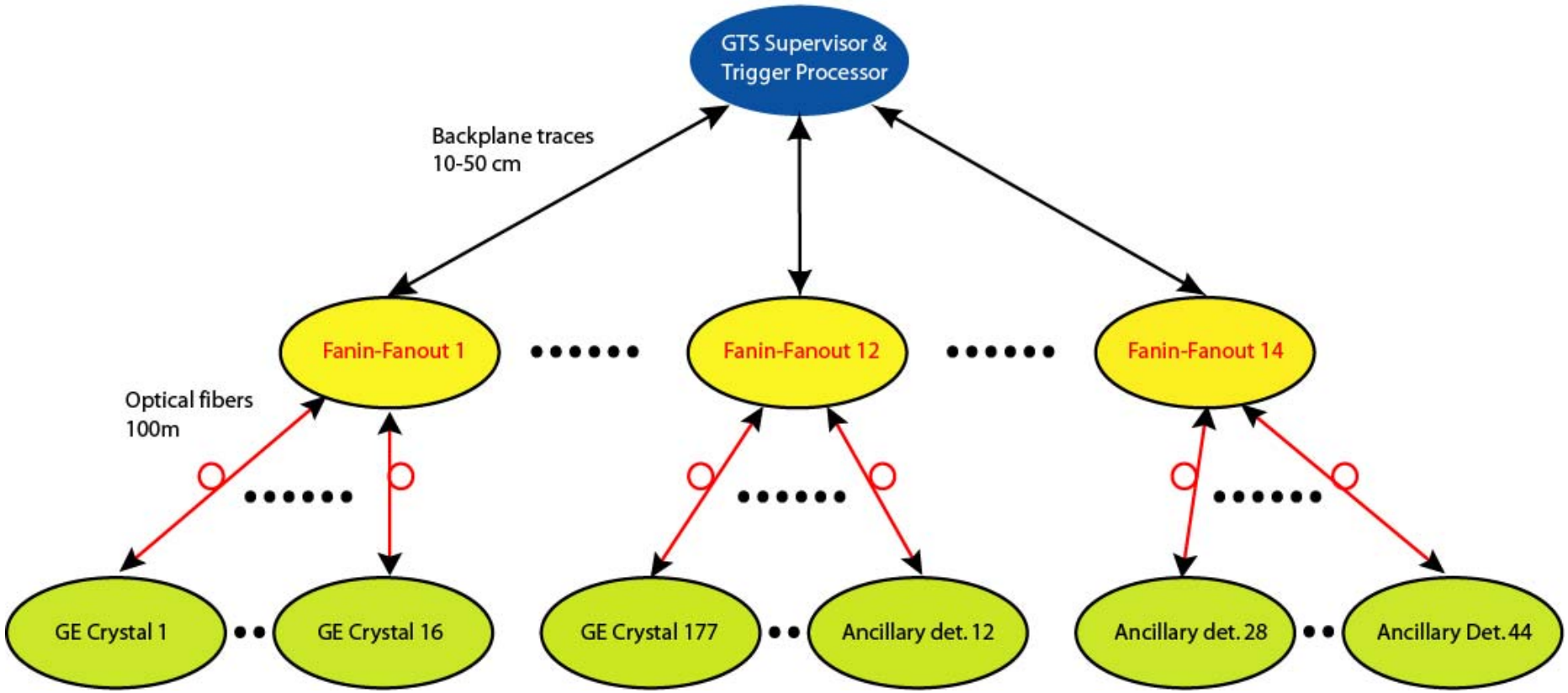
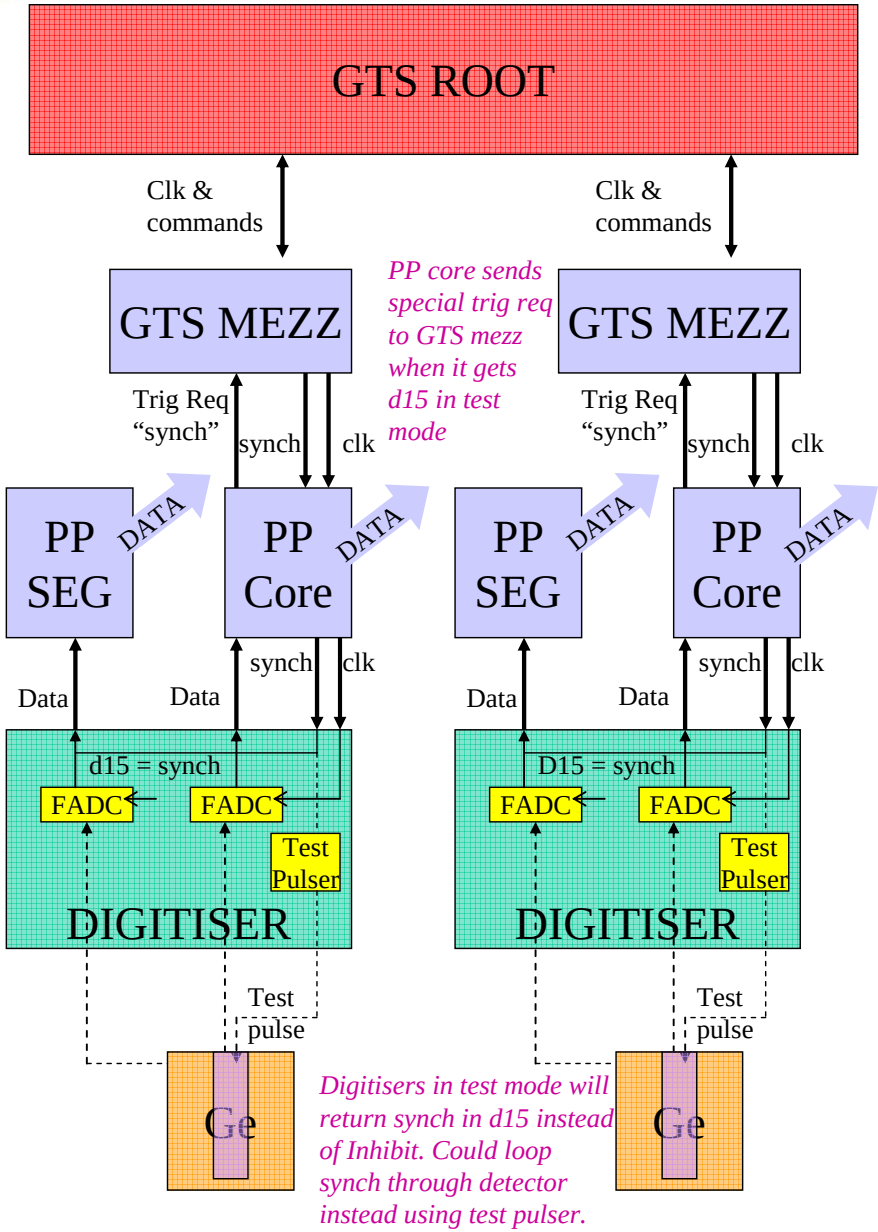
GTS Hierarchy




GTS ROOT
Clk & commands
Clk & commands
GTS MEZZ
GTS MEZZ
PP core sends special trig req to GTS mezz when it gets d15 in test mode
Trig Req "synch"
synch
clk
Trig Req "synch"
synch
clk
PP SEG
DATA
PP Core
DATA
PP SEG
DATA
PP Core
DATA
synch
clk
synch
clk
Data
Data
Data
Data
d15 = synch
D15 = synch
FADC
FADC
FADC
FADC
Test Pulser
Test Pulser
DIGITISER
DIGITISER
Test pulse
Test pulse
Ge
Ge
Digitisers in test mode will return synch in d15 instead of Inhibit. Could loop synch through detector instead using test pulser.

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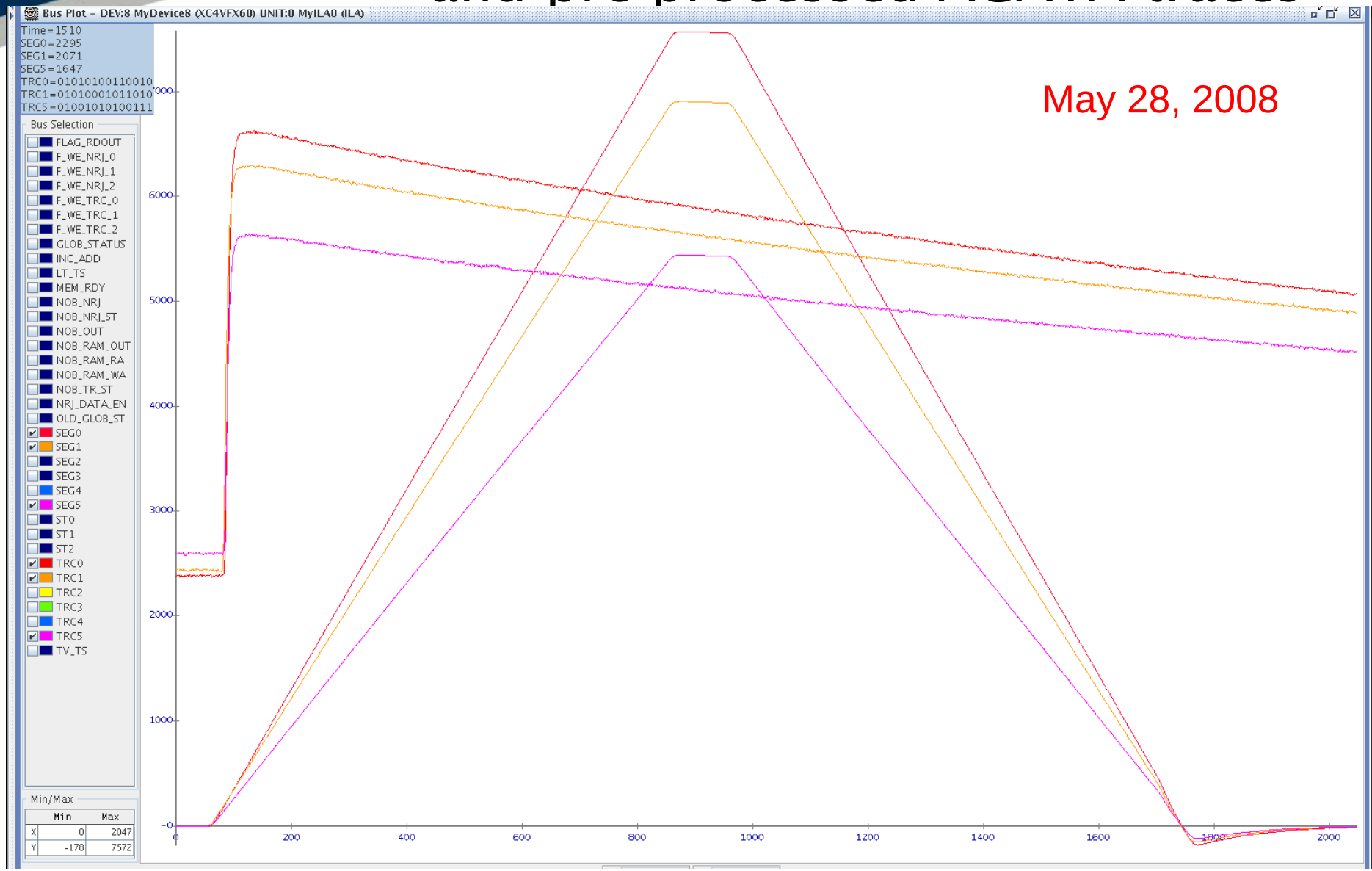
Digitized, optically-transmitted and pre-processed AGATA traces



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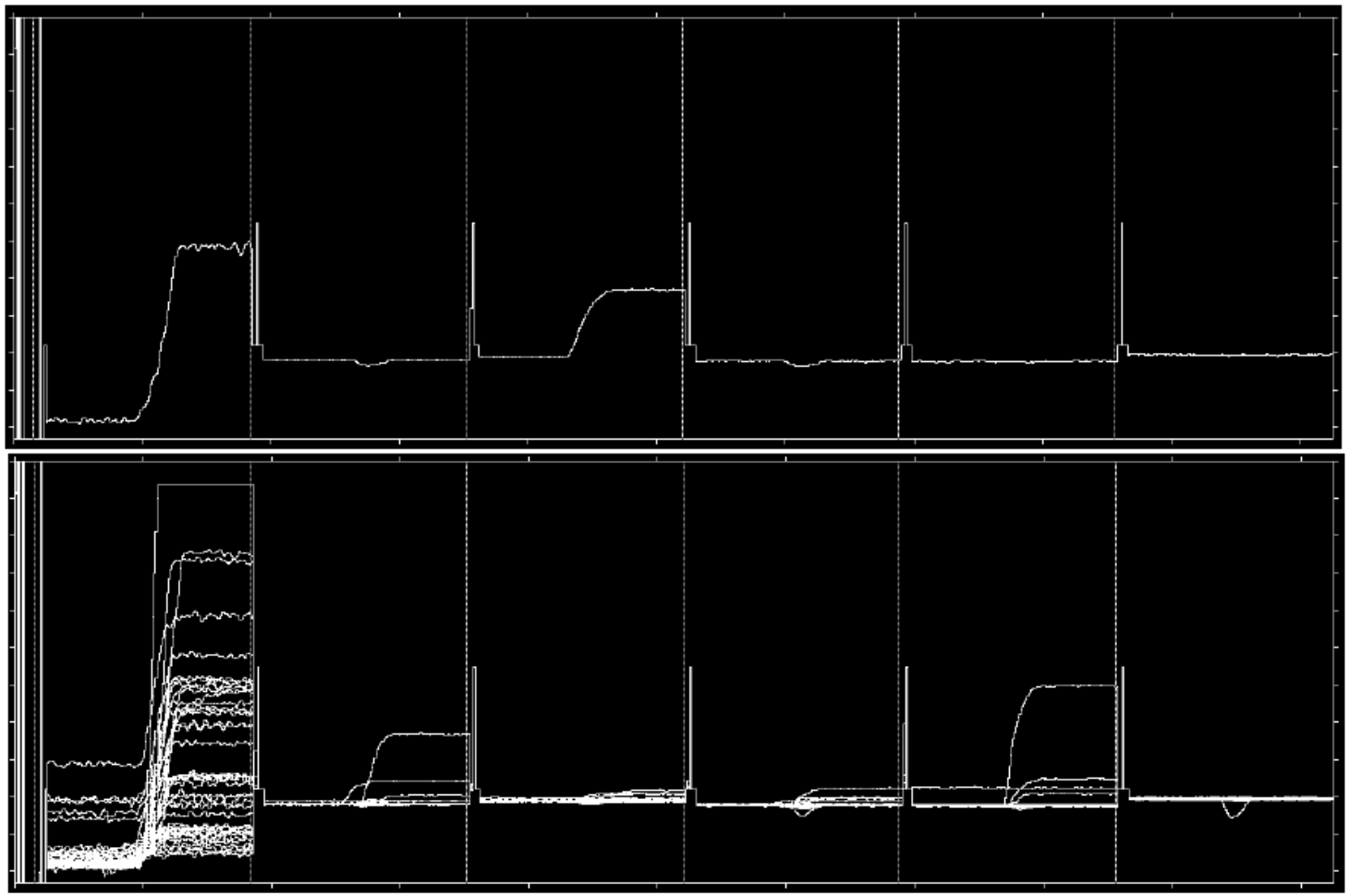
First events readout via PCIe July 4

Readout speed > 100 Mb/s, limited by disk access



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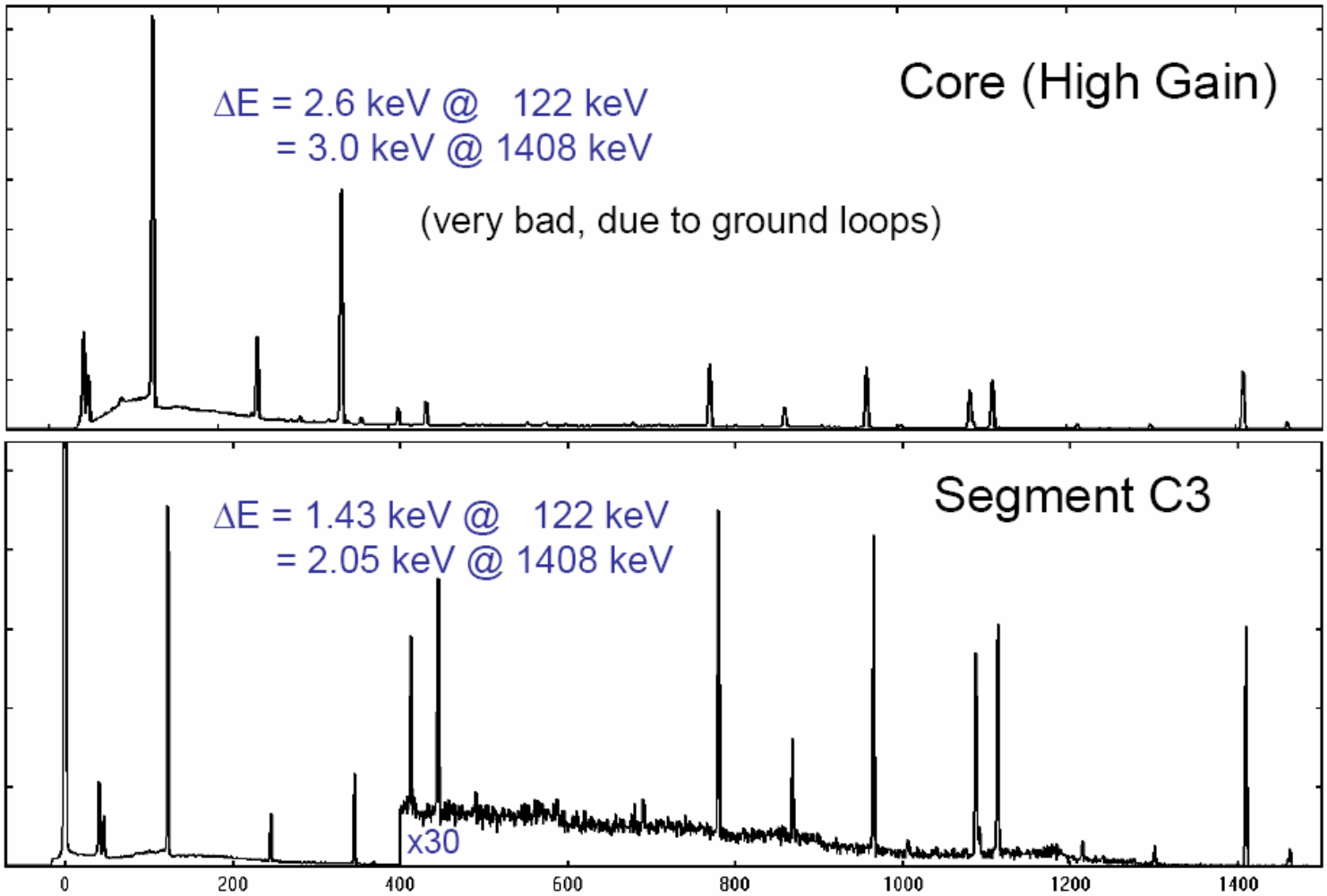
July 2008 energy resolution



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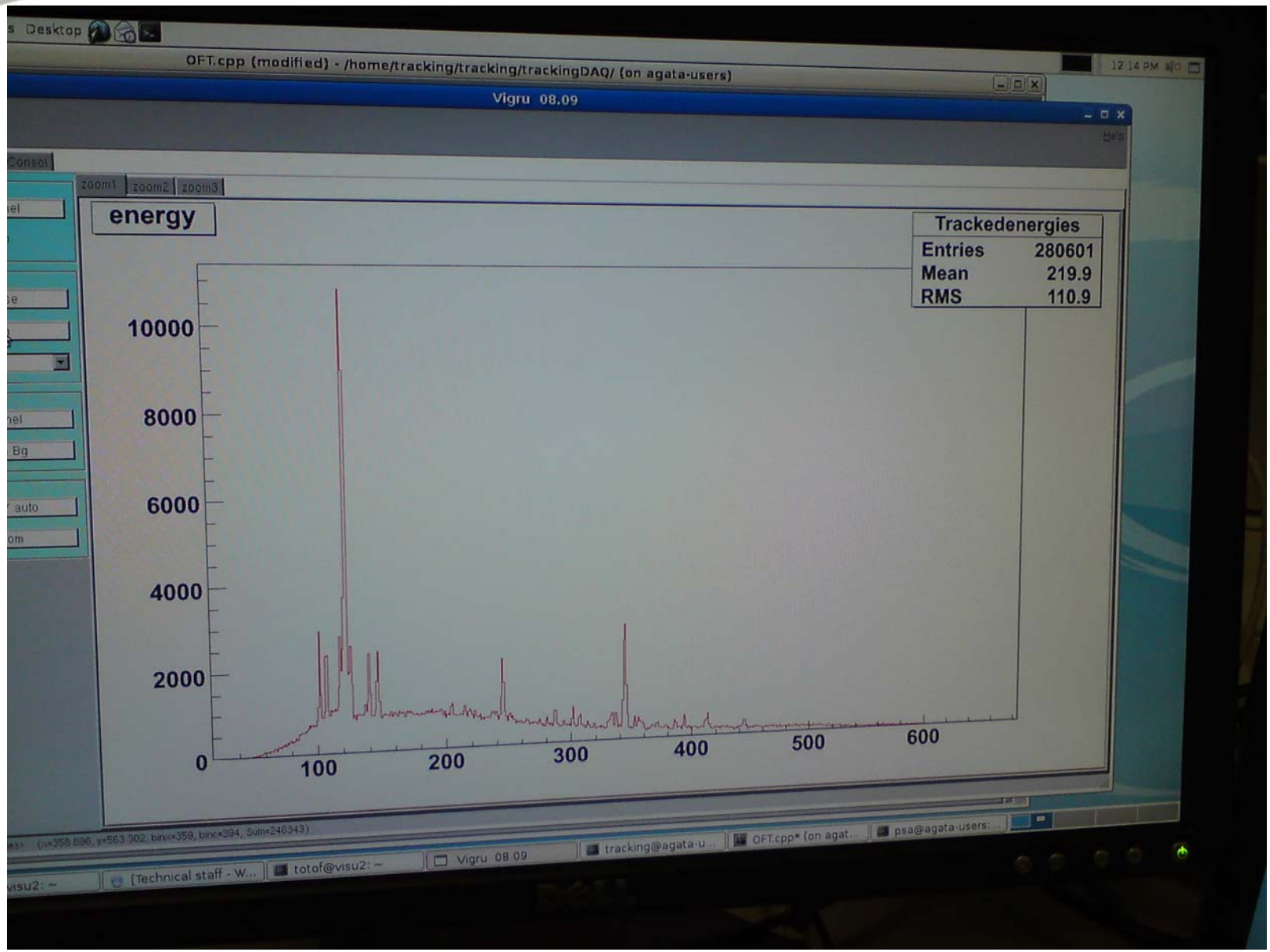
Feb 2009 Triple Cluster Live tracked data



Status of electronics

- **Digitisers**
  - 18 built
    - 8 LNL
    - 3 Turkey
    - 2 Strasbourg
    - 5 in DL.
- **Pre-processing Carriers**
  - first production cards delivered in Orsay 4/2/09.
  - Under tests before starting remainder of production.
- **Pre-processing Mezzanines**
  - production started
  - first cards to be tested week 12.
- **GTS mezzanine**
  - Final prototype test starting now
  - Production starts end April

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Provisional data format from PP

Item		Length in 16-bit words
Mezzanine header		16
Channel 1	header	8
	trace	160 samples
Channel 2	header	8
	trace	160 samples
Channel 3 … 6		

0	Mezzanine ID
1	Event number (2 words)
2	
3, 4, 5	Timestamp (3)
6	Number of samples in trace
7…15	Spare

0	Channel ID
1, 2	Energy 2 words (need to modify MWD)
3	Channel status (pileup, over/underflow…)
4… 7	Spare (e.g. BL value, energy from ToT …)

Length of Segment mezzanine block
→ 16+6*(8+160) = 1024 words

Length of Core Mezzanine block
→ 16+2*(8+160) = 352 words

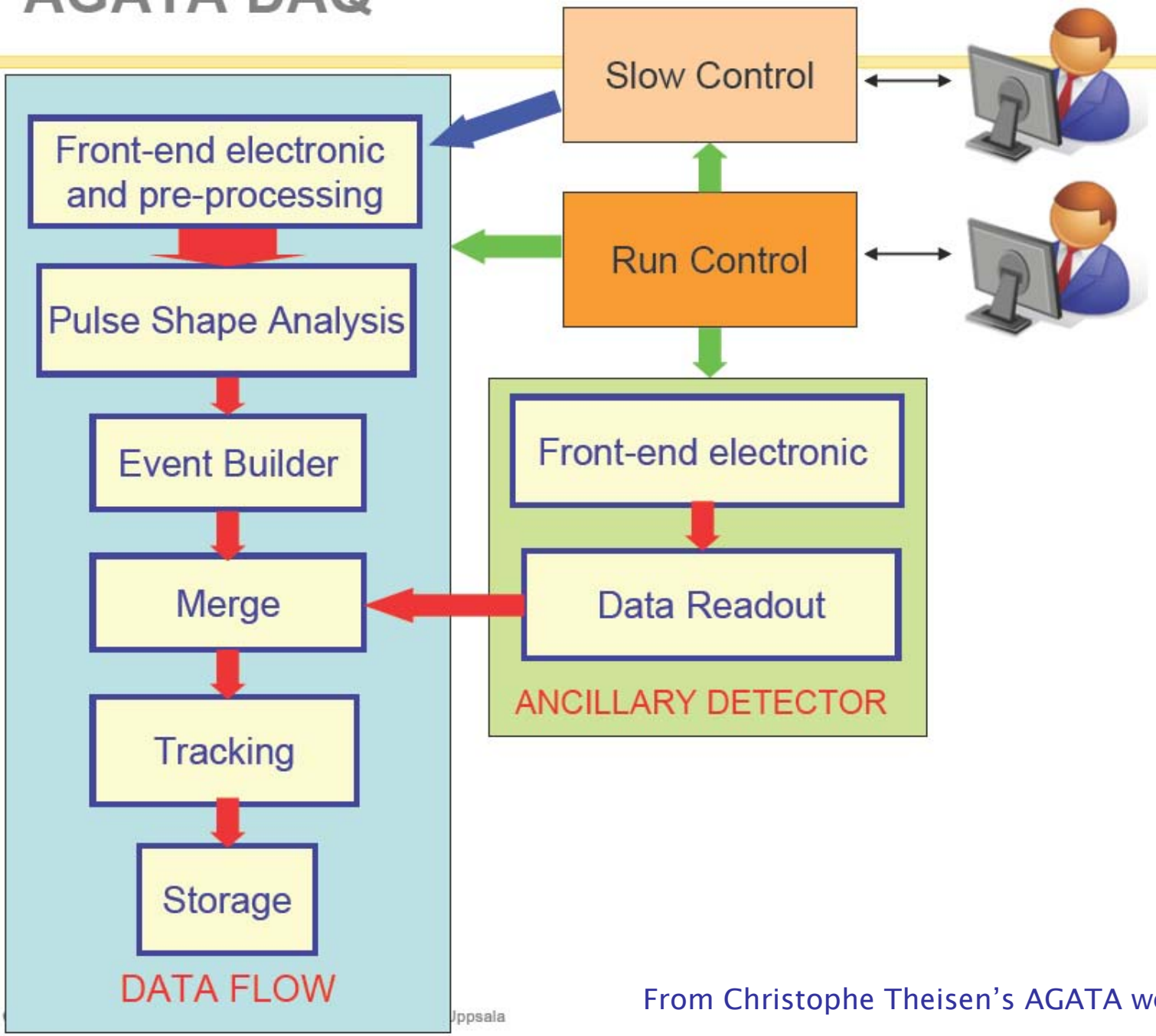
Length of event from Carrier 0 (CC+2 SG)
→ 352 + 2 * 1024 = 2400 words
(430 events in the 2 MB of DPRAM)

Length of event from Carrier 1 (4 SG)
→ 4 * 1024 = 4096 words
(256 events in the 2 MB of DPRAM)

Total length of event → 6496 words

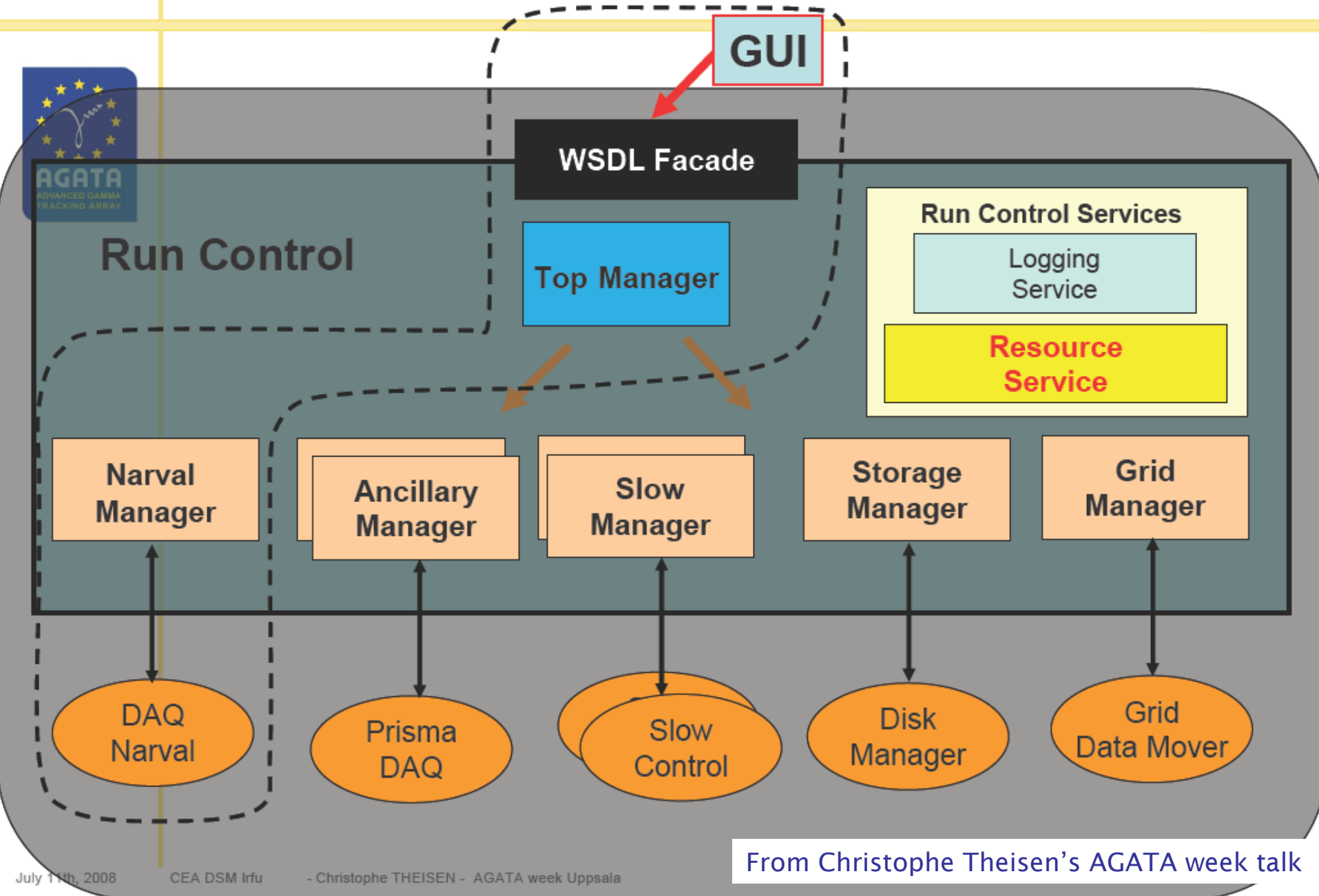
Possibility to reduce length by ~50 %

AGATA DAQ



From Christophe Theisen's AGATA week talk

Run Control Structure



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PRISMA with AGATA DAQ scheme

SETUP + CONTROL

CPU

AGAVA

ADC

VME crate

GTS

Event rate:
~20kHz (5Mb/sek)

Pre-preccessing & Narval Producer

Narval

Narval

. . .

Narval

From Piotr Bednarczyk's AGATA week talk

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AGATA- designed by an international team

- **DIGITISER** *Team size approx 10 people, 3 in UK (Patrick Coleman-Smith, Jim Thornhill, Dave Wells)*
  - STFC Daresbury
    - Digitiser digital design and PCB design for core and segment cards, production VHDL, digitiser mechanics
  - University of Liverpool
    - Digitiser Power supply and control boards, control card VHDL, digitiser mechanics
  - IPHC Strasbourg
    - Digitiser analogue design for core and segment cards and VHDL for standalone testing
- **Pre-processing** *Team Size approx 14 people, 1 in UK (Ian Lazarus)*
  - IPN Orsay
    - Carrier VHDL design (FPGA2- trigger distribution)
    - Carrier VHDL production code
    - Carrier commissioning (production run of 34 cards)
    - Original carrier design
  - INFN Padua
    - Carrier rework (prototype and pre-production)
    - Carrier VHDL (release 0 for initial tests)
    - Carrier VHDL (FPGA 0- data readout)
    - Delivery of 6 tested carriers system commissioning
    - GTS Mezzanine
  - CSNSM Orsay
    - Segment mezzanine (hardware and VHDL)
    - Core mezzanine (hardware and VHDL)
    - Production run of core and segment mezzanines
  - IPHC Strasbourg
    - Supply of MWD code for use in core and segment mezzanines in “black box” format
  - STFC RAL and LPC CAEN
    - VHDL code for carrier readout (PCIe and proprietry “FASTER” protocols)
- **Global clock and trigger systems (GTS)** *Team size approx 5 people, none in UK*
  - INFN Padua
    - GTS trigger algorithms
    - Clock alignment systems
    - GTS processor card and Mezzanine card design