New DPP-TF firmware

Index

Introduction

The new DPP-TF firmware involves the FPGAs on both the mother and daughter board. The main changes can be summarized as follow:

1) New memory management and event data format:

the memory is divided in *Buffers*; each buffer contains *Ne* events *(Events Aggregate)*; one event can contain one waveform of *Ns* samples (acquisition window) and/or one time stamp related to the trigger that caused the acquisition and/or one energy, that is the height of the trapezoid associated to the pulse that generate the above trigger. In case there are other pulses and triggers within the same acquisition window, the relevant time stamps and energies won't be saved in the data events. The position in the event data of the time stamp and energy words (when present) is fixed. Waveform, time stamp and energy can be enabled/disabled individually.

2) Individual trigger in/out:

each channel can generate a self-trigger and this can be propagated to one LVDS GPIO on the front panel of the board; likewise, each channel can be individually triggered from one GPIO. This feature is not implemented yet (it will be soon).

3) Multi board Synchronization and Start/Stop acquisition:

the propagation/distribution of the clock to several boards was already implemented in the previous firmware; however, we have fixed some bugs that could cause the loss of lock in the PLL; perhaps this might fix the problem found when reading the board in MBLT via the VME bus. Concerning the Start/Stop of the acquisition, we have implemented different options that will be described below.

4) DPP algorithms:

we have introduced some changes in the DPP algorithms in order to improve the ability to detect pulse pile-up, especially when it occurs on the rising edge of the pulses (Rise Time Discriminator). We tested this technique at high rates (up to 1 Mcps) using a random generator getting very good results. More tests will be done with real detectors.

There are also other minor changes that are reported in the list of changes at the end of this document.

NOTE: starting from release 3.0 of the mother board FPGA, the optical link has been upgraded to an improved throughput version (CONET2 link) that is not backward compatible with previous CAEN proprietary link. The CAEN A2818 PCI-to-CONET Optical link bridge board firmware must be upgraded in order to be able to directly connect with digitizers through optical link. In the new PCI express card A3818, the CONET2 protocol is native. VMEbus access to board (through VME master) remains unchanged.

1.1 Registers

We report here only the registers that change with respect to the old version.

1.1.1 FRONT PANEL CONTROL

Address: 0x811C
Bits: [31:0]
Access Mode: Read and Write

[0] 0x00000001 Default: 0	**LEMO I/Os (TRGIN, TRGOUT/GPO, SIN/GPI) Electrical Levels:** 0 = NIM, 1 = TTL
[1] 0x00000002 Default: 0	**LVDS GPIO Output Enable:** 0=enabled, 1=high impedance Note: the output enable is meaningful only for the GPIOs that are used as outputs according to the bits [5:2]
[2] 0x00000004 Default: 0	**LVDS GPIO[3:0] direction:** 0=input, 1=output
[3] 0x00000008 Default: 0	**LVDS GPIO[7:4] direction:** 0=input, 1=output
[4] 0x00000010 Default: 0	**LVDS GPIO[11:8] direction:** 0=input, 1=output
[5] 0x00000020 Default: 0	**LVDS GPIO[15:12] direction:** 0=input, 1=output
[7:6] 0x000000C0 Default: 0	**LVDS GPIO mode:** 00: General Purpose IO: the IO can be read or written (depending on the direction) through the register Front Panel IO Data at address 0x8118 01: Predefined IO settings (see the table below) 10: Trigger pattern: all GPIOs are used as input and their value is latched at the arrival of the trigger and saved in the event header in place of the trigger time tag. 11: reserved
[15:8]	**Reserved**
[17:16] 0x00030000 Default: 0	**TRGOUT/GPO Mode:** 00: TRGOUT propagates the internal trigger sources according to the FP Trigger Out Mask Register (0x8110). 01: TRGOUT is used to propagate signals of the Mother Board, according to the bits [19:18] of this register (Common Signals Virtual Probe) 10: TRGOUT is used to propagate signals of the Daughter boards (Channel Signals Virtual Probe) 11: Reserved
[19:18] 0x000C0000 Default: 0	**Common Signal Virtual Probe (propagated onto TRGOUT)**: this bit are meaningful only when bits[17:16]=01 00: RUN: the signal is active when the acquisition is running. This option can be used to synchronize the start/stop of the acquisition through the TRGOUT/GPO→TRGIN or TRGOUT/GPO→SIN/GPI daisy chain. 01: Reference CLK. This clock is synchronous with the sampling clock of the ADC and this option can be used to align the phase of the clocks in different boards. 10: Reserved 11: Reserved
[31:20]	**Reserved**

Predefined GPIO setting:

GPIO	Direction	Function
[7:0]	out	Individual Triggers from channels
[8]	out	Memory Full
[9]	out	Event Data Ready
[10]	out	Global trigger
[11]	out	Acquisition Run Status
[12]	in	Time Tag Reset
[13]	in	Memory clear
[14]	in	Reserved
[15]	in	Reserved

1.1.2 ACQUISITION CONTROL

Address: 0x8100
Bits: [5:0]
Access Mode: Read and Write

[1:0] 0x00000003 Default: 0	**Start/Stop mode:** 00: SW controlled. Start and Stop of Run take place on SW command, that is by setting/resetting bit 2 01: SIN controlled. If the acquisition is armed (bit 2 = 1), the run starts when SIN is asserted and stops when SIN returns inactive. If bit 2 = 0, the acquisition is always off. 10: First Trigger. If the acquisition is armed (bit 2 = 1), the run starts on the first trigger pulse (rising edge on TRGIN); this pulse is not used as trigger, actual triggers start from the second pulse. The stop of run must be SW controlled (reset of Bit 2) 11: GPIO controlled: like 01 but using GPIO[?] instead of SIN
[2] 0x00000004 Default: 0	**Acquisition Start or Arm:** when bits[1:0] = 00, this bit acts as a run start/stop (0=stopped, 1=running); when bits[1:0] = 01, 10, 11, this bit arms the acquisition (0=disarmed, 1=armed); the actual start/stop is controlled by an external signal, as described above.
[3] 0x00000008 Default: 0	**Trigger Counting Mode:** 0 = only accepted triggers, 1 = all triggers. This bit is meaningless in case of DPP firmware.
[4] 0x00000010 Default: 0	**Reserved**
[5] 0x00000020 Default: 0	**Memory Full Mode:** 0 = the board is full when all buffers are full; 1 = keep one buffer free. This bit is meaningless in case of DPP firmware.

1.1.3 SW CLOCK SYNC

Address: 0x813c
Bits: -
Access Mode: Write Only

A write access to this register (with any data) forces the PLL to re-align all the clock outputs with the reference clock. In case of daisy chain clock distribution between boards, during the initialization and configuration, the reference clocks along the daisy chain can be unstable and a temporary loss of lock may occur in the PLLs; although the lock is automatically recovered once the reference clocks return stable, it is not guaranteed that the phase shift returns to a known state. This command allows the board to restore the correct phase shift between the CLKIN and the internal clocks. NOTE: the command must be issued starting from the first to the last board in the chain.

1.1.4 START/STOP RUN DELAY

Address: 0x8170
Bits: [31:0]
Access Mode: Read/Write

When the start of run is given synchronously to several boards connected in daisy chain, it is necessary to compensate for the delay in the propagation of the start (or stop) signal through the chain. This register sets the delay (expressed in trigger clock cycles, i.e. 10 ns for the x724 models) between the arrival of the start signal at the input of the board (either SIN or TRGIN) and the actual start of run. The delay is usually zero for the last board in the chain and rises going backward along the chain. The latency between the leading edge of the start at the input of the board and the leading edge of the TRGOUT (or GPIO) when used to propagate the RUN signal is about ??? ns. The maximum value for the delay is ???.

1.1.5 CONFIG

Address: 0x8000, 0x8004 (BitSet), 0x8008 (BitClear)
Bits: [31:0]
Access Mode: Read and Write

[0]	**Must be 0**
[1] 0x00000002 Default: 0	**Trigger Overlap**: when two acquisition widows are overlapped, the second trigger can be either accepted or rejected (it is suggested to keep this bit cleared when using the DPP) **0:** Trigger overlapping not allowed (no trigger is accepted until the current acquisition window is finished) **1:** Trigger overlapping allowed (the current acquisition window is prematurely closed by the arrival of a new trigger)
[2]	**Must be 0**
[3] 0x00000008 Default: 0	**Test Mode:** Test mode has been removed
[4]	**Must be 1**

[7:5]	**Must be 0**
[8] 0x00000100 Default: 0	**Individual trigger**: Must be 1
[9] 0x00000200 Default: 0	**Invert Input**: DPP algorithms are designed to work with positive pulses. The input signal polarity can be digitally inverted inside the FPGA before applying the DPP algorithms. **NOTE:** in order to allow for individual setting of the polarity, another bit has been added in the register DPP_PAR4; the signal will be inverted when the OR of the two bits is 1. **0:** The digital signal is not inverted (analog signals are positive) **1:** The digital signal is inverted (analog signals are negative)
[10]	**Must be 0**
[11] 0x00000800 Default: 0	**Dual Trace**: when the oscilloscope mode is enabled (readout of waveforms), it is possible to read two different waveforms from the FPGA (for example the input signal and the trapezoid). When the dual trace is enabled, the samples of two signals are interleaved, thus each waveform is recorded at 50 MSps. **0:** Dual Trace disabled (record one waveform at 100 MSps) **1:** Dual Trace enabled (record two waveforms at 50 MSps)
[13:12] 0x00003000 Default: 0	**Virtual Probe 1:** Select which signal is associated to the trace 1 in the readout data. **00:** Input **01:** Delta (input 1st derivate) **10:** Delta2 (input 2nd derivate) **11:** Trapezoid (output of the trapezoid filter)
[15:14] 0x0000C000 Default: 0	**Virtual Probe 2:** Select which signal is associated to the trace 2 in the readout data (only in dual trace mode). **00:** Input **01:** Threshold + Trigger + Peaking **10:** Trapezoid - Baseline **11:** Baseline (of the trapezoid)
[16] 0x00010000 Default: 0	**Oscilloscope Mode:** it enables the saving of a certain number of samples in the event data. The number of samples depends on the Custom Size register setting and they belong to one or two signals, according to the Dual Trace and Virtual Probe settings. **0:** Oscilloscope Mode disabled **1:** Oscilloscope Mode enabled
[17] 0x00020000 Default: 0	**Energy Mode**: when enabled, the peak amplitude of the pulses, that is the height of the trapezoid, is saved into the event data (last word of the event). **0:** Energy Mode disabled **1:** Energy Mode enabled
[18] 0x00040000 Default: 0	**Time Tag Mode**: when enabled, the time tag (i.e. time of the zero crossing in the RC-CR^2 timing filter) is saved into the event data (first word of the event). **0:** Time Tag Mode disabled **1:** Time Tag Mode enabled
[19]	**Must be 0**
[22:20] 0x00700000 Default: 0	**Digital Virtual Probe**: when the oscilloscope mode is enabled, each 32 bit word contains two samples (14 bits) plus two digital values (digital virtual probes). One of them is the trigger, while the second one is selected by these 3 bits among the following options: **000:** Trigger Window **001:** Armed (i.e. delta2 has exceeded the threshold) **010:** Peak Running (peak searching is running) **011:** Peak Abort (pile-up detected: peak searching is aborted) **100:** Peaking (position where the flat top is sampled to calculate the trapezoid's amplitude) **101:** Peak Hold Off (protection time after the peaking or abort) **110:** Acquisition Veto (when the ADC is overrange, the acquisition is vetoed) **111:** Trigger Hold Off (protection time after the trigger that prevents the board to get another trigger)
[23]	**Must be 0**
[24]	**Enable Event Data Format Word**: when enabled, the aggregate data contains an extra word (after the size) that reports the settings necessary to interpret the event data. For more details, see the description of the event data format below
[31:25]	**Reserved**

1.1.6 BUFF_ORG

Address: 0x800C
Bits: [3:0]
Access Mode: Read and Write

Unlike the old DPP and standard firmware, in the new DPP the memory is not statically paged since we don't need to implement circular buffers. Therefore, there is no need to define the page size a priori. As said in the introduction, the memory is divided in buffers that contain Ne events (*Aggregates*). The buffer size is equal to N times the event size (waveform + time stamp + energy + info_words). This register sets the number of buffers (according to the table below) that can be written in the memory before it goes full and the acquisition is suspended. It is care of the user to set the correct number of buffers according to their size and the memory size (small mem option (default) = 256K words, large mem option = 2M words, 1 word = 32 bit).

REG	num buffers (*)	Max buffer size	
		Small Mem	Large Mem
0	Reserved	-	-
1	Reserved	-	-
2	4	64K	512K
3	8	32K	256K
4	16	16K	128K
5	32	8K	64K
6	64	4K	32K
7	128	2K	16K
8	256	1K	8K
9	512	512	4K
A	1024	256	2K

(*) one buffer is normally left free in order to avoid data overwriting, thus the memory goes full when the used number of buffer is equal to the available buffers – 1.

Example: suppose to have waveform length = 400 samples (200 words) + time stamp (1 word) + energy (1 word), hence event size = 202 words. Suppose to have Ne = 30 (num events per buffer), hence aggregate size = 202*30+2 (size + format info) = 6062 words. You can have up to 256K/6062 = 43 blocks, hence you should set the register to 6 (63 blocks).

1.1.7 POST_TRG

Address: 0x8114
Bits: [31:0]
Access Mode: Read and Write

Since the memory buffers are not managed as circular buffers, it does not make sense to set a post trigger; instead, there is a delay line (FIFO) to allow for a pre-trigger (see next register).

1.1.8 PRE_TRG

Address: 0x1n38
Bits: [9:0]
Access Mode: Read and Write

Defines the number of samples of the pre trigger: NS_{PRE} = PRE_TRG * 2.

1.1.9 CUST_SIZE

Address: 0x8020
Bits: [15:0]
Access Mode: Read and Write

This register allows the user to set the waveform length, that is the number samples in the waveform, according to the formula Ns = CustSize * 2. WARNING: unlike the old DPP and the standard FW, in the new DPP the number of samples is only decided by this register and it cannot be zero, otherwise no sample will be saved. The maximum value allowed for CustSize is 64K.

1.1.10 NEV_AGGREGATE

Address: 0x1n34
Bits: [9:0]
Access Mode: Read and Write

Sets the number of events contained in one buffer (aggregate). It can be any number between 1 and 1023.

1.1.11 DPP_PAR1

Address: 0x1n24 (channel n), 0x8024 (all channels)
Bits: [31:0]
Access Mode: Read and Write

[7:0] 0x000000FF Default: 0	**Rise Time (b):** Rise time of the input signal (expressed in sample periods)
[13:8] 0x00003F00 Default: 0	**Averaging window (a):** Number of samples used for the signal mean on delta and delta2
[14] 0x00004000 Default: 0	**Reserved**
[15] 0x00008000 Default: 0	**Delta/Delta2:** use delta in place of delta2 for the trigger.
[31:16] 0xFFFF0000 Default: 0	**Decay Time (M):** time constant of the exponential decay of the input signal (expressed in sample periods)

1.1.12 DPP_PAR2

Address: 0x1n28 (channel n), 0x8028 (all channels)
Bits: [31:0]
Access Mode: Read and Write

[9:0] 0x000003FF Default: 0	**Trapezoid Rise Time (k):** Rise time of the trapezoid (expressed in sample periods). It acts as the shaping time of a traditional shaping amplifier.
[11:10]	**Reserved**
[21:12] 0x000FFC00 Default: 0	**Trapezoid Flat Top (m):** trapezoid flat top length
[23:22]	**Reserved**
[29:24] 0x3F000000 Default: 0	**Peak value power2 division:** the trapezoid is internally calculated over 48 bits, however, it does not make sense to use all the bits to represent the peak amplitude: the value reported in the readout data will be shifted right on N bits (i.e. divided by 2^N), being N this parameter
[31:30] 0xC0000000 Default: 0	**BaseLine mean:** number of samples to average in the baseline calculation: **00:** Baseline restoration disabled **01:** 16 samples **10:** 256 samples **11:** 2048 samples

1.1.13 DPP_PAR3

Address: 0x1n2C (channel n), 0x802C (all channels)
Bits: [31:0]
Access Mode: Read and Write

[13:0] 0x00003FFF Default: 0	**Threshold:** Threshold that must be exceeded by the signal delta2 to arm the trigger (the trigger will actually occur on the zero crossing of delta2)
[15:14] 0x0000C000 Default: 0	**Decimation:** input signal decimation (need FW rev 128.5 or later) **00:** decimation disabled **01:** 2 samples (50 MSps)

	10: 4 samples (25 MSps) **11:** 8 samples (12.5 MSps)
[26:16] 0x07FF0000 Default: 0	**Flat Top Delay:** define the position on the trapezoid flat top where to get the sample for the calculation of the peak height (0 is about at the beginning of the trapezoid)
[27]	**Reserved**
[29:28] 0x30000000 Default: 0	**Peak averaging window:** number of samples to average on the flat top to calculate the peak amplitude. **00:** 1 sample **01:** 4 samples **10:** 16 samples **11:** 64 samples
[31:30] 0xC0000000 Default: 0	**Digital Gain:** **00:** Digital Gain = 1 **01:** Digital Gain = 2 (only with decimation >= 2 samples) **10:** Digital Gain = 4 (only with decimation >= 4 samples) **11:** Digital Gain = 8 (only with decimation = 8 samples)

1.1.14 DPP_PAR4

Address: 0x1n30 (channel n), 0x8030 (all channels)
Bits: [31:0]
Access Mode: Read and Write

[9:0] 0x000003FF Default: 0	**Trigger Window Width:** used by the rise time discriminator: the zero crossing of delta2 must occur before the end of the Trigger Window
[15:10] 0x0000FC00 Default: 0	**Trigger Hold Off:** defines how long the trigger hold off must be extended beyond the zero crossing
[21:16]	**Peak Hold Off:** defines how long the peak hold off must be extended beyond the end of the trapezoid
[29:22]	**Reserved**
[30]	**Overlapping Trapezoid reject:** when enabled, one trapezoid whose rising edge overlaps the falling edge of the previous one is considered piled-up and thus rejected,
[31]	**Invert Input:** individual setting for the input signal inversion. This bit is ORed with the common Invert Bit in the Config Register.

1.2 Event Data Format

"EVENTS AGGREGATE" DATA FORMAT

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

FI												AGGREGATE SIZE																				SIZE
DT	ES	EE	ET			VP1		VP2			DP				NUM SAMPLES																	FORMAT
TT																																EVENT 0
T_1	D_1											S_1																	T_0	D_0	S_0	
T_3	D_3											S_3																	T_2	D_2	S_2	
T_{n-1}	D_{n-1}											S_{n-1}																	T_{n-2}	D_{n-2}	S_{n-2}	
BASELINE (to be implemented)																													0	PEAK (ENERGY)		
TT																																EVENT 1
T_1	D_1											S_1																	T_0	D_0	S_0	
T_3	D_3											S_3																	T_2	D_2	S_2	
T_{n-1}	D_{n-1}											S_{n-1}																	T_{n-2}	D_{n-2}	S_{n-2}	
BASELINE (to be implemented)																													0	PEAK (ENERGY)		

FI: when 1, the second word is the Format Info

DT: Dual trace

ES: Waveform (samples) is enabled

EE: Energy is enabled

ET: Time Tag is enabled

VP1: Virtual Probe 1 Selection

VP2: Virtual Probe 2 Selection

DP: Digital Virtual Probe Selection

TT: Trigger Type (0=self trigger, 1=external trigger)

$S_{0, 2, 4... n-2}$: Even Samples of VP1

$S_{1, 3, 4... n-1}$: Odd Samples of VP1 when DT=0, else Even Samples of VP2

T_n: Trigger

D_n: Digital Virtual Probe

"CHANNELS AGGREGATE" DATA FORMAT

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	0	1	0	TOTAL AGGREGATE SIZE (in lwords)																												HEADER
BOARD ID								PATTERN														CHANNEL MASK										
								EVENT COUNTER																										
EVENT TIME TAG																																
EVENTS AGGREGATE CH0																																CH 0
EVENTS AGGREGATE CH1																																CH 1
...																																...
EVENTS AGGREGATE CH7																																CH 7

The readout of the digitizer is done using the Block Transfer; for each transfer, the board gives a certain number of Channels Aggregates (Data Block). The maximum number of aggregates that can be transferred in a BLT is defined by the former register MAX_NUM_EVENTS_BLT (actually it should be called MAX_NUM_AGGREGATES_BLT). Each aggregate is actually made of one 4 word header, in which there is the channel participating mask that indicates which channel is present with data in that aggregate. The header contains also the total size of the Channels Aggregate. The rest of the header is meaningless for the purpose of the DPP firmware.

DATA BLOCK

CHANNELS AGGREGATE 0
CHANNELS AGGREGATE 1
...
CHANNELS AGGREGATE n-1

1.3 Trigger

To be done

1.4 Synchronization

Mode 1: TRGOUT-TRGIN daisy chain

```
ACQ_CTRL[1:0] = 10
ACQ_CTRL[2] = arm
FP_CTRL[17:16] = 01
FP_CTRL[19:18] = 00
```

The boards are daisy chained through the TRGOUT and TRGIN connectors that first act as Start of Run and then as trigger: once the acquisition has been armed, the first pulse received from the TRGIN input starts the acquisition (that pulse is ignored by the trigger logic); as soon as the run starts, a pulse is sent to the TRGOUT of the board so that the next board in the chain can start the acquisition, and so on until the end of the chain. The first board in the chain can be either started by a pulse on its TRGIN or by a SW command. In the latter case, the first board must be programmed with ACQ_CTRL[1:0]=00. Since there is some latency (still to be measured) in the propagation of the start from one board to the next board, it is possible to delay the start with respect to the TRGIN signal. This delay can be programmed (register at address 0x8170). The delay doesn't affect the TRGOUT.

In this mode, it is not possible to stop the boards simultaneously (the stop must be issued by clearing Bit 2 of ACQ_CTRL).

The SIN input (leading edge) can be used to reset the time stamp, also during the acquisition.

Mode 2: TRGOUT-SIN daisy chain

```
ACQ_CTRL[1:0] = 01
ACQ_CTRL[2] = arm
FP_CTRL[17:16] = 01
FP_CTRL[19:18] = 00
```

The boards are daisy chained through the TRGOUT and SIN connectors. In this case, the start signal is not a pulse (edge) but it is a level: once the acquisition has been armed, the acquisition starts when SIN goes high and stops when it returns low. The TRGOUT of the board goes high/low according to the status of the acquisition, so that the next board in the chain can start/stop the acquisition, and so on until the end of the chain. The first board in the chain can be either started/stopped by driving its SIN high/low or by a SW command. In the latter case, the first board must be programmed with ACQ_CTRL[1:0]=00. Since there is some latency (still to be measured) in the propagation of the start from one board to the next board, it is possible to delay the start with respect to the SIN signal. This delay can be programmed (register at address 0x8170). The delay doesn't affect the TRGOUT.

In this mode, the TRGIN input can be normally used as external trigger. The reset of the time stamp as well as the propagation of the trigger output can be done using the GPIOs

Mode 3: GPIO

```
ACQ_CTRL[1:0] = 11
ACQ_CTRL[2] = arm
```

In this case, the boards are not daisy chained; instead, the start of the acquisition is given in parallel using a fan-out that drives the GPIO[?] of all board simultaneously. The start signal is a level: once the acquisition has been armed, the acquisition starts when GPIO[?] goes high and stops when it returns low. All the boards starts at the same time and there is no need to program different delays for the start.

In this mode, the TRGIN and TRGOUT can be normally used as external triggers. The SIN input (leading edge) can be used to reset the time stamp, also during the acquisition.

1.5 List of changes

- Discontinued memory test (ramp generator)
- Added bit for the individual input signal inversion (this bit is ORed with the common bit in the Config Register). See DPP_PAR4 at 0x1n30.
- Added automatic acquisition veto when the analog signal is outside the input dynamic range (ADC over-range);
- Modified options for DPP Virtual Probe2 and DPP Digital Probe. See CONFIG at 0x8000.
- Modified saving of digital virtual probe and trigger bits from half to full sampling frequency.
- Modified options for the calculation of the baseline (num. of samples for the moving window mean). See DPP_PAR2 at 0x1n28.
- Added parameter to extend the peak hold-off after the end of the trapezoid in order to prevent the baseline calculation (moving window mean) to start when the baseline is still unstable. See DPP_PAR4 at 0x1n30.
- Added bit to enable the rejection of the trapezoids whose rising edge overlap the falling edge of the previous one. See DPP_PAR4 at 0x1n30.
- Added parameter for the trigger hold off. See DPP_PAR4 at 0x1n30.
- Added Rise Time Discriminator able to detect two pulses piling up on the rising edge. See DPP_PAR4 at 0x1n30.
- Modified the operating mode of the external trigger (still to be defined with more details…)
- Added SW command (write access to 0x1n3A) to flush the current event block even if it is not filled up
- Added possibility to clear the time tag through the GPIO[xxx]
- Modified memory management and event data format
- Discontinued Post Trigger register and added Pre Trigger register at 0x1n38 (max pre trigger size = 512 samples)
- Modified Optical Link protocol from CONET1 to CONET2 (WARNING: CONET2 is not backward compatible)
- Added options for the TRGOUT (propagation of the RUN signal, CLOCK probe, etc…). See Front Panel Control at 0x811C
- Added register (0x8170) for the programmable delay on start/stop
- Added SW command (write to 0x813C) to force the clock re-alignment
- Modified options for Start/Stop acquisition. See Acquisition Control at 0x8100.
- Added possibility for SIN to act as a reset for the time stamp (in parallel with GPIO[???]) when not used as start of run.
- Modified SW reset to prevent the PLL and the relevant output clocks to be affected by it
- Discontinued register at 0x8128 (downsample operated by the mother board); not to be confused with the decimation in the DPP filters.
- Discontinued Gated acquisition mode (bit 0 of the Config register at 0x8000.