R3B registers map 5.00, 29Sep14

Table 1 is a summary of the registers that are accessible via software for the custom logic of the R3B readout system for the Silicon detector. The total address space for the plb_address_space peripheral is 64KB and is divided in address ranges that are currently configured to 1KB each (256 32-bit registers). The registers can be accessed by using the baseaddress of the plb_address_space peripheral and the address offset for each register, as shown in Table 1.

Register No	Register offset	Address byte offset (hex)	Register Name	Access Type	Value @power-up(hex)
Address Range 1: Date and version registers					
1	1	0x00000000	Date	Read	Release date
2	2	0x00000004	Version	Read	Release version
Address Range 2: DMA registers					
3	1	0x00000400	Dma_control	Read/Write	0x00000000
4	2	0x00000404	Dma_status	Read	0x00000C33
5	3	0x00000408	Buffer_base_addr	Read/Write	0x00000000
6	4	0x0000040C	Burst_size	Read/Write	0x00000400
7	5	0x00000410	Block_size	Read/Write	0x00000004
8	6	0x00000414	Buffer_size	Read/Write	0x00000008
9	7	0x00000418	Buffer_rd_pntr	Read/Write	0x00000000
10	8	0x0000041C	Buffer_wr_pntr	Read	0x00000000
11	9	0x00000420	Wr_byte_no_0	Read	0x00000000
12	10	0x00000424	Wr_byte_no_1	Read	0x00000000
13	11	0x00000428	Timer_cnt_0	Read	0x00000000
14	12	0x0000042C	Timer_cnt_1	Read	0x00000000
15	13	0x00000430	Lost_packet_cnt	Read	0x00000000
Address Range 3: Calibration registers					
15	1	0x00000800	Calib_control	Read/Write	0x00000000
16	2	0x00000804	Calib_status	Read	0x00000066
17	3	0x00000808	Calib_status_ch0	Read	0x00000000
18	4	0x0000080C	Calib_status_ch1	Read	0x00000000
19	5	0x00000810	Calib_status_ch2	Read	0x00000000
20	6	0x00000814	Calib_status_ch3	Read	0x00000000
21	7	0x00000818	Calib_status_ch4	Read	0x00000000
22	8	0x0000081C	Calib_status_ch5	Read	0x00000000
23	9	0x00000820	Calib_status_ch6	Read	0x00000000
24	10	0x00000824	Calib_status_ch7	Read	0x00000000
Address Range 4: Asic_Val_Rst_or registers					
25	1	0x00000C00	Asic_val_rst_or_control	Read/Write	0x00000000
26	2	0x00000C04	Val_width	Read/Write	0x00000000
27	3	0x00000C08	Val_delay	Read/Write	0x00000000
28	4	0x00000C0C	Val_no	Read/Write	0x00000000

29	5	0x00000C10	Rst_width	Read/Write	0x00000000
30	6	0x00000C14	Or_cnt_0	Read	0x00000000
31	7	0x00000C18	Or_cnt_1	Read	0x00000000
32	8	0x00000C1C	PacketNo_Valid_ch0	Read	0x00000000
33	9	0x00000C20	PacketNo_Not_Valid_ch0	Read	0x00000000
34	10	0x00000C24	PacketNo_Valid_ch1	Read	0x00000000
35	11	0x00000C28	PacketNo_Not_Valid_ch1	Read	0x00000000
36	12	0x00000C2C	PacketNo_Valid_ch2	Read	0x00000000
37	13	0x00000C30	PacketNo_Not_Valid_ch2	Read	0x00000000
38	14	0x00000C34	PacketNo_Valid_ch3	Read	0x00000000
39	15	0x00000C38	PacketNo_Not_Valid_ch3	Read	0x00000000
40	16	0x00000C3C	PacketNo_Valid_ch4	Read	0x00000000
41	17	0x00000C40	PacketNo_Not_Valid_ch4	Read	0x00000000
42	18	0x00000C44	PacketNo_Valid_ch5	Read	0x00000000
43	19	0x00000C48	PacketNo_Not_Valid_ch5	Read	0x00000000
44	20	0x00000C4C	PacketNo_Valid_ch6	Read	0x00000000
45	21	0x00000C50	PacketNo_Not_Valid_ch6	Read	0x00000000
46	22	0x00000C54	PacketNo_Valid_ch7	Read	0x00000000
47	23	0x00000C58	PacketNo_Not_Valid_ch7	Read	0x00000000
Address Range 5: Timestamp_Fpga_registers					
48	1	0x00001000	Ts_fpga_control	Read/Write	0x00000000
49	2	0x00001004	Butis_status	Read	0x00000000

Table 1

Address Range 1: Date and version registers

Date register (0x00000000)

Bit(s)	Name	Core Access	Reset Value	Description
31-24	Day	Read	N/A	Day of firmware release
23-16	Month	Read	N/A	Month of firmware release
15-0	Year	Read	N/A	Year of firmware release

Version register (0x00000004)

Bit(s)	Name	Core Access	Reset Value	Description
31-16	Major Release	Read	N/A	Major version of current release
15-0	Minor release	Read	N/A	Minor version of current release

Address Range 2: DMA registers

Dma control register (0x00000400)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 3	Reserved	N/A	N/A	Reserved
2	Capture	Read/Write	0	0-1 transition captures the values of the <total_wr_byte_no> and <timer> counters. Needs to be set to 0 in software.
1	reset	Read /write	0	1 = dma state machines and fifo reset 0 = normal operation
0	start	Read/write	0	0 = dma stop 1 = dma start

Dma status register (0x00000404)

Bit(s)	Name	Core Access	Reset Value	Description
31-12	Reserved	N/A	N/A	Reserved, reads always 0
11	Wrll_idle	Read	1	0 = Write local link state machine busy 1 = Write local link state machine not busy
10	Cmd_idle	Read	1	0 = Command state machine busy 1 = Command machine not busy
9	burst_timeout	Read	0	0 = no timeout 1 = timeout took place at some point. Value is latched and should be cleared by software with the assertion of rst, in the control register
8	burst_error	Read	0	0 = no error 1 = error took place at some point. Value is latched and should be cleared by software with the assertion of rst, in the control register.
7	Reserved	N/A	0	Reserved, reads always 0
6	fifo_full	Read	0	1 = fifo is full 0 = fifo is not full

5	fifo_prog_empty	Read	1	0 = at least one <Burst_size> is available. 1 = No <Burst_size> is available
4	fifo_empty	Read	1	0 = at least one fifo entry is available 1 = No fifo entry is available
3	Reserved	N/A	0	Reserved, reads always 0
2	buffer_full	Read	0	1 = buffer is full 0 = buffer is not full
1	buffer_prog_empty	Read	1	0 = at least one <Block_size> is available 1 = No <Block Size> is not available
0	buffer_empty	Read	1	0 = at least one <Burst_size> is available. 1 = No <Burst_size> is available

Buffer_Base_Addr register (0x00000408)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Buffer_Base_Addr	Read /write	0x00000000	Start address of buffer, in bytes

Burst_size register (0x0000040C)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Burst_size	Read/Write	0x00000000	Minimum entry to the buffer, in bytes, min = 64, max = 2048

Block_size register (0x00000410)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Block_size	Read/Write	0x00000000	in <Burst_size>, programmable empty threshold for the buffer. When the buffer entries are greater or equal to <Block_size>, <buffer_prog_empty> (in status register) de asserts.

Buffer_size register (0x00000414)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Buffer_size	Read/Write	0x00000000	in <Burst_size>, multiples of <Block_size>.

Buffer_rd_pntr register (0x00000418)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Buffer_rd_pntr	Read/Write	0x00000000	In < Burst_size>, use by hardware to compute the < buffer_full>, <buffer_prog_empty> and <buffer empty flags>. Reset to zero when it reaches 2x<Buffer_size>.

Buffer_wr_pntr register (0x0000041C)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Buffer_wr_pntr	Read	0x00000000	In <Burst_size>, for debugging purposes (could also be used by software to compute the empty flags). Resets to zero when it reaches 2x<Buffer_size>.

Wr_byte_no_0 (0x00000420)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Wr_byte_no_0	Read	0x00000000	Lower 32-bits of total bytes written into the buffer, in bytes

Wr_byte_no_1 (0x00000424)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Wr_byte_no_1	Read	0x00000000	Upper 32-bits of total bytes written into the buffer, in bytes

Timer_cnt_0 (0x00000428)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Timer_cnt_0	Read	0x00000000	Lower 32-bits of timer counter, in write clock cycles

Timer_cnt_1 (0x0000042C)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Timer_cnt_1	Read	0x00000000	Upper 32-bits of timer counter, in write clock cycles

Lost_packet_cnt (0x00000430)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Lost_packet_cnt	Read	0x00000000	Counts the number of packets that are lost, because the dma is full. When counter reaches maximum value, then that value is latched. Reset counter (dma control register, bit 1) to enable counting again.

Notes on dma operation:

- Write values to < Buffer_base_addr>, < Burst_size>, < Block_size> and <Buffer_size>.
- Reset dma by toggling the reset bit (bit 1) in the control register.
- Start dma by setting start bit (bit 0) in control register.
- Poll buffer_prog_empty (bit 1) in status register. When it is low, read a block of data.
- After reading a block of data, update the <Buffer_rd_pntr> register with <Buffer_rd_pntr> =<Buffer_rd_pntr> + <Block_size>. Reset the <Buffer_rd_pntr> to zero when it reaches 2x<Buffer_size>.

Notes on dma statistics:

- At any point, capture the value of the < Wr_byte_no_x> and <Timer_cnt_x> by asserting the capture bit (bit 2) in the control register to 1. The write throughput rate is then equal to: (Wr_byte_no_x /Time_cnt_x) x write clock frequency.
- Since the write throughput is expected to be higher than the read throughput and the write is inhibited when the buffer is full, then the write throughput will also reflect the read throughput.

The < Wr_byte_no_x> can also be used at the end of a dma operation (start = 0, bit 0, control register) to compare it with the Rd_byte_no. Both numbers should match.

- <Timer_cnt_x> can also be used by software in order to create a direct read throughput rate.

Address Range 3: Calibration registers

Calib control register (0x00000800)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 1	Reserved	N/A	N/A	Reserved
1	Reset	Read/write	0	0 = Reset disabled 1 = Reset Active
0	start	Read/write	0	0 = Calib stop 1 = Calib start

Calib status register (0x00000804)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 8	Reserved	N/A	N/A	Reserved
7	Reserved	N/A	N/A	Reserved
6	bitSlipIdle	Read	1	0 = bitSlip state machine busy 1 = bitSlip state machine not busy
5	bitSlipChIdle	Read	1	0 = bitSlipCh state machine busy 1 = bitSlipCh state machine not busy
4	bitSlipChDone	Read	0	0 = bitSlipCh state machine not done 1 = bitSlipCh state machine done
3	Reserved	N/A	N/A	Reserved
2	bitAlignIdle	Read	1	0 = bitAlign state machine busy 1 = bitAlign state machine not busy
1	bitAlignChIdle	Read	1	0 = bitAlignCh state machine busy 1 = bitAlignCh state machine not busy
0	bitAlignChDone	Read	0	0 = bitAlignCh state machine not done 1 = bitAlignCh state machine done

Calib status ch0-3 register (0x00000808 - 0x00000824)

Bit(s)	Name	Core Access	Reset Value	Description
31-30	Reserved	N/A	N/A	Reserved, reads always 0
29-24	TapDlyCnt	Read	0	This is equal to the final tap delay, (valid when bitAlignDone=1 and bitAlignError= 0)
23-22	Reserved	N/A	N/A	Reserved, reads always 0
21-16	jitterWindow	Read	0	The jitter window width in tap delays.
15-14	Reserved	N/A	N/A	Reserved, reads always 0
13	bitSlip	Read	0	Value is adjusted automatically to compensate for phase relationship b/w clk and clk_2x
12	edgeSel	Read	0	0 = iddr neg_edge output is stable 1 = iddr pos_edge output is stable
11	edge_end_second_overflow	Read	0	0 = no delay taps overflow. 1 = run out of delay taps, while looking for the second edge of the jitter window.
10	edge_end_first_overflow	Read	0	0 = no delay taps overflow. 1 = run out of delay taps, while looking for the second edge of the jitter window.
9	edge_start_second_overflow	Read	0	0 = no delay taps overflow. 1 = run out of delay taps, while looking for the first edge of the jitter window.
8	edge_start_first_overflow	Read	0	0 = no delay taps overflow. 1 = run out of delay taps, while looking for the first edge of the jitter window.
7	inPhase	Read	0	0 = iddr outputs are not in phase 1 = both iddr outputs are in phase (valid when pos_edge_stable and neg_edge_stable = 1)
6	neg_edge_stable	Read	0	0 = falling edge of iddr clk is aligned with edge of bit time 1 = falling edge of iddr clk is aligned with middle of bit time

5	pos_edge_stable	Read	0	0 = rising edge of iddr clk is aligned with edge of bit time 1 = rising edge of iddr clk is aligned with middle of bit time
4	stableRegion	Read	0	0 = sampling jitter window at start-up 1 = sampling outside jitter window (stable area) at start-up
3	bitSlipError	Read	0	0 = bitSlip ok 1 = bitSlip error (valid when bitSlipDone =1)
2	bitSlipDone	Read	0	0 = bitSlip is not done 1 = bitSlip is done
1	bitAlignmentError	Read	0	0 = bitAlign ok 1 = bitAlign error (valid when bitAlignDone=1)
0	bitAlignDone	Read	0	0 = bitAlign is not done 1 = bitAlign is done

Notes on Calibration registers:

- Start the bit alignment and bitslip by toggling start bit in Calib control register (0x00000800, bit 0).
- Check the Calib status register returns 0x77.
- Check the Calib status Ch0-3 register (bits 3-0 should be 5, i.e calib done with no errors).

Address Range 4: Asic_val_rst_or registers

Asic_val_rst_or control (0x00000C00)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 6	Reserved	N/A	N/A	Reserved
5	Or_cnt_rst	Read/write	0	0 = no reset 1 = reset
4	Asic_rst_rst	Read/write	0	0 = no reset 1 = reset (loads new values to Rst registers)
3	Asic_rst_trig	Read/write	0	0 = no reset pulse 1 = reset pulse with a pulse width as set in <Asic_pulseGen_width> register. Needs to be set to 0 in software.
2	Val_rst	Read/write	0	0 = no reset 1 = reset (loads new values to Val registers)
1	Val_mode	Read/write	0	0 = continuous pulses 1 = burst pulses as defined in <pulse
0	Val_trig	Read/write	0	0 = no valid pulses 1 = valid pulse(s) Needs to be set to 0 in software.

Val_width register (0x00000C04)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Val_width	Read/write	0	Pulse width of asic_val signal in clk cycles

Val_delay register (0x00000C08)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Val_delay	Read/write	0	Pulse delay of asic_val signal in clk cycles

Val_no register (0x00000C0C)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Val_no	Read/write	0	Pulse period No of asic_val signal

Rst_width register (0x00000C10)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Rst_width	Read/write	0	Pulse width of asic_rst signal in clk cycles

Or_cnt_0 (0x00000C14)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Or_cnt_0	Read	0x00000000	Number of <Or> rising edges, lower 32-bits.

Or_cnt_1 (0x00000C18)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Or_cnt_1	Read	0x00000000	Number of <Or> rising edges, upper 32.

Notes on Val registers:

- Set the < Val_width> and < Val_delay> registers. The sum of the 2 registers is the pulse period.
- Set the continuous or burst mode in < Asic_val_rst_or control> register, bit 1 (Val_mode)
- If Val_mode is set to burst, then set the number of bursts in the <Val_no> register
- Toggle Asic_rst (bit 2) in < Asic_val_rst_or control> register, in order to load the above values to the internal counters.
- Set Val_trig (bit 0) in < Asic_val_rst_or control> register, in order to start the Val pulses.

Notes on Rst registers:

- Set the <Rst_width> register.
- Toggle Asic_rst_rst (bit 4) in < Asic_val_rst_or control> register, in order to load the above value to the internal counter.
- Set asic_rst_trig (bit 3) in < Asic_val_rst_or control> register, in order to start the Rst pulse.

PacketNo_Valid_chX (0x00000CXX)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	PacketNo_Valid_chX	Read	0x00000000	Counts the Number of valid packets received from the Asic[1].

PacketNo_Not_Valid_chX (0x00000CXX)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	PacketNo_Not_Valid_chX	Read	0x00000000	Counts the Number of invalid packets received from the Asic[1].

[1] A packet is considered valid if the 2 starting bits have been received (2 ones) and the 48th bit (stop bit) is zero. If the stop bit is received as 1, then this is considered as an invalid packet.

Address Range 5: Timestamp Fpga registers

Timestamp_fpga_control (0x00001000)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 2	Reserved	N/A	N/A	Reserved
1	asic_ts_rst_ val_mode	Read/write	0	0 = blocks sync_pulses from being the asic_ts_rst 1 = allows sync_pulses to be the asic_ts_rst
0	Clk_sel	Read/write	0	0 = selects Butis_clk, external 200MHz 1 = selects internal 200MHz.

Notes:

When the asic_val mode is set to asic timestamp reset (see r3b asic user manual), in software, then asic_ts_rst_val_mode should also be set.

Butis_status (0x00001004)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 2	Reserved	N/A	N/A	Reserved
1	BuTis_uncertain_o	read	0	
0	BuTis_error_o	read	0	