R3B registers map 5.04, 14Dec17

Table 1 is a summary of the registers that are accessible via software for the custom logic of the R3B readout system for the Silicon detector. The total address space for the plb_address_space peripheral is 64KB and is divided in address ranges that are currently configured to 1KB each (256 32-bit registers). The registers can be accessed by using the baseaddress of the plb_address_space peripheral and the address offset for each register, as shown in Table 1.

Register No	Register offset	Address byte offset (hex)	Register Name	Access Type	Value @power-up(hex)
Address Range 1: Date, version and Module Id registers					
0	0	0x00000000	Date	Read	Release date
1	1	0x00000004	Version	Read	Release version
2	2	0x00000008	Module Id	Read/Write	0xFFFFFFFF
Address Range 2: DMA registers					
3	0	0x00000400	Dma_control	Read/Write	0x00000000
4	1	0x00000404	Dma_status	Read	0x00000C33
5	2	0x00000408	Buffer_base_addr	Read/Write	0x00000000
6	3	0x0000040C	Burst_size	Read/Write	0x00000400
7	4	0x00000410	Block_size	Read/Write	0x00000004
8	5	0x00000414	Buffer_size	Read/Write	0x00000008
9	6	0x00000418	Buffer_rd_pntr	Read/Write	0x00000000
10	7	0x0000041C	Buffer_wr_pntr	Read	0x00000000
11	8	0x00000420	Wr_byte_no_0	Read	0x00000000
12	9	0x00000424	Wr_byte_no_1	Read	0x00000000
13	10	0x00000428	Timer_cnt_0	Read	0x00000000
14	11	0x0000042C	Timer_cnt_1	Read	0x00000000
15	12	0x00000430	Lost_packet_cnt	Read	0x00000000
Address Range 3: Calibration registers					
16	0	0x00000800	RxChain_control	Read/Write	0x00000000
17	1	0x00000804	RxChain_status	Read	0xFFFF0000
18	2	0x00000808	EdgeDetCnt_10	Read	0x00000000
19	3	0x0000080C	EdgeDetCnt_32	Read	0x00000000
20	4	0x00000810	EdgeDetCnt_54	Read	0x00000000
21	5	0x00000814	EdgeDetCnt_76	Read	0x00000000
22	6	0x00000818	SampleChangeCnt_10	Read	0x00000000
23	7	0x0000081C	SampleChangeCnt_32	Read	0x00000000
24	8	0x00000820	SampleChangeCnt_54	Read	0x00000000
25	9	0x00000824	SampleChangeCnt_76	Read	0x00000000
26	10	0x00000828	BitErrCnt_10	Read	0x00000000
27	11	0x0000082C	BitErrCnt_32	Read	0x00000000
28	12	0x00000830	BitErrCnt_54	Read	0x00000000
29	13	0x00000834	BitErrCnt_76	Read	0x00000000

30	14	0x00000838	pckValCnt_10	Read	0x00000000
31	15	0x0000083C	pckValCnt_32	Read	0x00000000
32	16	0x00000840	pckValCnt_54	Read	0x00000000
33	17	0x00000844	pckValCnt_76	Read	0x00000000
34	18	0x00000848	ModIdErrCnt_10	Read	0x00000000
35	19	0x0000084C	ModIdErrCnt _32	Read	0x00000000
36	20	0x00000850	ModIdErrCnt _54	Read	0x00000000
37	21	0x00000854	ModIdErrCnt _76	Read	0x00000000
38	22	0x00000858	stopBitErrCnt_10	Read	0x00000000
39	23	0x0000085C	stopBitErrCnt_32	Read	0x00000000
40	24	0x00000860	stopBitErrCnt_54	Read	0x00000000
41	25	0x00000864	stopBitErrCnt_76	Read	0x00000000
42	26	0x00000868	ChainIdleState	Read/Write	0x00005555
Address Range 4: Asic_Val_Rst_or registers					
42	0	0x00000C00	Asic_val_rst_or_control	Read/Write	0x00000000
43	1	0x00000C04	Val_width	Read/Write	0x00000000
44	2	0x00000C08	Val_delay	Read/Write	0x00000000
45	3	0x00000C0C	Val_no	Read/Write	0x00000000
46	4	0x00000C10	Rst_width	Read/Write	0x00000000
47	5	0x00000C14	Or_cnt_0	Read	0x00000000
48	6	0x00000C18	Or_cnt_1	Read	0x00000000
Address Range 5: Timestamp_Fpga_registers					
49	0	0x00001000	Ts_fpga_control	Read/Write	0x00000000
50	1	0x00001004	Butis_status	Read	0x00000000

Table 1

Address Range 1: Date and version registers

Date register (0x00000000)

Bit(s)	Name	Core Access	Reset Value	Description
31-24	Day	Read	N/A	Day of firmware release
23-16	Month	Read	N/A	Month of firmware release
15-0	Year	Read	N/A	Year of firmware release

Version register (0x00000004)

Bit(s)	Name	Core Access	Reset Value	Description
31-16	Major Release	Read	N/A	Major version of current release
15-0	Minor release	Read	N/A	Minor version of current release

Module ID register (0x00000008)

Bit(s)	Name	Core Access	Reset Value	Description
31-14	Reserved	Read/write	All ones	Not Used
13-8	Module ID P side	Read/write	All ones	Asic Register 6 -> Bits 5-0
7-6	Reserved	Read/write	All ones	Not Used
5-0	Module ID N side	Read/write	All ones	Asic Register 6 -> Bits 5-0

Address Range 2: DMA registers

Dma control register (0x00000400)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 3	Reserved	N/A	N/A	Reserved
2	Capture	Read/Write	0	0-1 transition captures the values of the <total_wr_byte_no> and <timer> counters. Needs to be set to 0 in software.
1	reset	Read /write	0	1 = dma state machines and fifo reset 0 = normal operation
0	start	Read/write	0	0 = dma stop 1 = dma start

Dma status register (0x00000404)

Bit(s)	Name	Core Access	Reset Value	Description
31-12	Reserved	N/A	N/A	Reserved, reads always 0
11	Wrll_idle	Read	1	0 = Write local link state machine busy 1 = Write local link state machine not busy
10	Cmd_idle	Read	1	0 = Command state machine busy 1 = Command machine not busy
9	burst_timeout	Read	0	0 = no timeout 1 = timeout took place at some point. Value is latched and should be cleared by software with the assertion of rst, in the control register
8	burst_error	Read	0	0 = no error 1 = error took place at some point. Value is latched and should be cleared by software with the assertion of rst, in the control register.
7	Reserved	N/A	0	Reserved, reads always 0
6	fifo_full	Read	0	1 = fifo is full 0 = fifo is not full

5	fifo_prog_empty	Read	1	0 = at least one <Burst_size> is available. 1 = No <Burst_size> is available
4	fifo_empty	Read	1	0 = at least one fifo entry is available 1 = No fifo entry is available
3	Reserved	N/A	0	Reserved, reads always 0
2	buffer_full	Read	0	1 = buffer is full 0 = buffer is not full
1	buffer_prog_empty	Read	1	0 = at least one <Block_size> is available 1 = No <Block Size> is not available
0	buffer_empty	Read	1	0 = at least one <Burst_size> is available. 1 = No <Burst_size> is available

Buffer_Base_Addr register (0x00000408)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Buffer_Base_Addr	Read /write	0x00000000	Start address of buffer, in bytes

Burst_size register (0x0000040C)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Burst_size	Read/Write	0x00000000	Minimum entry to the buffer, in bytes, min = 64, max = 2048

Block_size register (0x00000410)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Block_size	Read/Write	0x00000000	in <Burst_size>, programmable empty threshold for the buffer. When the buffer entries are greater or equal to <Block_size>, <buffer_prog_empty> (in status register) de asserts.

Buffer_size register (0x00000414)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Buffer_size	Read/Write	0x00000000	in <Burst_size>, multiples of <Block_size>.

Buffer_rd_pntr register (0x00000418)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Buffer_rd_pntr	Read/Write	0x00000000	In < Burst_size>, use by hardware to compute the < buffer_full>, <buffer_prog_empty> and <buffer empty flags>. Reset to zero when it reaches 2x<Buffer_size>.

Buffer_wr_pntr register (0x0000041C)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Buffer_wr_pntr	Read	0x00000000	In <Burst_size>, for debugging purposes (could also be used by software to compute the empty flags). Resets to zero when it reaches 2x<Buffer_size>.

Wr_byte_no_0 (0x00000420)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Wr_byte_no_0	Read	0x00000000	Lower 32-bits of total bytes written into the buffer, in bytes

Wr_byte_no_1 (0x00000424)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Wr_byte_no_1	Read	0x00000000	Upper 32-bits of total bytes written into the buffer, in bytes

Timer_cnt_0 (0x00000428)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Timer_cnt_0	Read	0x00000000	Lower 32-bits of timer counter, in write clock cycles

Timer_cnt_1 (0x0000042C)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Timer_cnt_1	Read	0x00000000	Upper 32-bits of timer counter, in write clock cycles

Lost_packet_cnt (0x00000430)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Lost_packet_cnt	Read	0x00000000	Counts the number of packets that are lost, because the dma is full. When counter reaches maximum value, then that value is latched. Reset counter (dma control register, bit 1) to enable counting again.

Notes on dma operation:

- Write values to < Buffer_base_addr>, < Burst_size>, < Block_size> and <Buffer_size>.
- Reset dma by toggling the reset bit (bit 1) in the control register.
- Start dma by setting start bit (bit 0) in control register.
- Poll buffer_prog_empty (bit 1) in status register. When it is low, read a block of data.
- After reading a block of data, update the <Buffer_rd_pntr> register with <Buffer_rd_pntr> =<Buffer_rd_pntr> + <Block_size>. Reset the <Buffer_rd_pntr> to zero when it reaches 2x<Buffer_size>.

Notes on dma statistics:

- At any point, capture the value of the < Wr_byte_no_x> and <Timer_cnt_x> by asserting the capture bit (bit 2) in the control register to 1. The write throughput rate is then equal to: (Wr_byte_no_x /Time_cnt_x) x write clock frequency.
- Since the write throughput is expected to be higher than the read throughput and the write is inhibited when the buffer is full, then the write throughput will also reflect the read throughput.
  The < Wr_byte_no_x> can also be used at the end of a dma operation (start = 0, bit 0, control register) to compare it with the Rd_byte_no. Both numbers should match.
- <Timer_cnt_x> can also be used by software in order to create a direct read throughput rate.

Address Range 3: Calibration registers

RxChain_control register (0x00000800)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 24	CaptCnt	Read/Write	0000000	0-1 transition captures the values of the <StartModIdValCnt>, <PacValCnt> and <StopBitErrorCnt counters. Needs to be set to 0 in software.
23-16	SoftRst_ch7_0	Read/write	0000000	0 = Reset De-asserted 1 = Reset Asserted
15-8	PckEn_ch7-0	Read/write	0000000	0 = Blocks Packets to DMA 1 = Allows Packets to DMA
7-0	BitSlipStart_ch7-0	Read/write	0000000	0 = BitSlipStart stop 1 = BitSlipStart start (checking for 65K consecutive zeros)

RxChain_status register (0x00000804)

Bit(s)	Name	Core Access	Reset Value	Description
31-24	Ch7_0_asicPktIdle	Read	1111111	0 = asicPck state machine busy 1 = asicPck machine not busy
23-16	Ch7_0_ DinBin	Read	0000000	Decoded Manchester Encoded bit. When Din1Done /= Din0Done, then DinBin should be zero when the chain does not transmit any packets.
15-8	Ch7_0_ Din1Done	Read	0000000	Selects Manchester Encoded bit for packet Rx. See DinDone table below.
7-0	Ch7_0_ Din0Done	Read	0000000	Selects Manchester Encoded bit for packet Rx. See DinDone table below.

DinDone Table

ChX_Din1Done	ChX_Din0Done	Description
0	0	Not yet completed. Check that BitSlipStart has been asserted.
0	1	65K consecutive zeros has been found in Din0. Select Din0 for packet Rx.
1	0	65K consecutive zeros has been found in Din1. Select Din1 for packet Rx.
1	1	Error, check that Manchester encoded is enabled and is idling at zero.

EdgeDetCnt_XY* registers (0x00000808 - 0x00000814),

*where X = ch1 or ch3 or ch5 or ch7
Y = ch0 or ch2 or ch3 or ch6

Bit(s)	Name	Core Access	Reset Value	Description
31-16	EdgeDetCnt_X	Read	0	Counts the presence of edges from the oversampling of the bit time.
15-0	EdgeDetCnt_Y	Read	0	Counts the presence of edges from the oversampling of the bit time.

SampleChangeCnt_XY registers (0x00000818 - 0x00000824)

Bit(s)	Name	Core Access	Reset Value	Description
31-16	SampleChangeCnt _X	Read	0	Counts whenever a different sample is chosen to sample the bit time.
15-0	SampleChangeCnt_Y	Read	0	Counts whenever a different sample is chosen to sample the bit time.

BitErrCnt_XY registers (0x00000828 - 0x00000834)

Bit(s)	Name	Core Access	Reset Value	Description
31-16	BitErrCnt _X	Read	0	Counts whenever the Manchester Encoded data returns 2 bits of the same value.
15-0	BitErrCnt_Y	Read	0	Counts whenever the Manchester Encoded data returns 2 bits of the same value.

PckValCnt_XY registers (0x00000838 - 0x00000844)

Bit(s)	Name	Core Access	Reset Value	Description
31-16	PckValCnt_X	Read	0	Counts when valid asic packet (correct start bits, Module ID and stop bit) is received.
15-0	PckValCnt_Y	Read	0	Counts when valid asic packet (correct start bits, Module ID and stop bit) is received.

ModIdErrCnt_XY registers (0x00000848 - 0x00000854)

Bit(s)	Name	Core Access	Reset Value	Description
31-16	ModIdErrCnt _X	Read	0	Counts when state machine has not found the expected Mod ID..
15-0	ModIdErrCnt _Y	Read	0	Counts when state machine has not found the expected Mod ID.

StopBitErrCnt_XY registers (0x00000858 - 0x00000864)

Bit(s)	Name	Core Access	Reset Value	Description
31-16	StopIDErrCnt_X	Read	0	Counts when state machine has not found the expected stop bit.
15-0	StopIDErrCnt_Y	Read	0	Counts when state machine has not found the expected stop bit.

ChainIdleState (0x00000868)

Bit(s)	Name	Core Access	Reset Value	Description
31-16	StopIDErrCnt_X	Read	0	Counts when state machine has not found the expected stop bit.
15-0	StopIDErrCnt_Y	Read	0	Counts when state machine has not found the expected stop bit.

Notes on Calibration registers for software:

- Read Module ID Asic Reg6, bit 5-0 from both sides and write it to Module Id (0x00000008).

- Block data from being sent from the chains. One way is to write 0 in Asic Reg 1, bits 5 and 4. The Asic then expects VAL input high to validate a hit. Make sure the Val input is low. Another way is to write 0 to Asic Reg 5.

- Configure the Asics so that the chains output data that is Manchester Encoded.

- Reset the RxBlk block for all 8 chains by toggling the reset bits:
  RxChain_control register, (0x00000800, bits 23-16).

- Assert DinStart high for all 8 chains.
  RxChain_control register, (0x00000800, bits 7-0).

- Check for each channel that Din0Done is not equal to Din1Done.
  RxChain_status register, (0x00000804, Din0Done-> bits 7-0, Din1Done->bits 15-8).

- De-assert DinStart low for all 8 chains.
  RxChain_control register, (0x00000800, bits 7-0).

- Assert (active high) the packet enable bit for all 8 chains:
  RxChain_control register, (0x00000800, bits 7-0).
  (Deassert the above bits when the user requests a STOP in the DAQ program.)

- Enable data to be sent from the chains. Restore original value to Asic Reg 1, bits 5 and 4 or restore original value to reg5, if this was used to block the data in the first place.

- Do NOT issue any more Asic Reset in software from this point onwards. If you do, repeat the procedure above.

Notes on Counters for software:

<StartModIdValCnt> = <PacValCnt> and <StopBitErrorCnt

Address Range 4: Asic_val_rst_or registers

Asic_val_rst_or control (0x00000C00)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 6	Reserved	N/A	N/A	Reserved
5	Or_cnt_rst	Read/write	0	0 = no reset 1 = reset
4	Asic_rst_rst	Read/write	0	0 = no reset 1 = reset (loads new values to Rst registers)
3	Asic_rst_trig	Read/write	0	0 = no reset pulse 1 = reset pulse with a pulse width as set in <Asic_pulseGen_width> register. Needs to be set to 0 in software.
2	Val_rst	Read/write	0	0 = no reset 1 = reset (loads new values to Val registers)
1	Val_mode	Read/write	0	0 = continuous pulses 1 = burst pulses as defined in <pulse>
0	Val_trig	Read/write	0	0 = no valid pulses 1 = valid pulse(s) Needs to be set to 0 in software.

Val_width register (0x00000C04)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Val_width	Read/write	0	Pulse width of asic_val signal in clk cycles

Val_delay register (0x00000C08)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Val_delay	Read/write	0	Pulse delay of asic_val signal in clk cycles

Val_no register (0x00000C0C)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Val_no	Read/write	0	Pulse period No of asic_val signal

Rst_width register (0x00000C10)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Rst_width	Read/write	0	Pulse width of asic_rst signal in clk cycles

Or_cnt_0 (0x00000C14)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Or_cnt_0	Read	0x00000000	Number of <Or> rising edges, lower 32-bits.

Or_cnt_1 (0x00000C18)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	Or_cnt_1	Read	0x00000000	Number of <Or> rising edges, upper 32.

Notes on Val registers:

- Set the < Val_width> and < Val_delay> registers. The sum of the 2 registers is the pulse period.
- Set the continuous or burst mode in < Asic_val_rst_or control> register, bit 1 (Val_mode)
- If Val_mode is set to burst, then set the number of bursts in the <Val_no> register
- Toggle Asic_rst (bit 2) in < Asic_val_rst_or control> register, in order to load the above values to the internal counters.
- Set Val_trig (bit 0) in < Asic_val_rst_or control> register, in order to start the Val pulses.

Notes on Rst registers:

- Set the <Rst_width> register.
- Toggle Asic_rst_rst (bit 4) in < Asic_val_rst_or control> register, in order to load the above value to the internal counter.
- Set asic_rst_trig (bit 3) in < Asic_val_rst_or control> register, in order to start the Rst pulse.

Address Range 5: Timestamp Fpga registers

Timestamp_fpga_control (0x00001000)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 2	Reserved	N/A	N/A	Reserved
4	asic_ts_rst_ val_mode	Read/write	0	0 = blocks sync_pulses from being the asic_ts_rst 1 = allows sync_pulses to be the asic_ts_rst
3	reserved	N/A	N/A	Reserved
2	reserved	N/A	N/A	Reserved
1	custom_clk_sel	Read/write	0	0 = selects internal 200MHz. 1 = selects external 200MHz.
0	custom_clk_rst	Read/write	0	0 = DCM not reset 1 = DCM reset

Notes:

External clk:

Cbs setup to external ("tclkc input term noinv tclka",
"tclkd input term noinv tclka",
"fpclka output term noinv tclkc",
"fpclkb output term noinv tclkd",
"fpclkc input term noinv tclka",
"fpclkd output term noinv fmc_clk0_m2c",
"fmc_clk0_m2c input term noinv tclka",
"fmc_clk1_m2c output term noinv tclkc")

PLL disable : to be confirmed

Clk_mux to external, (Timestamp_fpga_control (0x00001000), bit 1 = 1)
Reset custom dcm, (Timestamp_fpga_control (0x00001000), toggle bit 0)

Internal clk:

Cbs setup to internal ("tclkc input term noinv tclka",
"tclkd input term noinv tclka",
"fpclka output term noinv tclkc",
"fpclkb output term noinv tclkd",
"fpclkc input term noinv tclka",
"fpclkd output term noinv fmc_clk0_m2c",
"fmc_clk0_m2c input term noinv tclka",
"fmc_clk1_m2c output term noinv fpclkc")

PLL enable (reg2 = 0xE8
reg6 = 0x00
reg 10 = 0x00
reg 14 = 0x0A
reg 18 = 0x20
reg 22 = 0x01)

Clk_mux to internal, (Timestamp_fpga_control (0x00001000), bit 1 = 0)

Reset custom dcm, (Timestamp_fpga_control (0x00001000), toggle bit 0)

When the asic_val mode is set to asic timestamp reset (see r3b asic user manual), in software, then asic_ts_rst_val_mode should also be set.

Butis_Dcm_status (0x00001004)

Bit(s)	Name	Core Access	Reset Value	Description
31 - 2	Reserved	N/A	N/A	Reserved
5	custom_clk_locked	Read	0	0 = custom DCM not locked 1 =custom DCM locked
4	proc_clk_locked	Read	0	0 = processor DCM not locked 1 = processor DCM locked
3	Reserved	N/A	N/A	Reserved
2	Reserved	N/A	N/A	Reserved
1	BuTis_uncertain_o	Read	0	
0	BuTis_error_o	Read	0	

Place Asic reset status bit: asserted when at least 1 asic reset takes places after bitslip is done