Development of a Silicon Tracker and Front-End Electronics for R^3B

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by

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Abstract

A highly segmented silicon tracking detector has been constructed at the University of Liverpool that will form an integral part of the future R^3B (Reactions with Relativistic Radioactive Beams) experimental setup at FAIR (Facility for Antiproton and Ion Research). The requirements and design of the tracking detector are explained as well the tracker's functionality in relation to the other R^3B detectors. The tracking detector will provide high resolution position measurements and vertex capabilities that will significantly enhance the wide ranging physics programme that is anticipated for R^3B.

Individual detectors have been constructed by combining several silicon sensors with a double-sided stereoangle strip geometry. All sensors have a strip pitch of 50 μm to ensure high granularity. The tracker is formed of two types of detector which have a total of 4096 or 3072 independent strips. All silicon sensors used for detector construction have been subjected to a quality assurance process at the University of Liverpool. The different stages of the quality assurance process are described and the results for all accepted sensors are presented. The process by which detectors are produced is outlined and the final test data for each completed detector is presented.

The detector readout relies on an Application Specific Integrated Circuit (ASIC), which has been designed, at Rutherford Appleton Laboratory, specifically for the silicon tracker. A detailed description of the R^3B ASIC architecture is given and ideal operational amplifier calculations have been performed for the different pulse processing stages. A bare ASIC test setup has been assembled at STFC Daresbury, to develop an understanding of the performance of the pre-production ASIC (version two). An analysis of the results has identified issues which have been corrected for the final production ASIC (version three). The results of pre-production ASIC testing have been compared with the specifications and a discussion of the measurements of several key performance criteria is presented, along with theoretical calculations for comparison and verification.

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Chapter 1

Introduction

FAIR (Facility for Antiproton and Ion Research) is a new international accelerator facility, which is a further development of the existing GSI facility, near Darmstadt in Germany. FAIR signifies the continuation of a worldwide effort focussing on the development of rare isotope beam (RIB) accelerators, for the purposes of studying the structure of nuclear matter using short short-lived RIBs [1] [2]. Other such facilities that are currently operational or under construction include: RIBF (Radioactive Isotope Beam Factory) at RIKEN in Japan, FRIB (Facility for Rare Isotope Beams) at Michigan State University in USA, TRIUMF (TRI-University Meson Facility) in Canada and SPIRAL I and II at GANIL in France.

An essential component of the FAIR project is the double-ring heavy ion synchrotron (SIS100), which will deliver ion beams with substantially greater intensities and energies than the existing GSI facility. The R^3B experimental area will receive the highest energy RIBs available at FAIR. The aim of the R^3B (Relativistic Reactions with Radioactive Beams) collaboration is to construct a versatile experimental setup using relativistic radioactive beams across the full energy range of the SIS100. The experimental assembly is designed to conduct kinematically complete nuclear reactions in inverse kinematics with fixed targets. The R^3B silicon tracker is located closest to the target and consists of three separate layers of double-sided silicon detectors. The silicon tracker will provide important particle interaction information and enable vertex measurements. The silicon tracker has been designed and constructed by a team at the University of Liverpool. The front-end electronics are provided by STFC Daresbury and Rutherford Appleton Laboratories.

The silicon tracker is a highly segmented detector that enables high precision position measurements of charged particles, such as protons, which are emitted

from the target region. A new ASIC has been custom designed for the front-end electronics to cope with the high channel density of the tracker. Extensive testing of the R^3B ASIC has been conducted to verify its applicability for reading out signals ranging from high-energy protons to slow heavy ions.

This thesis will focus on the development and construction of the silicon tracker as well as testing of the front-end electronics. Chapter 2 gives an overview of the R^3B experiment and the importance of the silicon tracker. The silicon tracker's key properties and an example physics case are also discussed in Chapter 2. Chapter 3 introduces the principles of semiconductor technology with an emphasis on silicon and strip detectors. Chapter 4 describes the silicon sensors that have been used to construct the tracker and the quality assurance process by which each sensor has been tested. Chapter 5 introduces the R^3B ASIC design as well as the basic principles of analogue front-end electronics including ideal calculations. Chapter 6 presents a series of tests whereby programmable parameters of the ASIC have been tested and compared with ideal operational amplifier calculations. Chapter 7 outlines the current status of the silicon tracker and the R^3B ASIC testing results.

Chapter 2

FAIR and R^3B

An overview of the FAIR facility is given with a description of the accelerator stages and the beams that will be delivered to the R^3B experimental setup. The kinematic requirements of the R^3B experimental setup and the subsequent design of the R^3B detectors is explained. The key performance criteria and design of the silicon tracker are presented and the necessity of the tracker's inclusion in the R^3B experimental setup is justified.

2.1 FAIR

FAIR is a new facility that is currently under development. FAIR will be coupled with the previous GSI facility to deliver a range of ion beams of all elements up to uranium. The existing GSI facility will be equipped with a new proton linear accelerator to form the pre-accelerator and injector phase for the new FAIR project [3]. Figure 2.1 shows the layout of the new FAIR facility alongside the existing GSI facility. The addition of a double-ring heavy ion synchrotron (SIS 100/300) will significantly increase the intensity and energy of primary beams at FAIR. The primary ion beams exiting the SIS 100/300 are used to generate secondary ion beams up to 1.5 AGeV, which will be delivered to various experimental halls and storage rings at the FAIR facility such as the R^3B experimental setup.

For the first stage of acceleration, a low-energy beam of stable isotopes is extracted from the ion-source and injected into a universal linear accelerator (UNILAC), which can reach energies of up to 11.4 AMeV [4]. After the UNILAC, the stable-ion beam is accelerated up to 2 AGeV (for ^{238}U) courtesy of the SIS 18 synchrotron. A further stage of acceleration, up to 2.7 AGeV for uranium, will be

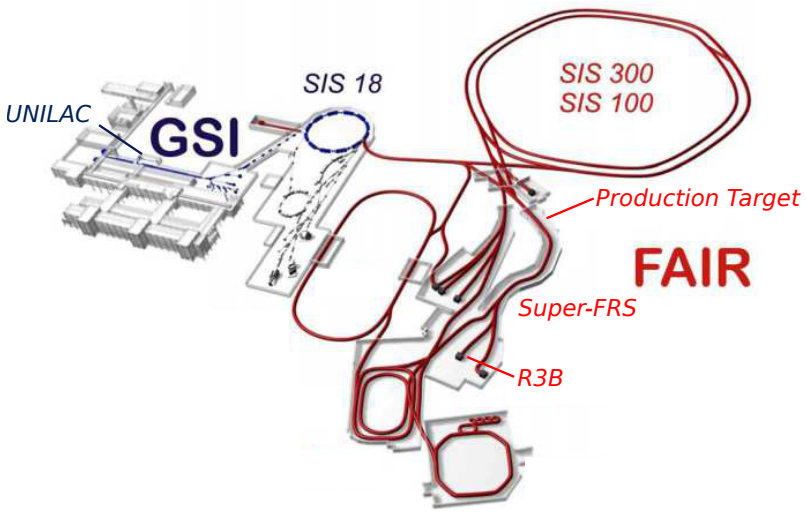


Figure 2.1: The new FAIR facility in Darmstadt, Germany. The Super-FRS delivers beams of unstable nuclei to the R^{3}B experimental facility.

achieved by the SIS 100 with a maximum intensity of 5×10^{11} particles per second [5], which represents a significant increase in intensity in comparison with the existing GSI facility. When completed, the SIS 300 will be capable of delivering primary beams of uranium 92^+ with energies up to 35 AGeV (89 GeV for protons). Primary beams circling the SIS 100/300 can be compressed resulting in short bunches of 50-100 ns in duration or alternatively form continuous beams with average intensities of up to around 3×10^{11} ions per second.

Secondary radioactive ion beams (RIBs) can be produced via the in-flight fragmentation process [6], by impinging the SIS 100/300 primary ion-beam upon a thin rare isotope production target. The rare isotope production target is positioned after the double-ring synchrotron. A higher energy primary beam allows the use of thicker production targets, which enables FAIR to achieve significantly higher secondary beam intensities than the previous GSI facility. The resulting radioactive ion fragments are then separated according to their magnetic rigidity by a series of superconducting dipole magnets to produce a RIB. The RIB can then be tracked on to another fixed target within a given experimental hall. At FAIR, the process of separating the radioactive isotopes will be performed by the Superconducting FRagment Separator (Super-FRS) [7], which is designed to produce a broad range of secondary RIBs at energies up to 1.5 AGeV.

FAIR will produce the highest energy RIBs in the world, which will provide the opportunity to probe exotic nuclear matter at higher densities than ever before. The NUSTAR (NUclear STructure, Astrophysics, and Reactions) collaboration aims to

exploit the physics opportunities offered by such RIBs. The NUSTAR high-energy experimental area is the R^{3}B hall located at the focal plane of the high-energy branch of the Super-FRS.

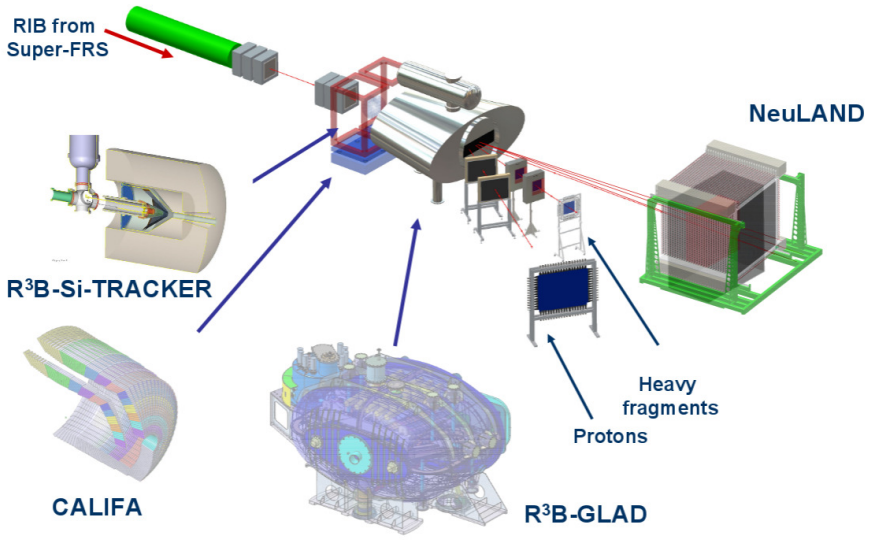


Figure 2.2: The R^{3}B setup with its main constituents: the silicon tracker and the calorimeter CALIFA surround the target region. The neutron time-of-flight spectrometer NeuLAND and the heavy-fragment tracking detectors are positioned downstream from the dipole magnet R^{3}B-GLAD.

2.2 R^{3}B Experiment

The purpose of the R^{3}B collaboration is to construct a versatile setup for fixed target experiments with high efficiency, acceptance and resolution to conduct kinematically complete measurements of reactions with high-energy RIBs [8]. High-energy RIBs with intensities up to 10^9 pps [9] are foreseen, resulting in event rates ranging from 1-10^4 pps. Reaction experiments using exotic nuclei at relativistic energies are a proven tool for accessing the intrinsic structure of such nuclei [10], furthermore R^{3}B is the only experiment capable of providing such measurements with relativistic beams up to around 1.5 AGeV (upper limit of energy is constrained by the maximum magnetic rigidity of 20 Tm of the Super-FRS magnets). The experimental configuration has been designed to provide improved granularity and to accommodate the higher event rates and energies with greater efficiency than the previous setup. The flexibility of the setup enables R^{3}B to cover a range of experiments with different reaction types and physics goals. Experiments conducted where a high-energy RIB is incident on

a fixed target will emit an array of different particles. The processes by which the particles are detected are different depending on how the particle interacts with matter.

The interaction between an incoming beam-ion and a fixed target will result in the emission of several particles such as protons, neutrons, gamma rays and heavy ions. The fixed target setup and beam energies greater than tens of MeV, means that the majority of beam-like (heavy-ion) emitted fragments are forward-focussed. Heavy fragments will thus travel downstream from the target region at small angles relative to the beam axis. The lighter target-like fragments will be less forward focussed than the beam-like fragments.

An array of particle detectors are positioned around the target and downstream of the target. This enables the study of the structure of beam nuclei using inverse kinematics. Figure 2.2 shows the R^{3}B experimental configuration that is capable of detecting light charged particles, gamma rays, heavy ions and neutrons. The energy loss and position of all emitted species will be measured using the full experimental setup.

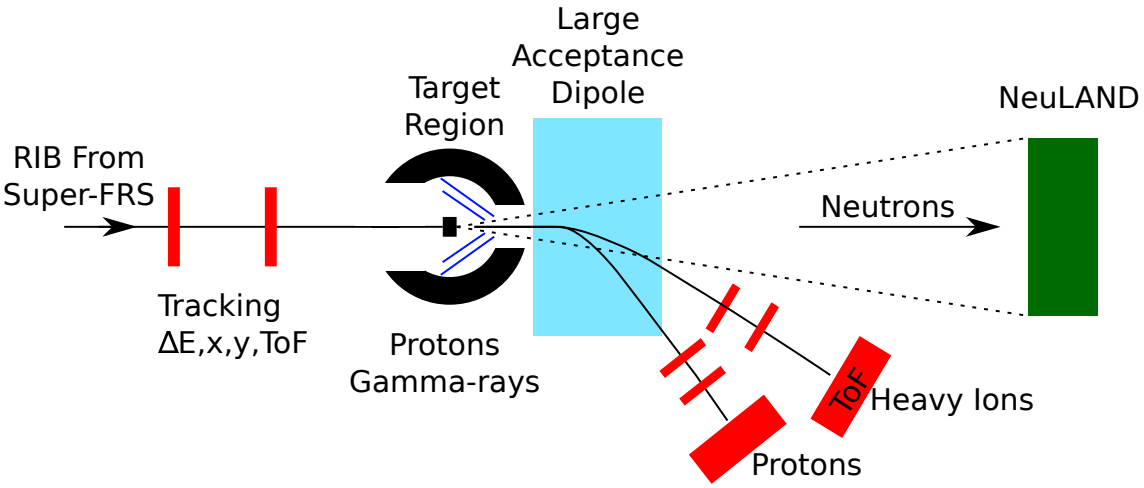
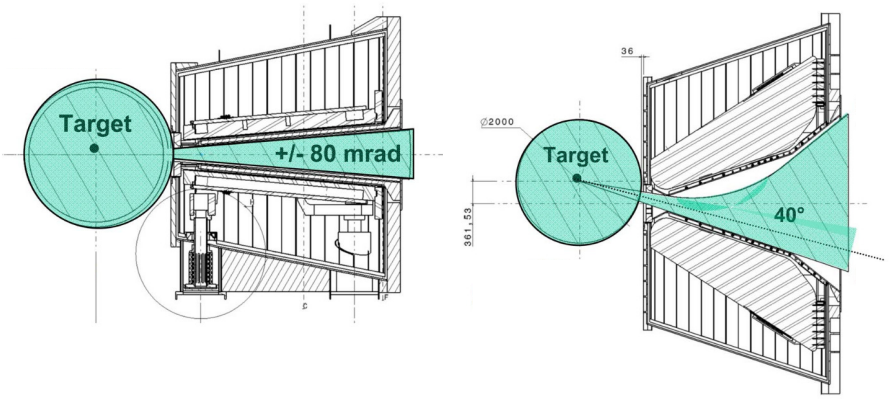


Figure 2.3: A schematic of the experimental set-up. The target region is surrounded by the silicon tracker (blue lines) and a large calorimeter (black). Neutrons are detected by NeuLAND (green) and beam-like particles are tracked before and after the dipole magnet by an array of detectors (red).

2.2.1 Heavy Ion Identification

A schematic of the R^{3}B detector configuration is shown in Figure 2.3 displaying the relative positions of the various detectors and trajectories of particles. An incom-

ing beam ion can be tracked prior to becoming excited by an interaction with a target nucleus, which allows the beam momentum, angle and position to be determined. Beam tracking is achieved using a series of detectors positioned upstream of the target. After the interaction; the R^{3}B-GLAD (GSI Large Acceptance Dipole) superconducting magnetic spectrometer [11] will bend the trajectories of forward emitted heavy beam-like particles, which are then incident upon an array of tracking detectors positioned at known angles relative to the beam axis. The GLAD superconducting magnet allows the bending of the trajectories of beam-like heavy ions due to the Lorentz force. The trajectories of the beam-like particles can thus be tracked before and after the interaction providing mass identification and momentum measurement. The GLAD superconducting magnet has been designed with a $\pm$ 80 mrad inlet aperture providing large acceptance both horizontally and vertically (see Figure 2.4a). The inner vacuum chamber of GLAD is shaped such that the trajectories of heavy ions and protons can be deviated by up to 40° in the horizontal plane as shown in Figure 2.4b.



(a) Side view of GLAD. (b) Top view of GLAD.

Figure 2.4: The GLAD superconducting magnet has an 80 mrad inlet aperture and allows particle trajectories to be bent by up to 40° in the horizontal plane [11].

The final tracking detector, positioned furthest from the target, is the ToF (Time-of-Flight) wall. The time taken for a particle to travel from the target to the ToF wall is known as the time-of-flight and can be used to determine a particle's velocity $\beta = \frac{v}{c}$ according to the expression

$$\text{ToF} = \Delta t = \frac{L}{c\beta}, \tag{2.1}$$

where L is the distance from the target to the ToF scintillator detector. Increasing

the distance from the target to the scintillator detector improves the ToF resolution and thus the velocity resolution ($L \approx 20$ m). The energy loss ΔE of a charged particle in a material is a function of the particle's charge ($\propto Z^2$) and velocity ($\propto \beta^{-2}$). Therefore, combining the measurements of ΔE and β allows the particle's charge Z to be determined. The Lorentz force due to the magnetic field bends the charged particle's trajectory resulting in a circular track with radius ρ. Magnetic rigidity $B\rho$ is a property that determines the effect of a magnetic field on a particle's trajectory depending on its momentum and charge and is given by

$$B\rho = \frac{p}{q} \propto \frac{A}{Z}, \tag{2.2}$$

where B is the magnetic field in Tesla, p is the particle's momentum, q is the charge, A is the mass number and Z is the particle's charge. A high momentum particle will have a straighter path than a low momentum particle of the same charge.

By measuring the position of the interaction with the tracking detectors, the radius of curvature ρ can be determined for a particle. Measuring a particle's velocity and its magnetic rigidity allows individual isotopes to be distinguished according to their mass to charge relationship [12] [13](ΔE vs ToF).

2.2.2 Neutron Measurement

FAIR has the capability to deliver neutron-rich RIBs to the R^{3}B experimental setup, hence many experiments at R^{3}B require neutron detection. Neutron-rich beams will result in a range of experiments where several free neutrons are emitted from the target region per interaction and thus neutron detection in coincidence with other emitted species is essential for kinematically complete measurements [14]. The path of a high-energy neutron emitted from the target region will be forward focussed and pass through the magnetic spectrometer. The path of a neutron is unaffected by the magnetic spectrometer and the neutron detector is accordingly positioned along the beam axis after the magnetic spectrometer. A neutron position and time of flight measurement determines the neutron's velocity and hence its momentum.

2.2.3 Light Charged Particle and Gamma-ray Measurement

Light target-like species that are emitted from the target region will be less forward focussed meaning a system of detectors surrounding the target is required. The target region is surrounded by two detectors. The innermost detector is the

silicon tracker, which primarily provides high-resolution position and energy loss measurements. The second detector encloses the tracker and provides full calorimetry measurements of tracked charged particles. The combination of both detector systems allows a precise measure of a charged particle's trajectory as well as its total kinetic energy, which is essential for the physics programmes envisaged at R^{3}B.

Light charged particles such as protons will be emitted in coincidence with gamma rays. The gamma rays will pass through the tracker undetected and the position and energy is measured only by the calorimeter. The calorimeter and tracker have been constructed to cover a range of possible angles. Close attention has been paid to the most forward angles to ensure the detection of high-energy forward focussed protons for beam energies up to 700 AMeV, corresponding to protons at $\approx$ 320 MeV in the most forward directions.

2.3 R^{3}B Detectors

The R^{3}B experimental setup utilises a range of different particle detectors in order to measure the energy, time and position of heavy ions, protons, neutrons and gamma rays. A range of detection technologies are applied depending on the essential physics requirements such as timing, position or energy resolution whilst considering the system cost. The geometries and various materials that are utilised by the R^{3}B detectors are outlined.

2.3.1 In-Beam Tracking Detectors

The R^{3}B tracking detectors employ a range of detection principles using silicon, scintillator and gas detection mediums [15] to measure the energy and position of heavy ions and protons. Fast timing measurements are achieved using fast scintillators, which also yield energy loss information. Position and energy loss measurements are obtained by a combination of silicon detectors and thin plastic scintillator fiber detectors. Straw-tube gas detectors are also used for the tracking of protons after the dipole magnet.

Straw-tube detectors [16] operate similarly to proportional chambers with a single anode wire encased in a long aluminium tube which forms the cathode. Roughly 700 straw-tubes of diameter 10 mm and approximately 1 m in length will be used to construct four straw-tube walls. The walls are constructed from horizontally and vertically positioned straw-tubes which offers two-dimensional position resolution.

Each wall contains three layers of straw-tubes each having a 25 μm gold-plated tungsten anode wire with a range of possible gas mixtures.

A thin plastic scintillator (LOS) with dimensions 55×55×0.5 mm^3 [17] is positioned before the target which provides fast timing measurements ($<$ 10 ps RMS resolution) to accurately determine the start time of the reaction. Thin silicon detectors and fiber detectors can be positioned before and after the target to determine a particle's charge and position. The ToF wall is constructed from scintillator material due to the fast timing response capabilities ($\approx 50 - 100$ ps RMS resolution). The time-of-flight is determined by the difference in time between the LOS detector and the ToF wall. The timing resoution of the ToF wall and thin plastic scintillator LOS are therefore crucial to the accuracy of the experiment.

The large plastic scintillator ToF wall is positioned after the magnetic spectrometer with dimensions 120 × 80 cm^2. The R^{3}B ToF wall consists of four planes of plastic scintillators where each plane is made up of 44 individual scintillator paddles that are each coupled to two PMTs (photomultiplier tube) [18]. The ToF wall operates in conjunction with other fibre scintillator detectors [19] which are positioned closer to the magnetic spectrometer to provide full tracking. Several position sensitive fibre scintillator detectors have been developed, one example consists of 1024 square fibers each with a profile of 250 × 250 μm which are coupled to multianode PMTs and fully cover the active area of the ToF wall. The position of protons downstream of the magnetic spectrometer are measured with a position resolution on the order of 200 μm by virtue of the array of straw-tube gas detectors.

2.3.2 NeuLAND

Neutrons are chargeless and so exhibit no electromagnetic properties by which they may interact with a medium. Neutrons can only interact via the strong nuclear force, which has a smaller interaction probability cross section due to the short range of the nuclear force, meaning neutrons are capable of penetrating several centimetres or more into matter before interacting. Neutron detection therefore requires a relatively thick detecting medium.

When a neutron does interact with a nucleus of the medium there are a number of possibilities depending on the neutron's energy. For example, the neutron may scatter off the nucleus inelastically or elastically or the neutron may be captured by the nucleus resulting in an excited nuclear state. The sum of the individual cross sections is σ_{tot} that is given by

$$\sigma_{tot} = \sigma_{elastic} + \sigma_{inealstic} + \sigma_{capture}, \tag{2.3}$$

which represents the probability of a neutron interaction occurring [20].

Elastic scattering is the dominant interaction for high-energy neutrons. A high-energy neutron (> 100 MeV) will lose energy by scattering both inelastically and elastically until it has slowed sufficiently to enable neutron capture to ensue. When captured, the excited nucleus can either de-excite by emitting a gamma ray or a form of charged radiation resulting in heavy charged particles. Therefore neutrons are only detected through indirect or secondary ionisation processes. If a neutron scatters off a heavy nucleus, the neutron will retain more of its kinetic energy than the case where a neutron collides with a particle of similar mass such as a proton. Neutrons can thus be slowed down most efficiently by using a proton or light-nuclei rich absorbing medium [21].

NeuLAND [22] (New Large-Area Neutron Detector) is a neutron time-of-flight detector, which is positioned along the beam axis after the magnetic spectrometer within the R^{3}B experimental cave. In its entirety, NeuLAND is constructed from 3000 individual organic (RP408) plastic scintillator bars, each with a size of $5 \times 5 \times 250$ cm^3. The modules are arranged in double planes consisting of 100 modules, where 50 modules are positioned horizontally and the other 50 modules are vertically arranged. Therefore the active face area presented by NeuLAND is 250×250 cm^2 with a total of 30 double planes resulting in a depth of 3 m. Every plastic scintillator module is connected to a PMT at the two ends, which allows the position resolution along the length of the module to be determined by the time difference between two signals.

2.3.3 CALIFA

The CALIFA (CALorimeter for In Flight detection of γ-rays and high-energy chArged particles) calorimeter is a large scintillator array that surrounds the silicon tracker and reaction target and provides full-energy measurements for protons, light ions and gamma rays. The calorimeter consists of two sections; a forward end cap [23] and a barrel section [24]. The barrel section consists of 1952 CsI(Tl) crystals providing high angular resolution over an angular range from 43.2° to 140.4° (see Figure 2.5). The beam-line is defined as being at 0°, angles between 0° and 90° correspond to the region downstream from the target region and angles between 90° and 180° are upstream of the target region.

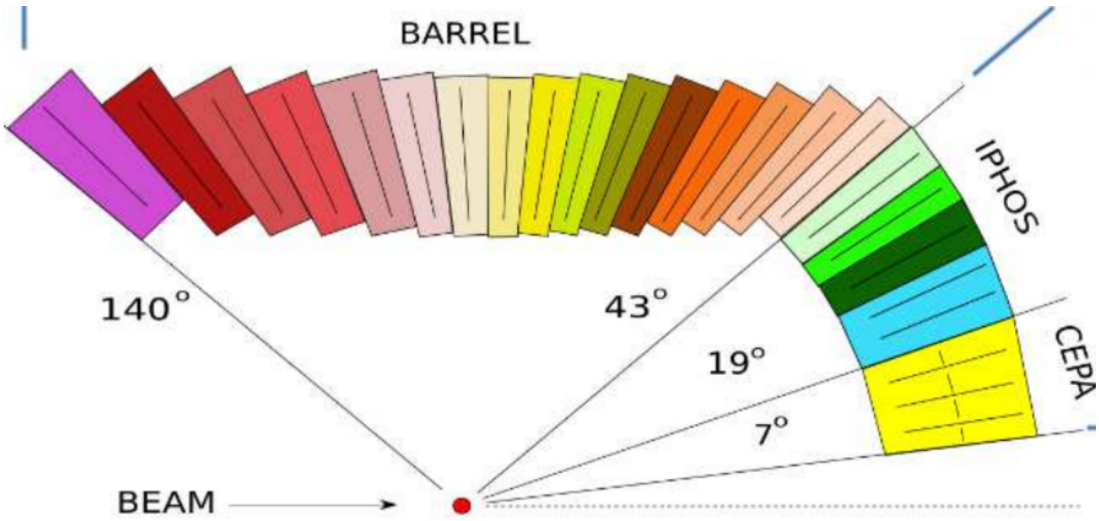


Figure 2.5: The CALIFA barrel angular coverage ranges from 7° to 140° with the end cap (IPHOS and CEPA) covering the most forward angles [24].

One of the key requirements of the R^{3}B setup is to study reactions with high-energy protons in coincidence with gamma rays. An end cap has been included to cover an angular range from 7.0° to 43.2° to ensure the detection of high-energy forward-focussed protons and gamma rays. The end cap consists of 608 scintillator crystals, utilising a combination of La_3Br:Ce and La_3Cl:Ce for the most forward angles and CsI(Tl) for the remainder of the end cap [25]. The use of La_3Br:Ce La_3Cl:Ce scintillator crystals provides better energy resolution and greater detection efficiency at the most forward angles where the majority of gamma ray and protons are expected due to foward focussing of the emitted particles.

The depth of the end cap scintillator crystals is 22 cm to ensure that high-energy protons are completely stopped within the crystal, to ensure full energy measurements for protons with kinetic energies up to about 320 MeV. The shape and size of the crystals has been designed to provide adequate granularity to allow determination of the emission angle of gamma rays, which is necessary for applying Doppler corrections whereby the gamma ray energy can be calculated in the rest frame of the excited projectile remnant. The regions below 7° and above 140.3° are not covered by the calorimeter. The opening in the backward hemisphere (140.3° to 180°) is necessary to provide adequate space for the target support structure and readout electronics for other detection systems.

The calorimeter can provide full-energy measurements of the emitted charged particles, however the position resolution is limited by the crystal size. A total of 11

crystal sizes are used for the calorimeter, the dimensions of a typical frustum-shaped crystal are of the order $22 \times 2 \times 4$ cm^3. All crystals are arranged in a cylindrical formation with the longest axis oriented towards the target. In order to achieve high precision position resolution measurements for light charged particles, another more highly segmented device is required. The calorimeter has therefore been designed to allow the installation of a smaller tracking detector within the barrel radius.

2.4 Silicon Tracker Design

The silicon tracker represents a substantial component of the R^{3}B setup which is essential for the detection of light target-like particles. The silicon tracker system is closest to the target, within the vacuum of the beam pipe, and provides high granularity x, y, z coordinates for charged particle trajectories emanating from the target. The tracker is constructed from double-sided silicon to form three independent layers allowing vertex reconstruction with a position resolution of approximately 1-2 mm (rms), which facilitates the use of thick targets (several cm). The primary purpose of the tracker is to provide high-resolution position measurements for charged particles (mainly protons) as they pass through the three layers of silicon sensors whilst recording the time and energy loss of the interactions. The total energy deposited by a light charged particle will be obtained by summing the energy deposited in the three silicon layers and the CALIFA scintillator crystals. The k_x, k_y and k_z components of the total momentum vector $\vec{k}$ can therefore be determined using the silicon tracker's position information in conjunction with the total energy information.

The three layers of double-sided silicon are shown in Figure 2.6 where the inner layer is situated closest to the beam axis. The two outer layers are positioned further away from the beam axis and separated from each other by about 1 cm. The inner layer is positioned close to the target in order to improve the vertex reconstruction capabilities whilst reducing the size and cost of the assembly. The geometry is such that the tracker covers an angular range of 6° to 102° allowing the most forward focussed and highest energy protons to be tracked and stopped within the crystals of CALIFA. Two layers is the minimum requirement for particle tracking. A third layer is included in the design to negate strip redundancy so that at least two interaction positions are always recorded thereby allowing greater efficiency for vertex reconstruction. The design specification requires the percentage of dead channels in each layer to be less than 3%.

Two design options were initially investigated; the first was a barrel design with

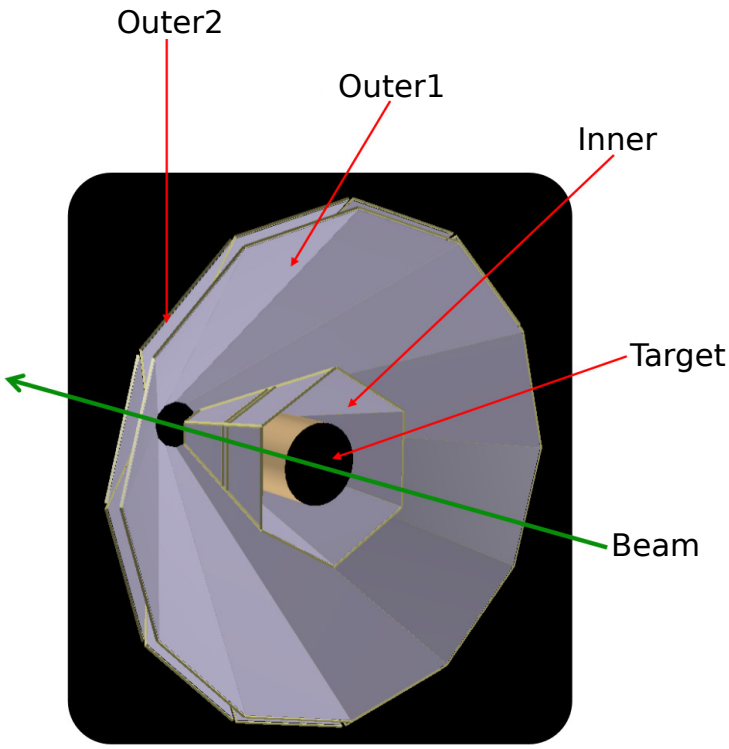


Figure 2.6: Silicon tracker design showing two outer layers and one inner layer in a lampshade configuration.

two silicon layers running parallel to the beam axis and the second was the lampshade configuration. The lampshade geometry was the more favourable for two key reasons. Firstly the angle of the silicon relative to the beam axis allows a more uniform effective thickness across the full length of the sensor. The barrel geometry would have resulted in the most forward focussed (highest energy) particles experiencing a greater sensor thickness than particles emitted at 90° to the beam axis. The barrel geometry would have therefore resulted in greater straggling and multiple Coulomb scattering for the most forward angles, where the highest number of tracks is expected. Secondly, the lampshade configuration facilitates the use of trapezoid silicon sensors, which allows a strip geometry (see section 4.1.1) such that all front-end electronics, cooling and mechanical support can be positioned at backward angles relative to the target and thus away from particle tracks. A typical barrel geometry with double-sided orthogonal strips would have required an electronic readout on two sides of the sensor. A two-sided readout would have resulted in at least part of the electronics residing between the target and CALIFA, thereby interfering with particle tracks. A barrel geometry using sensors with double met-

Table 2.1: Summary of the properties of each layer of the silicon tracker.

Layer	Detectors	Area (cm^2)	No. of ASIC	Channels	Beam Distance (cm)
Inner	6	722	144	18432	7.21 to 1.82
Outer1	12	2426	384	49152	20.40 to 2.37
Outer2	12	2426	384	49152	21.55 to 3.52

allisation would have allowed the readout to be positioned on just one side of the sensor, however this would have increased the material budget and sensor cost in comparison to the trapezoid sensors that have been used.

Each strip of a sensor acts as an independent electrode and collects the signal generated within the bulk material due to incident radiation. The attainable position resolution is limited by the strip pitch of 50 μm. This strip pitch was selected to provide an angular resolution of the order of a few mrad whilst guaranteeing a suitable hit rate per strip to avoid pile-up. The outer layers have been designed such that the strip length is long enough to extend to the most forward angles whilst allowing the electronics and support structure to be situated far enough upstream. The maximum strip length is limited by the hit rate and capacitance per strip, a longer strip will cover a larger solid angle and thus experience a greater hit rate whilst the larger capactitance will increase the noise of the strip. The signal charge collected by an electrode, due to energy deposition within the bulk, will depend on the properties of the charged particle as well as the effective thickness of the silicon. A sensor thickness of 300 μm has been selected to limit the effects of multiple Coulomb scattering whilst ensuring that signals are sufficiently large to be detected above the noise level of the system. The possibility of 100 μm silicon sensors was investigated for the inner layer, but concerns regarding the signal to noise ratio and sensor procurement supported the use of 300 μm silicon sensors for all layers.

Double-sided sensors were selected in order to minimise the material thickness whilst providing a measure of the traversing particle's energy. The three layers are referred to individually as inner, outer1 and outer2. The inner layer consists of six separate detectors in a conical arrangement that are situated closest to the beam axis. The outer1 layer is made up of twelve separate detectors that are situated further from the beam axis. The outer2 layer consists of another twelve detectors, which are the same design as the outer1 layer detectors, but positioned further from the beam axis. The properties of the layers are summarised in Table 2.1. The number of channels for the fully assembled tracker is 116736 and equates to a total sensitive area of approximately 5600 cm^2. The high channel density requires the use

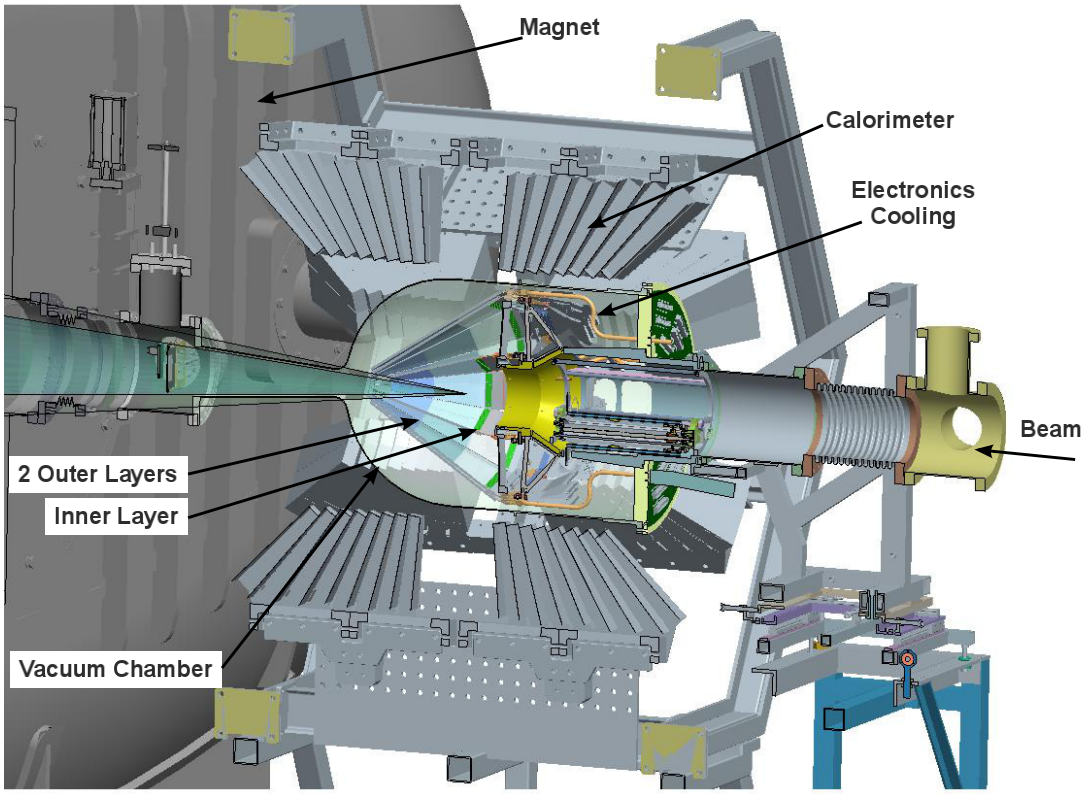


Figure 2.7: Schematic of the silicon tracker's position in the final experimental setup.

of a custom made ASIC (Application Specific Integrated Circuit) for the electronic readout which is described in Chapter 5. The ASIC has a quoted dynamic range of 40 keV to 50 MeV to allow tracking of high-energy protons and heavy ions.

The silicon tracker is situated within the beam pipe and must therefore be operated under vacuum conditions ($\approx 10^{-8}$ bar). The tracker is housed within its own vacuum chamber with 2 mm thick aluminium walls, which connects to the beam pipe as shown in Figure 2.7. During operation, heat generated due to ASIC operation is removed from each detector by cooling a copper block via an external chiller. The silicon tracker's ASIC has been custom designed with power consumption as a key consideration to ensure detectors can be operated under vacuum at about 20°C. The silicon tracker's vacuum chamber is surrounded by the calorimeter.

2.5 Silicon Tracker Physics Case

The silicon tracker and CALIFA surround the target region and are essential for a large part of the physics programme of R^{3}B. The silicon tracker allows the detection

and tracking of target-like recoils in coincidence with heavy fragments, neutrons and gamma rays when used as part of the complete R^{3}B setup. A recoil detection system (silicon tracker and CALIFA), coupled with GLAD and the downstream detection systems thus enables the study of (in)elastic scattering as well as direct reactions such as transfer and knockout reactions for isospin asymmetric nuclei [26] [27]. Direct reactions that typically involve the participation of just a few bodies have been widely used in the past to study stable nuclei using normal kinematics. Nuclear structure information can be discerned for nuclei far from stability by employing reactions using inverse kinematics [28], where a RIB is incident upon a light stable target.

Nucleon transfer reactions, whereby one or more nucleons are exchanged between the projectile and target, have been exploited to study single-particle states by reconstructing the excitation energy spectrum [29]. Transfer reactions such as (d, p) and (p, d) which probe the proton and neutron valence states by adding or removing nucleons, require the detection of light recoils and gamma rays in coincidence with the projectile. Ion beam energies around 100 AMeV or more [30] result in small cross sections for transfer reactions and for such energies knockout reactions are more favourable for studying single-particle states [31]. Knockout reactions occur when a nucleon is removed from the projectile nucleus due to an interaction with a target nucleon. A knockout reaction such as $(p, 2p)$ or (p, pn) removes a nucleon thereby leaving a hole state at a particular energy level within the nucleus, which may subsequently breakup or de-excite via gamma-ray emission. At beam energies greater than 100 AMeV, the reaction mechanism is simplified such that a semi-classical approximation of the reaction between projectile and target becomes valid (see section 2.5.1). The secondary beams at R^{3}B will allow the study of knockout reactions via kinematically complete measurements of projectile, recoils, gamma rays and projectile-like fragments.

For the case of single proton knockout, the removed proton will be forward emitted and pass through the three layers of the silicon tracker and each layer will measure an energy loss and a position for the proton interaction. The position measurements can be used to reconstruct the proton's trajectory and the measured energy loss can be added to the energy deposited in the calorimeter to obtain a total energy measurement. If a hydrogen target is used, the proton from the target will obtain a similar kinetic energy to the removed proton with a forward focussed trajectory. If the second proton from the interaction is also tracked, then the trajectories of the two protons can be reconstructed and the location (vertex) at which the

interaction occurred can be precisely determined with a precision of about 1-2 mm. The process whereby the interaction vertex is determined allows the use of much thicker and heavier targets, which improves the experimental yield and reduces the time required to accumulate sufficient data.

Previous proton scattering experiments have been carried out with a proton-rich CH_2 target that requires the use of a complementary carbon target to identify unwanted background events due to reactions with the carbon in the CH_2 target. The silicon tracker has been designed to allow the inclusion of a liquid hydrogen target as well as standard foil targets. A thick liquid hydrogen target (100-250 mg/cm^2) of more than 3-4 cm in length requires a detector capable of locating the interaction vertex within the target volume with high precision. Accurately locating the vertex allows the energy loss of the recoil particles in the target material to be accounted. The tracker and its associated electronics have been designed to cope with event rates as high as 5 kHz/ch to allow experiments with intense secondary beams and a liquid hydrogen target. The use of thick heavy targets would be impossible without the silicon tracker, as the vertex could not be accurately reconstructed and energy straggling within the target volume and angular uncertainty would severely impact on the measurements.

As well as providing vertex measurements, the tracker may be used to provide high-granularity, energy and multiplicity measurements with high efficiency and acceptance for charged particles. Such capabilities are highly desirable for measuring the energies and angular distributions of fragments emitted from heavy-ion collisions [32].

2.5.1 Quasi-Free Scattering

When a high-energy projectile induces the knockout of a nucleon from a nucleus and the nucleon is not influenced by the spectator nucleons, the process is deemed to be quasi-free. Quasi-free scattering (QFS) reactions in inverse kinematics require incident beam energies in the range 100-1000 AMeV [33]. In this energy range the direct knockout of a proton from the nucleus ${}^{A}Z$ yields a reaction ${}^{A}Z(p,2p)^{A-1}(Z-1)$ when a beam is directed onto a proton target such as liquid hydrogen. The two scattered protons and the ${}^{A-1}(Z-1)$ fragment carry important nuclear structure information concerning the properties of the knocked-out proton prior to its removal [34] [35]. At these energies the nucleon-nucleon cross section is minimised and the mean free path of the knocked-out proton is similar in magnitude to the nuclear

radius, meaning that the proton can be assumed to depart the nucleus without interference from spectator nucleons, which simplifies the reaction. Whereas transfer reactions and knockout reactions are limited to the valence nucleons at the nuclear surface, quasi-free scattering reactions permit the study of valence and deeply bound nucleons.

At R^{3}B, proton-proton $(p, 2p)$ quasi-free scattering in inverse kinematics using the silicon tracker will allow studies of single-particle states for exotic nuclei, thereby revealing shell structure evolution effects for nuclei near the neutron drip-line. In-medium effects such as the nucleon-nucleon interaction and its dependence on N/Z asymmetry as well its density dependence will also be probed through QFS reactions. Studies of clusterisation of the core in exotic nuclei will be pursued through quasi-free scattering reactions of the form $(p, p\alpha)$ and (p, pd) for example.

A high-energy proton with momentum $\vec{k_0}$ incident upon a bound nucleon will scatter as if both particles are free. The bound nucleon will be removed from the nucleus thereby forming a hole in the (A-1) nucleus. Assuming that the nucleon does not interact with the spectator nucleons, applying conservation of momentum and energy produces the following expression

$$\vec{k_{A-1}} = \vec{k_0} - \vec{k_1} - \vec{k_2} = -\vec{k_3} \ , \tag{2.4}$$

where the target nucleus is at rest. The momentum vector for the two scattered protons is represented by $\vec{k_1}$ and $\vec{k_2}$, and $\vec{k_3}$ is the internal momentum of the proton inside the nucleus prior to scattering. The recoil momentum of the (A-1) fragment is therefore equal and opposite to the internal momentum of the knocked-out proton. There are two possibilities by which the internal momentum of the scattered proton can be determined, either by measuring the momentum of the incoming proton and the two outgoing protons or by measuring the momentum of the (A-1) fragment. The inclusion of the silicon tracker will enable accurate determination of the momentum components k_x, k_y, k_z for the two scattered protons, thereby allowing a measure of the internal momentum of the initally bound proton with no knowledge of the (A-1) fragment required. Applying the conservation of energy, the binding energy of the bound nucleon B_N can be expressed as

$$B_N = T_0 - (T_1 + T_2 + T_{A-1}) \ , \tag{2.5}$$

where B_N is the nucleon binding energy, T represents the kinetic energy where

particle 0 is the incoming proton, 1 and 2 are the emitted protons and (A-1) is the fragment possessing the hole state. Measuring the kinetic energy of all species before and after the reaction with the target allows the energy of the single-particle state to be determined. Reconstructing the binding energy spectrum is expected to reveal peaks for certain energies corresponding to nuclear shells within the nucleus from which the nucleons are removed. The binding energy and the internal momentum of a nucleon can then be correlated with a specific shell.

A signature of a typical QFS event is a strong spatial correlation of the two emitted protons, which can be easily identified by the tracker. Beam energies ≥ 100 MeV resulting in kinematical focussing of the two protons will result in a difference in polar angle (relative to beam axis) in the laboratory between the two protons of $\Delta\theta < 90°$. The two emitted protons are expected to have an azimuthal separation angle of $\Delta\phi \approx 180°$. A pilot experiment was conducted using the previous LAND-ALADIN setup with a ^{12}C beam at 400 AMeV, which resulted in an opening angle of $\Delta\theta \approx 80°$ [36]. The position resolution and angular coverage of the silicon tracker will be greatly beneficial when identifying associated pairs of protons from quasi-free scattering reactions.

The knock-out of a deeply bound proton results in the (A-1) fragment obtaining an excitation energy $E*$ related to the energy level of the single-particle state, which is greater for more deeply bound protons. The binding energy of the removed proton B_p can be revealed by directly measuring the excitation energy

$$B_p = S_p + E* \ , \tag{2.6}$$

where S_p is the proton separation energy. The magnitude of the excitation energy of the (A-1) fragment means de-excitation will occur via either gamma-ray emission or breakup for bound and unbound states, respectively. The gamma-ray energies can be measured by CALIFA whereas the breakup fragments produced by unbound states, can be measured by the detector systems positioned downstream of GLAD. The invariant-mass technique [37] will be used at R^{3}B for reconstructing the excitation energy of unbound reaction products by detecting all breakup products. The invariant-mass M_{in} for a nucleus A breaking up to form a nucleus (A-1) and a nucleon N can be expressed as

$$M_{in} = \sqrt{(E_{A-1} + E_N)^2 - (|\vec{P_{A-1}} - \vec{P_N}|)^2} = \sqrt{E_{total}^2 - \vec{P_{total}^2}} \ , \tag{2.7}$$

where E_{total} and P_{total} are the total energy and momentum of the breakup reaction products. The rest mass of the system before breakup M_A is equivalent to the invariant-mass such that for an initial system prior to breakup, with excitation energy $E*$ the invariant mass is given by

$$M_{in} = M_A + E* \ . \tag{2.8}$$

The possibility of kinematically complete measurements at R^{3}B thus allows the excitation energy and internal momentum to be measured for single-particle states for bound and unbound systems. The silicon tracker will enable clear identification and selection of quasi-free scattering events.

Chapter 3

Semiconductor Detectors

The fundamental principles of radiation detection are covered with an overview of semiconductor detector technology. The properties of n-type and p-type doped silicon are explained in detail and the properties of the p-n junction and its application for radiation detection is demonstrated. A theoretical description of signal charge formation is given as well as the essential concepts of silicon strip detectors.

3.1 Radiation Detection Principles

Radiation detectors require the interaction of radiation within a material resulting in the deposition of energy. This energy deposited is then converted into an electronic signal and processed by an electronic readout.

The application of semiconductors and gaseous detectors for the purposes of radiation detection are well established due to their ionising properties, which facilitate the formation of mobile electrons within the sensitive volume due to passing radiation. The mobile charge carriers (electrons and holes) generated within a semiconductor are analogous to the electron-ion pair generated in a gaseous detector. Radiation can interact with gas molecules resulting in ionisation, a typical gas molecule can require about 30 eV to form an electron-ion pair. Semiconductor materials typically have a band-gap energy on the order of 1 eV [38]. The number of charge carriers generated in a semiconductor is approximately ten times greater than for a gaseous detector. The greater density of a solid medium further increases the number of generated charge carriers.

The basic principles of operation for a semiconductor detector are akin to those of a gaseous ionisation chamber. The active medium is enclosed by a pair of elec-

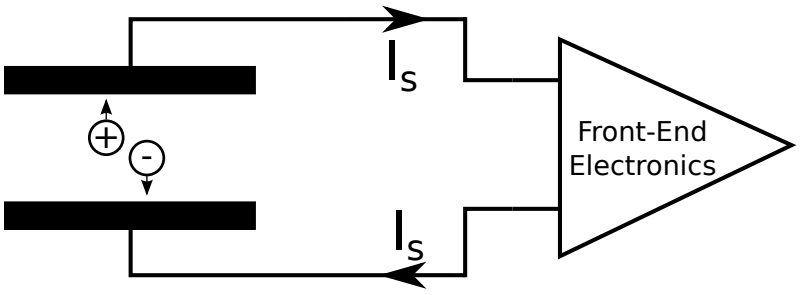


Figure 3.1: The basic detection principle where a pair of electrodes bound a sensitive region and a signal current I_s arises that can be measured. The current signal is extracted by the front-end electronics for further processing.

trodes. Applying a voltage to the electrodes, establishes an electric field within the sensitive detector volume. This causes ionised charge to drift with negative and positive charges moving in opposite directions. This motion of charges induces an electrical signal in the nearby electrodes (see Figure 3.1). The magnitude of the induced electrical signal is proportional to the initial deposited energy. The current signal I_s is then extracted by an external circuit for further processing and analysis. Depending on whether the sensing medium is semiconductor or gaseous, the charge collection and signal processing techniques can vary. This work will focus on discussions based around semiconductor detectors for tracking applications.

3.2 Semiconductor Properties

The use of semiconductor devices for radiation detection is a well established technology, which has many desirable properties. A solid detection medium means small and thin detectors can be constructed which retain sufficient density to ensure ample charge carrier statistics are gathered for small detection volumes. Another advantage is that highly segmented sensors can be produced. Each sensor has many independent electrodes providing position resolution measurements.

3.2.1 Band Theory of Solids

The band-gap properties of a material have important consequences for a material's electrical properties. In the case of free atoms; the electrons exist in quantised states and possess discrete energies where each electron must have a unique set of quantum numbers. An electron has half-ineteger spin ($s = \pm 1/2$) meaning it is a fermion and thus obeys Fermi-Dirac statistics and the Pauli exclusion principle. It

is due to the exclusion principle, which says that two fermions cannot occupy the same quantum state, that electrons occupy specific orbitals of a host atom. When several atoms are brought together in a crystal lattice, the discrete levels cannot overlap and so they acquire energy levels that are similar but not the same. When a large number of atoms are confined within a crystal structure, the energy levels form a quasi-continuous band which can extend over several electron volts.

Most solid materials are grouped into three categories based on their electrical properties: conductors, semiconductors and insulators. The electrical properties of a material are determined by the configuration of the valence and conduction bands and the forbidden energy states (band-gap) that exist between them. The valence band is of lower energy than the conduction band. The valence band is populated by electrons that have an energy such that they are bound to their lattice site. The conduction band is populated by mobile electrons that are not fixed to their lattice site. Conduction electrons can freely travel through the lattice of the material.

A material is classified as a conductor if there is no energy gap between the valence and conduction bands. This enables many electrons to populate the conduction band hence resulting in high electron mobility. An insulator is characterised by a large band-gap (≥ 5 eV) which prevents valence electrons from populating the conduction band due to thermal excitations, thereby resulting in minimal conductivity. Silicon dioxide (SiO_2) is an example of an insulator material.

A semiconductor material usually has a band-gap of < 2 eV. The band-gap of a semiconductor is such that, at room temperature, a small number of valence electrons can be thermally excited across the band-gap and reach the conduction band. An excitation that promotes an electron from the valence band to the conduction band results in a mobile positive hole in the valence band and a mobile electron in the conduction band. The electron-hole pair are the charge carriers for the semiconductor detector. If the material is cooled then the energy available from thermal excitations is significantly smaller than the band-gap energy so that all electrons reside in the valence band and the material is non-conducting. Increasing the temperature results in a higher number of positive holes in the valence band and more mobile electrons in the conduction band.

A schematic of the band structure of a semiconductor is shown in Figure 3.2 where $N(E)$ is the density of allowed energy states. The Fermi-Dirac distribution $F(E)$ determines the probability that an electron will occupy a given energy state

E is given by

$$F(E) = \frac{1}{1 + e^{\frac{E - E_F}{kT}}} \ , \tag{3.1}$$

where E_F is the Fermi energy, k is the Boltzmann constant and T is the absolute temperature. The Fermi energy is the greatest energy that can be occupied by a fermion at 0 K. For a pure semiconductor material, the Fermi energy resides exactly halfway between the top of the valence band E_{V} and the bottom of the conduction band E_{C}. At 0 K the valence band for a semiconductor is fully occupied ($F(E) = 1$) and the conduction band is empty ($F(E) = 0$). With increasing temperature there is a greater probability that an electron will become thermally excited and overcome the energy gap thereby resulting in higher conductivity.

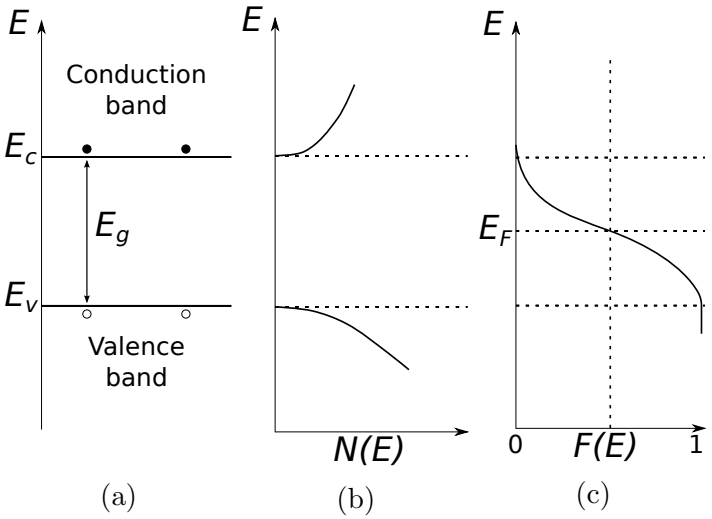


Figure 3.2: An intrinsic semiconductor. (a) Band diagram. (b) Density of allowed energy states. (c) Fermi distribution function.

Silicon is a group 4 element with atomic number 14. The crystal structure of silicon results in overlapping of the 3s and 3p subshells. This overlap gives rise to the formation of a lower band (valence band) and an upper band (conduction band), which are separated by a forbidden energy-gap. The energy difference between the valence band and conduction band is $E_g = 1.12$ eV for silicon at 300 K [38]. The magnitude of the band-gap is determined by the lattice periodicity, which leads to different band-gap energies for different semiconductor materials.

3.2.2 Charge Carrier Properties

The number of electron-hole pairs generated in a semiconductor depends on the energy deposited by the incident radiation E_i and the ionisation energy ε_{pair} of the material. Where ε_{pair} is the energy required to produce one electron-hole pair. For a semiconductor such as silicon, the top of the valence band and bottom of the conduction band are not aligned with respect to their momentum. A semiconductor with such a band configuration is known as an indirect band-gap semiconductor and requires a change in electron energy as well as a change in crystal momentum for an electron to be excited from the valence band to the conduction band. It is for this reason that $\varepsilon_{pair} > E_g$ for an indirect band-gap semiconductor like silicon. The majority of the deposited energy results in non-ionising excitations such as phonon excitation. The values of the ionisation energy and band-gap energy are shown in Table 3.1 for silicon for different temperatures. For silicon, the average electron-hole production energy $\varepsilon_{pair} \approx 3.6$ eV is roughly three times greater than the band-gap $E_g = 1.12$ eV.

Table 3.1: Band-gap and ionisation properties of silicon.

Type	ε_{pair} 300K	ε_{pair} 77K	E_{gap} 300K	E_{gap} 0K
Si	3.62	3.76	1.12	1.17

Ionising radiation impinging on a semiconductor will result in the production of charge carriers within a localised area of the detector. Within this volume, the liberated electrons will further excite and ionise other valence electrons via collisional losses within the material. This results in the creation of a charge cloud where the number of generated electron-hole pairs N_i is expressed as

$$N_i = \frac{E_i}{\varepsilon_{pair}} \ . \tag{3.2}$$

The ionisation of a silicon atom results in the formation of a mobile electron-hole pair at a lattice site, which will eventually recombine resulting in no mobile charge carriers. The thermal velocity of the charge carriers results in a rapid motion in random directions at room temperature. If an electric field ϵ is applied, the mobile charge carriers will move apart in a direction parallel to the direction of the electric field with a drift velocity. Such motion will prevent the occurrence of electron-hole recombination.

The drift velocity with which the charge carriers can be swept through the lattice due to an electric field is dependent upon the particle's mobility. Mobility is a property that represents how easily the motion of a charge carrier is influenced by an applied electric field. The mobility for holes μ_h and electrons μ_e varies for different materials. A charge carrier's mobility and drift velocity are related by

$$\nu_h = \mu_h \times \epsilon \ , \tag{3.3}$$

for holes in the valence band and

$$\nu_e = \mu_e \times \epsilon \ , \tag{3.4}$$

for electrons in the conduction band where ν_h and ν_e are the hole and electron drift velocities, respectively. The motion of holes occurs indirectly via the motion of several electrons from neighbouring lattice sites. A hole moves in a particular direction by several electrons reconfiguring with a net motion in the opposite direction. For this reason, the mobility for electrons is typically greater than that of holes. For silicon, the mobility of electrons is approximately three times greater than that of holes (for Si: $\mu_e = 1350$ and $\mu_h = 450$ cm^2/Vs for low electric field strengths [39]). The drift velocity of either charge carrier increases with increasing electric field strength. For an electric field strength of $\epsilon > 5 \times 10^4$ V/cm, the electron drift velocity in silicon reaches a maximum of about 10^7 cm/s [40]. The current signal from a semiconductor is strongly influenced by the charge carrier mobilities and the applied electric field. Most semiconductor detectors are operated with sufficiently strong electric fields so that the charge carrier velocity reaches the saturation velocity.

3.2.3 Semiconductor Doping

For an intrinsic (pure) semiconductor the number of electrons in the conduction band n is equal to the number of holes in the valence band p such that

$$n = p = n_i \ , \tag{3.5}$$

where n_i is the intrinsic carrier concentration ($n_i \approx 10^{10}$ cm^{-3} for silicon at 300 K [41]).

The band-gap properties and conductivity of a semiconductor can be altered by adding specific concentrations of impurity atoms to the crystal lattice structure.

Silicon is a group four element meaning each atom has four valence electrons. By adding either trivalent (p-type) or pentavalent (n-type) dopant atoms to the silicon crystal lattice, either an excess of holes or electrons can arise which alters the conductive behaviour of a material. The term extrinsic semiconductor refers to a doped semiconductor which results in some lattice sites being occupied by dopant atoms instead of silicon atoms.

Donor Doping

The addition of a pentavalent, group five element such as phosphorus, arsenic or antimony to a pure silicon crystal is called n-type (donor) doping. Donor doping contributes an extra electron to the crystal lattice. Donor atoms will replace some silicon atoms within the lattice and form a covalent bond with each of the four surrounding silicon atoms. An n-type dopant has an extra valence electron which is weakly bound to the dopant atom and can be more easily ionised at lower temperatures. Ionisation of this excess electron will give rise to a conduction electron with no corresponding hole appearing within the valence band. In n-type semiconductors the electrons are majority carriers and holes are minority carriers. Donor impurities give rise to electrons with discrete energy levels situated just below the conduction band (within the forbidden band-gap). These electrons can be easily excited into the conduction band at low temperatures (see Figure 3.3a). When all donor impurities are ionised, the concentration of electrons in the conduction band n is approximately equal to the concentration of donor impurities N_D such that

$$n \approx N_D \ , \tag{3.6}$$

and

$$n \gg p \ . \tag{3.7}$$

The typical concentration of dopant impurities is on the order of 10^{13} atoms/cm^3. The addition of donor impurities increases the concentration of conduction electrons thereby shifting the Fermi level closer to the conduction band for an n-type material.

Acceptor Doping

Adding a trivalent (group three) element such as gallium, boron or indium to a semiconductor material is called p-type (acceptor) doping. An acceptor atom will occupy a lattice site and form three complete covalent bonds with the surround-

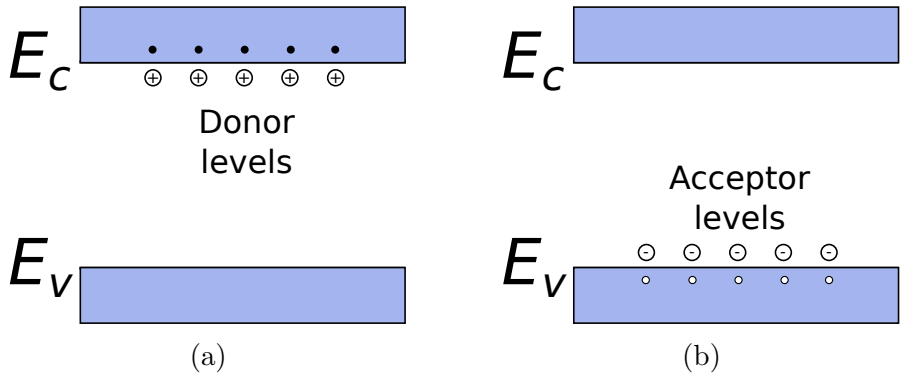


Figure 3.3: A schematic of the energy bands for doped semiconductors for (a) n-type doping and (b) p-type doping where the dopant atoms are ionised. The terms E_C and E_V represent the energy level of the bottom of the conduction band and top of the valence band respectively. Excitations result in ionisation of dopant atoms, yielding mobile electrons in the conduction band (n-type) and mobile holes in the valence band (p-type).

ing silicon atoms but the fourth covalent bond possesses just one electron and is incomplete. The absence of an electron results in a hole at the acceptor impurity lattice site. This is similar to when an electron is excited from the valence band to the conduction band in an intrinsic semiconductor. The vacancy can be filled by an electron from a neighbouring atom which results in the hole moving within the lattice. Consequently, the addition of acceptor impurities introduces acceptor sites which acquire an energy level that is slightly above the valence band in the forbidden band-gap (see Figure 3.3b). At low temperatures the acceptor levels are fully occupied as electrons are thermally excited from the valence band to the acceptor levels. The thermally excited electrons leave behind holes in the valence band that act as mobile charge carriers. In p-type semiconductors holes in the valence band are the majority carriers. If the concentration of acceptor impurities N_A is large compared to the intrinsic carrier concentration, then the number of holes in an extrinsic semiconductor is dominated by the concentration of acceptors. The concentration of holes in the valence band of a p-type material is given by

$$p \approx N_A \ , \tag{3.8}$$

and

$$p \gg n \ . \tag{3.9}$$

Adding acceptor impurities to a semiconductor will reduce the energy of Fermi level towards the valence band for a p-type material

3.3 The P-N Junction

An abrupt interface occurs within a crystal material where a donor doped region meets an acceptor doped region; this configuration is known as a p-n junction and forms the basis of all semiconductor radiation detectors. When considered as separate bodies, the p and n-type regions are electrically neutral. The n-type region contains excess electrons with immobile donor lattice sites whereas the p-type region contains an excess of mobile holes and fixed acceptor lattice sites.

3.3.1 Built-In Potential

Where two doped regions meet; the concentration of conduction electrons in the n-type region and holes in the p-type region results in a sharp concentration gradient leading to diffusion occuring across the junction. The diffusion and subsequent recombination of holes and electrons forms a region at the junction which is depleted of mobile charge carriers. Within the depleted region, only the fixed charges of the dopant ions remain resulting in negative acceptor ions on the p-side and positive donor ions on the n-side. The net positive space charge in the n-type and net negative space charge in the p-type forms an electric field which prevents futher diffusion as shown in Figure 3.4. Thermal equilibrium is achieved when the potential difference, due to the space charge, balances the diffusion current and the resultant net current flow through the junction is zero. The potential between the n-type and p-type regions at thermal equilibrium is known as the built in potential V_{bi} where

$$V_{bi} = \frac{kT}{e} \ln\left(\frac{N_A N_D}{n_i^2}\right) . \tag{3.10}$$

The symbols N_A and N_D represent the acceptor and donor dopant concentrations where n_i is the intrinsic carrier concentration. For a p-n junction in thermal equilibrium the valence and conduction bands are offset due to the built in potential. However, the Fermi level remains constant over the entire device.

The region devoid of mobile charge carriers extends from the junction into both the n-type and p-type regions and is called the depletion region. Depending on the donor concentration N_D and the acceptor concentration N_A the extent to which the

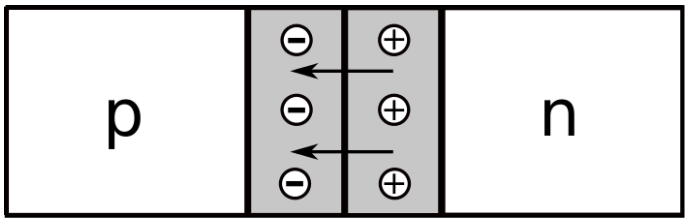


Figure 3.4: A schematic representation of a p-n junction showing the space charge formation near the junction preventing further diffusion of charge carriers. The shaded region represents the depletion region. The arrows indicate the electric field direction and the circled charges are the fixed dopant ions.

depletion region extends into the n or p-side of the junction can be controlled. The electric field is a maximum at the junction and extends into the depletion region on both sides of the junction. The electric field will cause any electrons generated within the depletion region, due to incident radiation or thermal excitation, to be swept towards the n-type region. Similarly, holes generated within this region are transported towards the p-type region. This controlled motion of charged particles within a region of high resistivity bounded by electrodes is attractive for radiation detection purposes.

3.3.2 P-N Junction Biasing

The volume of the depletion region is of great importance as it represents the total charge sensitive region of the detector. The size of the depletion region formed by thermal diffusion alone is rather small (typically order of μm) and located in the vicinity of the junction. By applying a potential across a p-n junction, the properties of the depletion region can be significantly altered. Forward biasing of the junction occurs when a positive voltage is applied to the p-side and a negative voltage is applied to the n-side. This reduces the size of the depletion region meaning conduction electrons will be attracted across the junction from the n-side to the p-side. Holes will also be attracted from the p-side to the n-side, resulting in a low resistance across the junction.

Reverse biasing of the junction is when a positive potential is applied to the n-side and a negative potential is applied to the p-side. This increases the potential difference across the junction and will cause the conduction electrons on the n-side and holes on the p-side to be attracted away from the junction. The depletion region will expand outwards from the junction as shown in Figure 3.5. Reverse biasing results in the minority carriers (holes in the n-side and conduction electrons

in the p-side) being attracted across the junction. The low concentrations of the minority carriers produce only a small current. Reverse biasing of a p-n junction can establish a large region devoid of mobile charge carriers with a large electric field capable of quickly and efficiently transporting electrons and holes towards nearby electrodes.

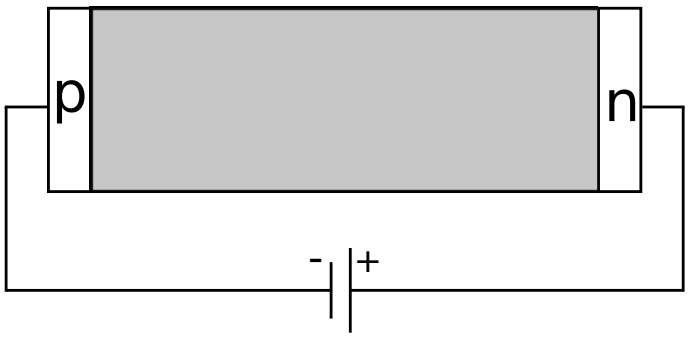


Figure 3.5: A schematic representation of a reverse biased p-n junction. The shaded region represents the depletion region.

3.3.3 Silicon Detectors

Semiconductor detector p-n junctions are usually constructed using a heavily doped region and a lightly doped region ($N_D \gg N_A$ or $N_A \gg N_D$) to form a one sided abrupt junction. An example of an abrupt junction may be a lightly doped n-type region in contact with a heavily doped p+ region. The heavier doping concentration of the p+ means there are a greater number of holes diffusing across the junction that will travel further into the n-type bulk before recombining with electrons and so the depletion region extends into the lightly doped region whilst barely extending into the highly doped layer. This allows the heavily doped layer to be made very thin, which is ideal for detecting weakly penetrating radiation.

An example of a silicon detector using a one sided abrupt p-n junction is depicted in Figure 3.6. The junction is formed between the heavily doped p+ contact and the lightly doped n-type bulk. The depletion region grows from the p+ contact (junction side) towards the n+ contact (ohmic side) by applying a relative positive potential to the n+ electrode or a negative potential to the p+ electrode. Such a detector is typically operated with a reverse bias voltage such that the depletion region extends over the entire bulk region. Reverse biasing therefore results in a large depleted volume enclosed by the p+ and n+ electrodes. The bulk region thus

forms the depleted sensitive volume within which charge carriers are generated and transported to the electrodes due to the applied electric field.

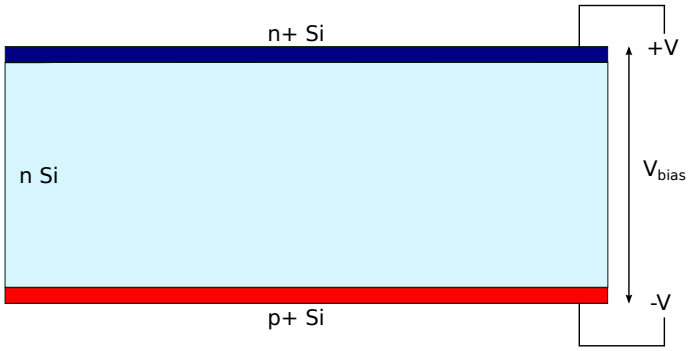


Figure 3.6: Schematic of a reverse biased p-n junction used as a detector. The junction grows from the p+ side for an n-type bulk.

The width of the depletion region for the case depicted in Figure 3.6 is given by

$$d = \sqrt{\frac{2\varepsilon_{Si}(V_{bias} + V_{bi})}{eN}} \tag{3.11}$$

where ε_{Si} is the dielectric constant of silicon ($\varepsilon_{Si} = \varepsilon_r\varepsilon_0$), V_{bias} is the potential difference across the junction, e is the electron charge and N represents the dopant concentration of the more lightly doped region. The symbol ε_r denotes the relative permittivity and ε_0 is the vacuum permittivity. The value of V_{bias} in equation 3.11 is positive for reverse bias and negative for forward bias.

Full Depletion

The full depletion voltage V_{FD} is the minimum voltage which results in the depletion region, and electric field, extending over the entire bulk thickness w. Taking the relationship given in equation 3.11 and setting the depletion region thickness d equal to the bulk thickness w and assuming that $V_{bias} \gg V_{bi}$. The value for the full depletion voltage is given by

$$V_{FD} = \frac{eNw^2}{2\varepsilon_{Si}}. \tag{3.12}$$

Therefore, the width of the depletion region is dependent upon the bulk dopant concentration, bulk thickness and is proportional to $\sqrt{V_{bias}}$.

Increasing the width of the depletion region and thus the separation of the electrodes, results in decreasing the detector capacitance. When the bulk region is not

fully depleted $V_{bias} \leq V_{FD}$, the bulk capacitance is

$$C_{bulk} = \frac{\varepsilon_{Si} A}{d} = A\left(\frac{eN\varepsilon_{Si}}{2(V_{bias} + V_{bi})}\right)^{1/2} . \tag{3.13}$$

When fully depleted $V_{bias} > V_{FD}$, the full depletion capacitance is

$$C_{bulk} = \frac{\varepsilon_{Si} A}{w} \tag{3.14}$$

where A is the area of the electrode that spans the depletion region. The capacitance is therefore smaller for thicker detectors. The relationship between applied bias voltage and detector capacitance can be useful for measuring the full depletion voltage by studying the CV relationship of real detectors.

As the charge carrier drift velocity depends on the applied electric field within the depletion region, detectors are usually over depleted to achieve large electric fields and fast drift velocities. The maximum electric field arises at the junction and its magnitude for $V_{bias} \leq V_{FD}$ is given by

$$\epsilon_{max} \approx \frac{2V_{bias}}{d} = \left(\frac{2eNV_{bias}}{\varepsilon_{Si}}\right)^{1/2} . \tag{3.15}$$

The maximum value of the electric field increases with bias voltage as $\sqrt{V_{bias}}$, which can typically reach values of up to $10^6 - 10^7$ V/m for a fully depleted detector. The electric field within the bulk has a linear dependency on position within the bulk and is related to the maximum electric field according to

$$\epsilon(x) = \epsilon_{max}\left(1 - \frac{x}{d}\right) \tag{3.16}$$

where x is the distance from the junction and d is the depletion region width. Increasing the bias voltage beyond the full depletion voltage will increase the maximum electric field and result in a more uniform field profile.

3.4 Signal Formation

Electron-hole pairs within the detector bulk drift due to the electric field and are collected by their respective electrodes. Electrons are collected at the n+ electrode and holes at the p+ electrode. The motion of the charge carriers induces an almost instantaneous signal in the collecting electrode which can be measured as a current

in an external circuit. Signal formation is dependent on the electric field and charge carrier velocity within the depleted region.

3.4.1 Shockley-Ramo Theorem

The Shockley-Ramo theorem [42] [43] explains signal formation within a detector due to charge carrier motion. The theorem states that the current i induced on a collecting electrode due to a charge q with instantaneous velocity $\vec{v}$ can be expressed as

$$i = q\vec{E_w}.\vec{v} \ , \tag{3.17}$$

where $\vec{E_w}$ is the weighting field. The weighting field is dependent on the instantaneous position of a charge relative to the position of the readout electrode. The weighting field determines how charge motion couples to the readout electrode and depends on the geometry. The operating electric field within the depletion region that causes the drift is not the same as the weighting field. The total charge Q_s induced on an electrode is obtained by integrating equation 3.17 over a time interval such that

$$Q_s = \int_{t_i}^{t_f} i dt \ , \tag{3.18}$$

where the difference between t_i and t_f is the charge collection time.

3.4.2 Charge Collection

The total signal charge Q_s generated due to an energy E deposited in the detector is given by

$$Q_s = \frac{E}{\varepsilon_{pair}} e \ , \tag{3.19}$$

where e is the charge of an electron and ε_{pair} is the ionisation energy of the semiconductor. The initial energy deposited E can be related to the current pulse $i_s(t)$ induced in an electrode via the following expression

$$E \propto Q_s = \int i_s(t) dt \ . \tag{3.20}$$

Upon collection, the induced charge signal is amplified and converted to an output voltage signal courtesy of a charge sensitive preamplifier. The quantity of moving charge q generated within the bulk medium is proportional to the total energy deposited in the bulk and thus the energy loss of the radiation can be determined

via analysis of the output pulse from the preamplifier.

The charge collection time is the time required for a charge carrier to reach a collecting electrode and is thus dependent on sensor thickness, bias voltage and carrier mobility μ. The difference in electron and hole mobility yields a charge collection time that is three times faster for electrons than holes in silicon. For a silicon sensor of thickness 300 μm that is overdepleted, a typical charge collection time on the order 10 ns and 30 ns [39] can be expected for electrons and holes, respectively. Decreasing the value of the bias voltage will result in a smaller electric field and longer charge collection times.

3.5 Strip Detectors

Silicon strip detectors are widely used because of the high position resolution measurements that are possible by constructing detectors with finely spaced electrodes. Segmentation of the electrodes into strips enables signals induced in each electrode to be independently processed. This improves rate capability and also reduces electronic noise. The maximum strip length for a sensor is limited by the sensor capacitance and the event rate. Long strips have a larger capacitance and therefore more noise. A longer strip will have a larger solid angle and subsequently will receive a high event rate. Therefore it is advantageous to use shorter strips with a smaller solid angle and less noise allowing signal processing techniques with smaller dead times.

A single-sided strip sensor is constructed by segmenting the electrode on just one side to form individual strips of highly doped implants (p+ or n+ electrodes). An example of a single-sided strip detector with n-type bulk and p+ strips is shown in Figure 3.7. The aluminium strips at the surface allow an electrical connection to the implant strips. The aluminium contact strip is DC connected to the implant strip. The silicon dioxide (SiO_2) insulation layer seals the assembly and provides passivation and protection of the silicon whilst offering the possibility of an AC coupling capacitance. The detector is depleted by applying a positive bias to the n+ aluminium backside whilst keeping the p+ strips grounded. This results in a depletion region which expands, with increasing bias voltage, from each p+ implant towards the n+ backplane.

Transverse diffusion within the bulk, which occurs due to effects such as thermal diffusion, spreads the charge cloud over multiple strip electrodes. Segmentation of the electrodes results in multiple strips collecting charges from a single ionising par-

ticle track (assuming particle trajectory is not perpendicular to sensor) and hence provide position resolution in the direction perpendicular to the strip length. Evaluating the ratio of charge collected at each electrode allows a position resolution to be obtained, which is less than the electrode pitch [39].

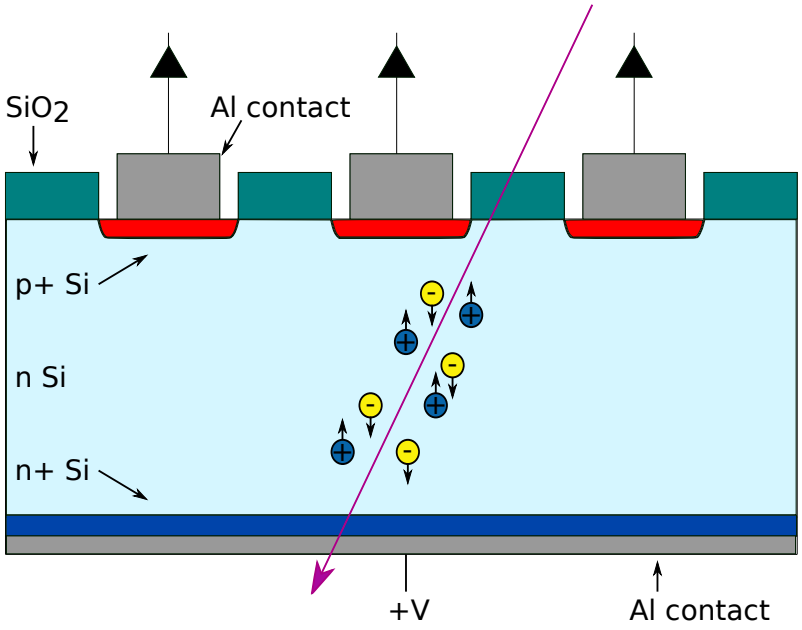


Figure 3.7: A possible strip detector geometry with DC coupled p+ implants in n-type bulk silicon.

3.5.1 Double-Sided Detectors

Double-sided silicon strip detectors (DSSSD) are formed by segmenting the n+ and p+ contacts on both sides of the bulk. The strips on opposite sides can be oriented such that they are angled with respect to each other to provide two-dimensional position resolution. Strips on opposite sides are often angled orthogonally but are sometimes positioned with an angle less than 90 degrees. A DSSSD allows both types of charge carriers to be collected at segmented electrodes where a two-dimensional position measurement is determined by the area where two strips on opposite sides intersect (see section 4.1.1 for strip angle explanation). The spatial resolution is subsequently determined by the electrode segmentation. Electron-hole pairs generated within the bulk due to passing radiation will propagate towards their respective electrodes. This results in an electrical current in a collecting electrode, which is dependent on the position of the incident particle relative to the electrode.

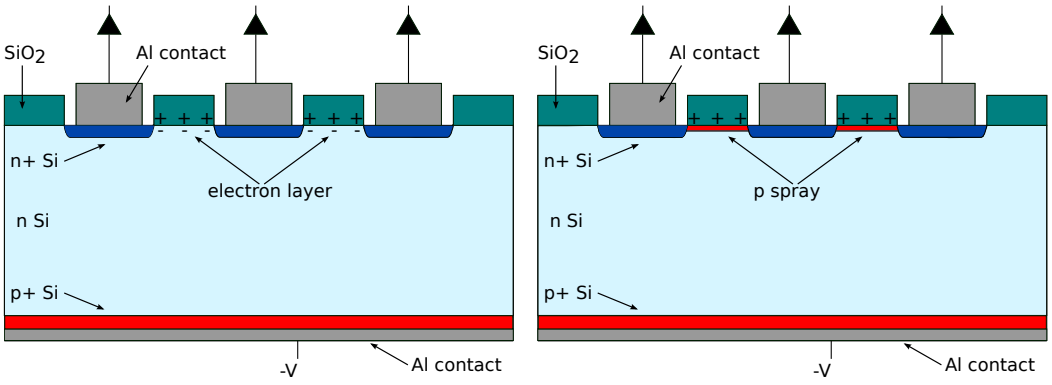
An abrupt junction is formed where the n-type bulk meets a p+ strip implant. A double-sided detector is reverse biased by applying a positive (negative) potential to every n+ (p+) strip whilst grounding the p+ (n+) strips. Reverse biasing of the detector results in the depletion region growing from each of the junction implants towards the ohmic side. A double-sided detector must always be over-depleted ($V_{bias} > V_{FD}$) to ensure that the electric field is sufficient to ensure collection of holes from the whole bulk volume.

3.5.2 Implant Isolation

Unlike for the case of p+ strips in n-type bulk material, special care must be taken when segmenting n+ strips in n-type bulk to maintain isolation between the neighbouring strips. Total ionising dose effects can result in adjacent strips becoming electrically connected on the side of the detector where electrons are collected. Incident radiation will produce ionisation of the silicon bulk material as well as ionisation of the silicon dioxide layer. For silicon, the mobility of holes is approximately three times less than that for electrons, but for SiO_2 the mobility of holes is significantly smaller [44] than that of the electrons due to the irregular structure. Consequently, the electrons leave the oxide within a time scale of the order of a picosecond [45]. Prior to escaping the oxide, some electron hole pairs will undergo recombination. Holes which do not recombine will remain relatively immobile within the oxide layer. Over time the holes will migrate towards the SiO_2-Si interface where the highly irregular structure can result in some holes becoming permanently trapped. The presence of a large number of holes at the oxide-silicon interface alters the electric field within the silicon bulk close to the interface. This accumulation of positive charge ultimately induces an electron accumulation layer in the n-type bulk silicon. The electron accumulation layer electrically connects adjacent n+ strips thereby decreasing the inter-strip resistance.

Figure 3.8 shows a detector with n+ strips in an n-type bulk. The left side (Figure 3.8a) diplays an electron accumulation layer within the bulk, which shorts neighbouring n+ strips. The right side (Figure 3.8b) displays a technique, known as p-spray, whereby neighbouring strips are electrically isolated. Introducing a p-type region between the n+ strips results in a lateral p-n junction that disrupts the electron accumulation layer and isolates the n+ strips. The p-spray technique uses a thin layer of medium doped p-type silicon which extends across the entire region between adjacent strips. An alternative technique to p-spray that is used for

isolation is p-stop [46]. A p-stop uses a highly doped p+ implant positioned between adjacent n+ strips to achieve strip isolation. For double-sided sensors with small strip separations, the p-stop technique is not a possibility for strip isolation due to limited available space between neighbouring strips. The p-stop technique requires the fabrication of twice as many implants (one p-stop for every n+ implant) on one side of the sensor, which makes this a more costly and less attractive option when using sensors with a very large number of strips.



(a) No isolation. (b) P-spray isolation.

Figure 3.8: Isolation of n+ strips in n-type bulk.

3.5.3 Strip Capacitance

For a strip detector, the two main contributions to the total strip capacitance are due to interstrip capacitance C_s and the backplane (bulk) capacitance C_b. The interstrip capacitance arises due to neighbouring strips and the backplane capacitance is the capacitance between a strip on the junction side and the ohmic side, or vice versa. The backplane capacitance is dependent on the bulk thickness. The majority of the total capacitance is usually due to the capacitance between neighbouring strips. The interstrip capacitance is dependent on the strip pitch p and the strip dimensions such as length l and width w. Strip pitch is defined as the distance from the centre of one strip to the centre of the neighbouring strip. The pitch is referred to when discussing electrical segmentation and not the strip width. The interstrip capacitance per unit length in units of pF/cm is given by

$$\frac{C_s}{l} = 0.03 + 1.62\frac{w + 20\ \mu\text{m}}{p}\ , \tag{3.21}$$

[47] which is typically about 1-2 pF/cm for strip pitches of 25 - 100 μm [39]. The backplane capacitance C_b for a strip can be obtained from equation 3.14 and is given by

$$\frac{C_b}{l} \approx \varepsilon_r \varepsilon_0 \frac{p}{d} \ . \tag{3.22}$$

The symbol d is the detector thickness, ε_r is the relative permittivity and the strip is represented as an electrode with a width equal to the strip pitch (fringing field is limited to centreline between two strips). The interstrip and backplane capacitance values have been calculated for silicon ($\varepsilon_r = 11.7$) for different values of strip pitch, width and detector thickness and the results are plotted in Figure 3.9. For a given pitch, the interstrip capacitance is greatest for larger strip widths. The interstrip capacitance is largest for strips with a small pitch. The backplane capacitance increases as a detector becomes thinner and larger strip pitches also result in greater backplane capacitance.

For a silicon strip detector with a strip pitch of $p = 50$ μm, a strip width of $w = 38$ μm and a detector thickness of $d = 300$ μm, the interstrip capacitance is

$$\frac{C_s}{l} = 0.03 + 1.62\frac{38 + 20}{50} = 1.91 \text{ pF/cm} \tag{3.23}$$

and the backplane capacitance is

$$\frac{C_b}{l} = 11.7 \times \varepsilon_0 \times \frac{50}{300} = 0.17 \text{ pF/cm} \ . \tag{3.24}$$

For such a configuration, the backplane capacitance accounts for approximately 8% of the total strip capacitance C_{strip} and for a 10 cm strip length the total capacitance is given by

$$C_{strip} \approx (1.91 + 0.17) \times 10 = 21 \text{ pF}. \tag{3.25}$$

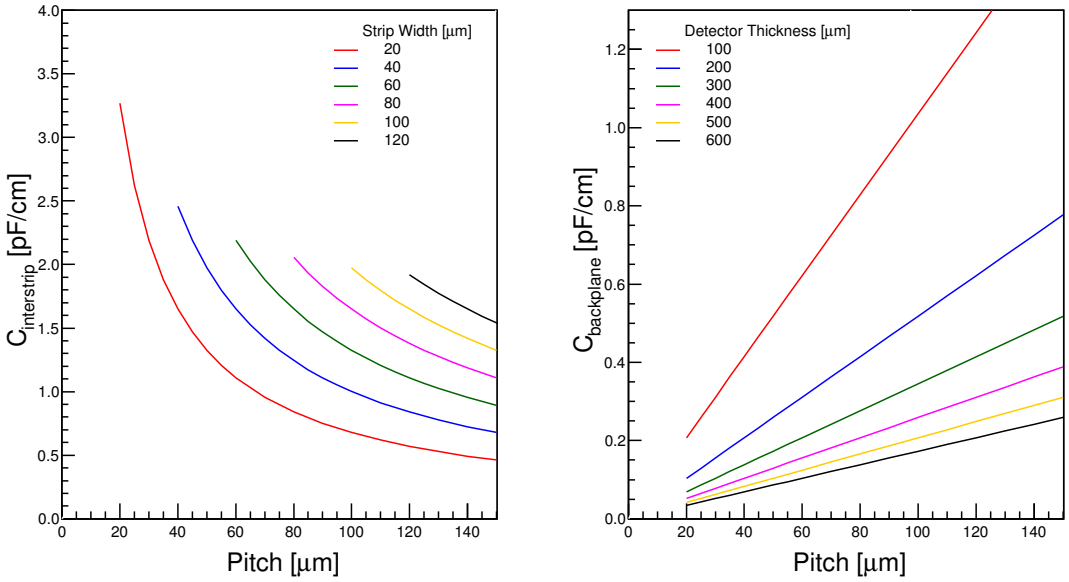


Figure 3.9: The values for the interstrip and backplane capacitance are calculated for different silicon strip detector geometries.

Chapter 4

Silicon Sensors and Detector Construction

The properties of each of the four sensor types are outlined along with the resulatant detectors, which are produced by combining several sensors. The stereo-angle strip geometry and its benefits are explained. The different stages of the quality assurance process, used to identify defective sensors, is covered in detail. The data for all non-defective sensors, used for detector construction, are shown. The quality assurance data is presented and explained using the semiconductor principles outlined in Chapter 3. A short summary of the process used to construct a complete detector is given as well as the test data of each completed detector.

4.1 Sensor Design

The tracker is constructed using just two types of detectors. One type of detector is used to construct the inner layer and another type of detector is used for both outer layers. Figure 4.1 shows the dimensions of the different detectors and the silicon sensors used for the construction. There are four different double-sided silicon sensors referred to as A,B,C and D that are used for the construction. The properties of each sensor type are outlined in Table 4.1, according the manufacturer's (Micron Semiconductor Ltd) specifications. All sensors have been produced from silicon ingots using the float zone (FZ) crystal growth technique. The inner layer detectors, which have the smallest area, are constructed by bonding together the strips of two individual B and D sensors. One complete outer detector is built by wire bonding together three sensors (A,B and C). The C sensor has the largest area with a total

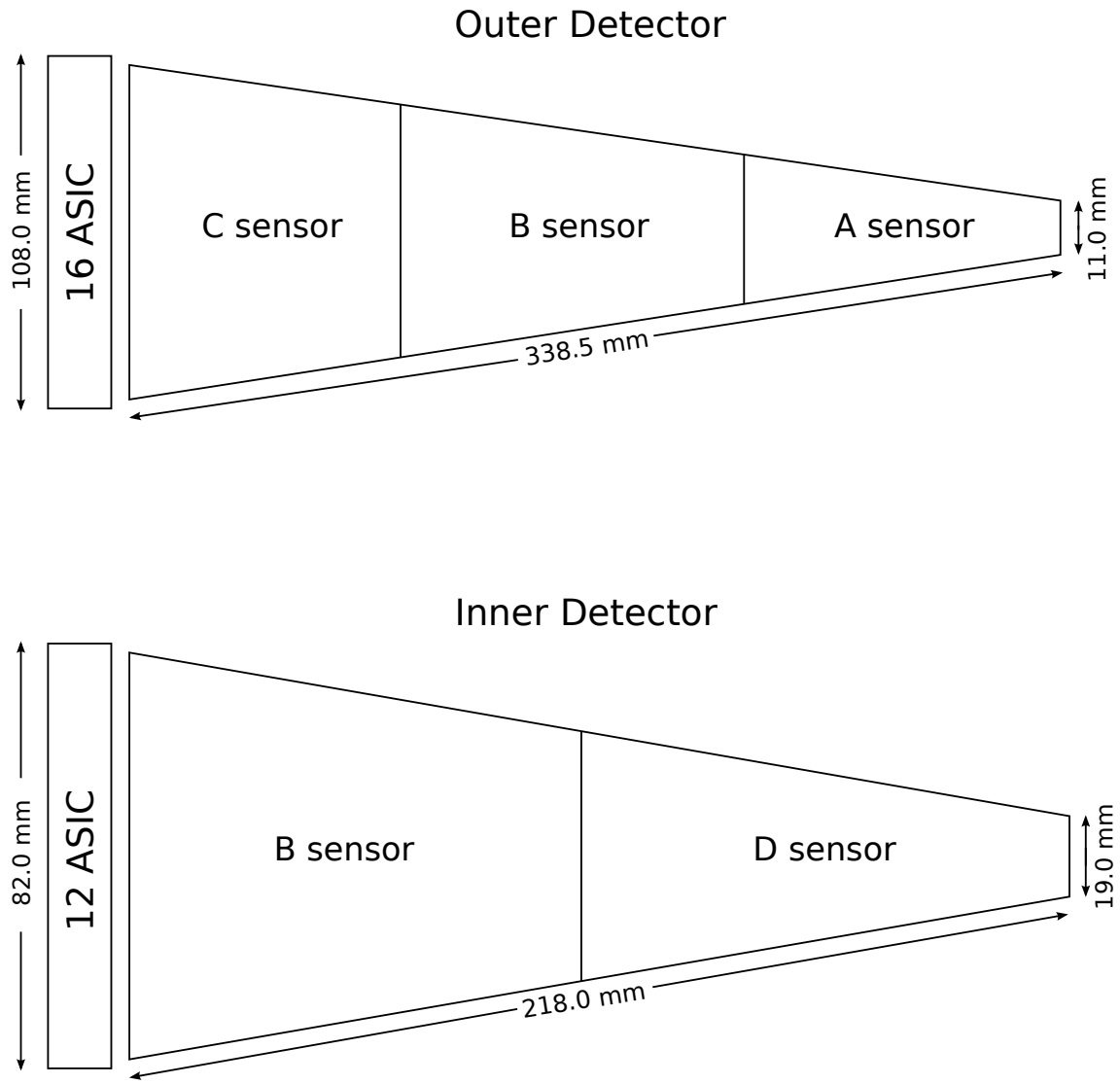


Figure 4.1: A schematic of the inner and outer detectors showing their dimensions and the sensors used for the construction.

of 2048 strips on each side, and the D sensor has the smallest area with 876 strips on each side. The B sensor is used to construct both the inner and outer detectors. A photograph of all four sensor types is shown in Figure 4.2.

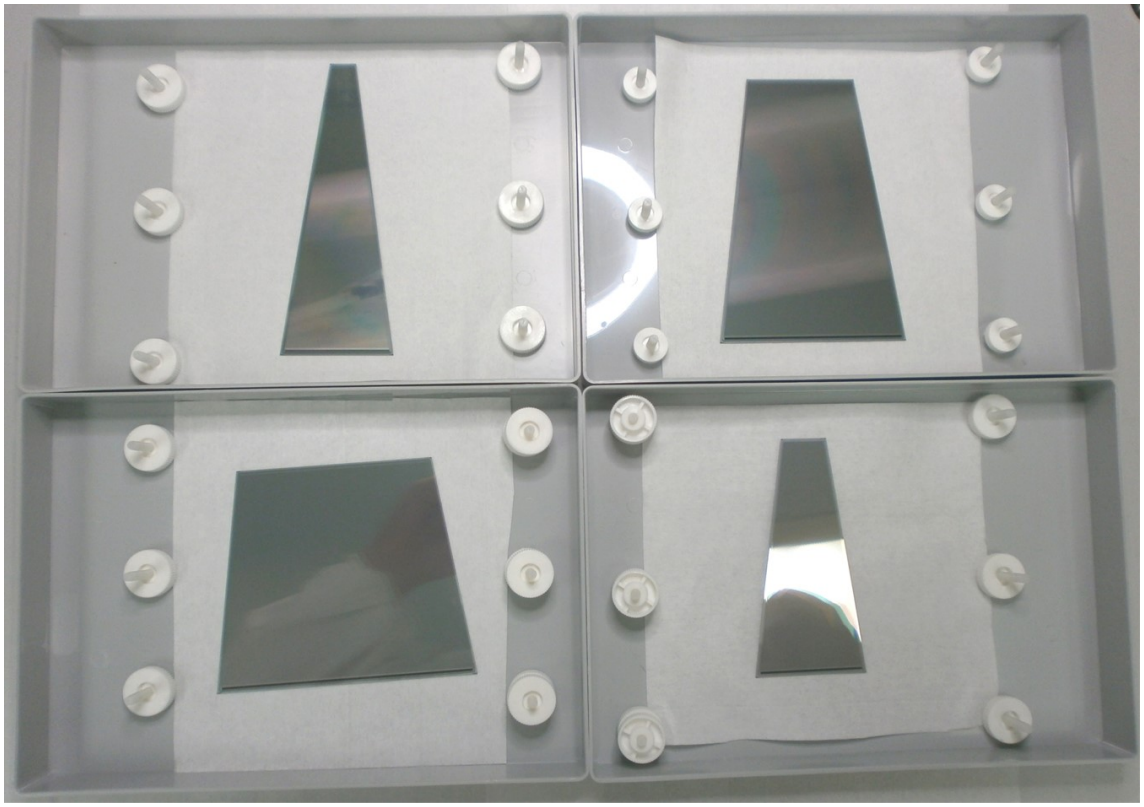


Figure 4.2: A photograph of all sensors used for the construction. A sensor is top left, B sensor is top right, C sensor is bottom left and D sensor is bottom right.

Table 4.1: Summary of the properties of each sensor type.

Sensor	A	B	C	D
Strips [per side]	889	1536	2048	876
Thickness [μm]	300	300	300	300
Active Area [cm^2]	31	48	49	24
Bias Resistor [MΩ]	25-300	25-300	25-300	25-300
Full Depletion [V]	53	53	53	53
Max Total Current [μA]	1.1	2.2	2.5	1.0
Max Strip Current [nA]	2.0	1.9	1.4	1.9
Operating Voltage [V]	80	80	80	80
Max Rise Time [ns]	100	100	100	100

4.1.1 Strip Geometry

All sensors are a trapezoid shape with an electrical segmentation determined by a strip pitch of 50.5 ± 1.0 μm and a sensor thickness of 300 ± 30 μm. The sensors are all n-type bulk material with heavily doped p+ strips on one side and heavily doped n+ strips on the opposite side. The junction electrodes are formed by the strips on the p-side. All strips, on both sides, have the same width and separation. The average strip width and strip separation is 38 μm and 12 μm, respectively. Isolation of strips on the n-side is achieved by applying a thin p-spray to the region between adjacent n+ strips (see section 3.5). The small strip separation necessitated the need for p-spray instead of using p-stop technology. For all sensors, every strip has an aluminium contact that is DC connected to the doped implant. Each strip is equipped with a test pad and bond pad which provides a DC connection to the strip implant and are also connected to the bias rail via a polysilicon resistor shown in Figure 4.3. The bias resistors are included to aid the silicon sensor quality assurance process by conveniently allowing strip biasing via the bias rail. For the final detector configuration, each strip is biased via the DC bond pad which is connected to the front-end electronics. The bias rail completely surrounds the sensor and is itself surrounded by a further nine guard rings which surround the sensor's implanted strips and prevent its operation from being dominated by edge effects. The guard rings are biased via punch through from the bias rail and thus collect currents from the sensor edge and form a stable boundary. The spacing of the guard rings gradually increases to produce a uniform potential drop so that the outermost ring is at the same potential on both the biased and unbiased side of the sensor.

The strips run parallel to the edge of the sensor resulting in variable strip length due to the sensor's trapezoid shape. Some of the strips run the full length of the sensor whereas some strips are much shorter as they terminate at the sensor edge as shown in the drawing in Figure 4.4. The A and D sensors are situated furthest from the readout electronics and thus signify the end of the chain of sensors. The B and C sensors are furnished with additional bond pads at the strip end which is not connected to the bias resistor in order to facilitate the grouping of multiple sensors. Figure 4.5 shows a microscope picture of the end of the strips furthest from the bias resistors for an A and B sensor where the bond pads and variable strip length can be seen.

On the reverse side of the sensor, the geometry is the same except that the strips now run parallel to the opposite edge of the sensor. This means that the bond pad

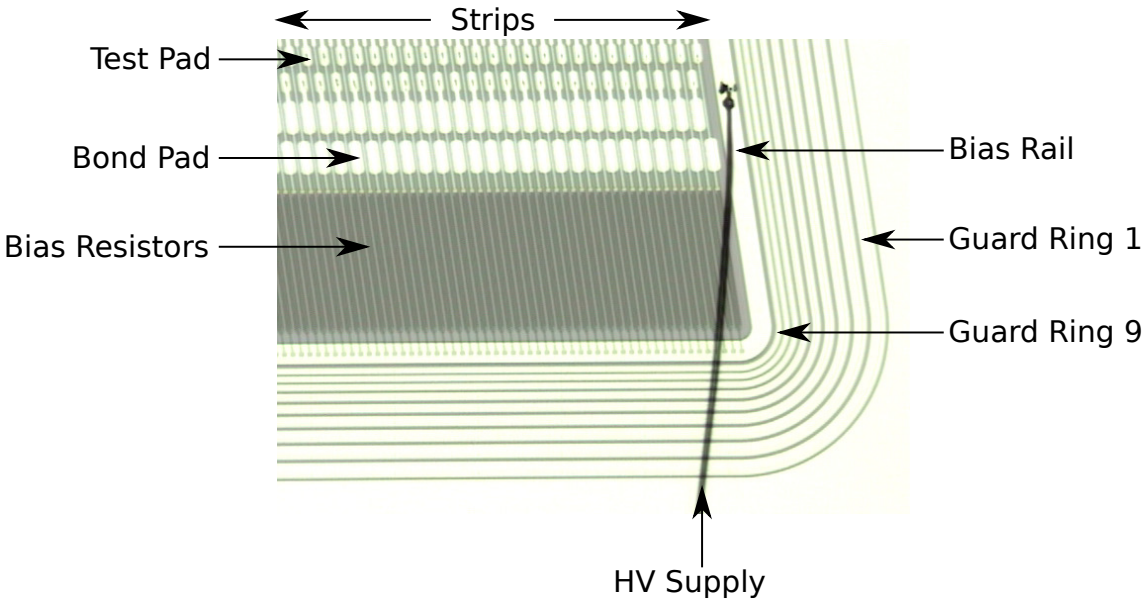


Figure 4.3: The test pads and bond pads provide a DC connection to the strip implant and are connected to the bias rail via a polysilicon resistor.

for the shortest strip of the p-side is directly opposite the bond pad of the longest strip of the n-side and vice versa. This strip geometry was selected as it allows sensors without double metallisation and the front-end electronics can be situated at just one end of the sensor, upstream from the target region. Another advantage of the strip layout is that it can reduce the probability of mismatching hits on the two opposing sensor faces.

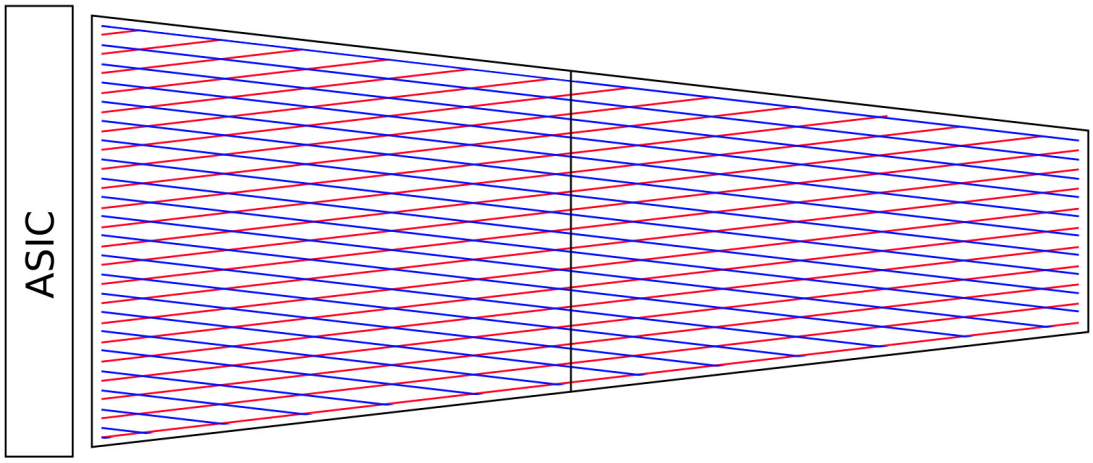


Figure 4.4: A schematic of the strip geometry of the R^3B silicon sensors. Red lines indicate strips on the p-side and blue lines are strips on the n-side (or vice versa).

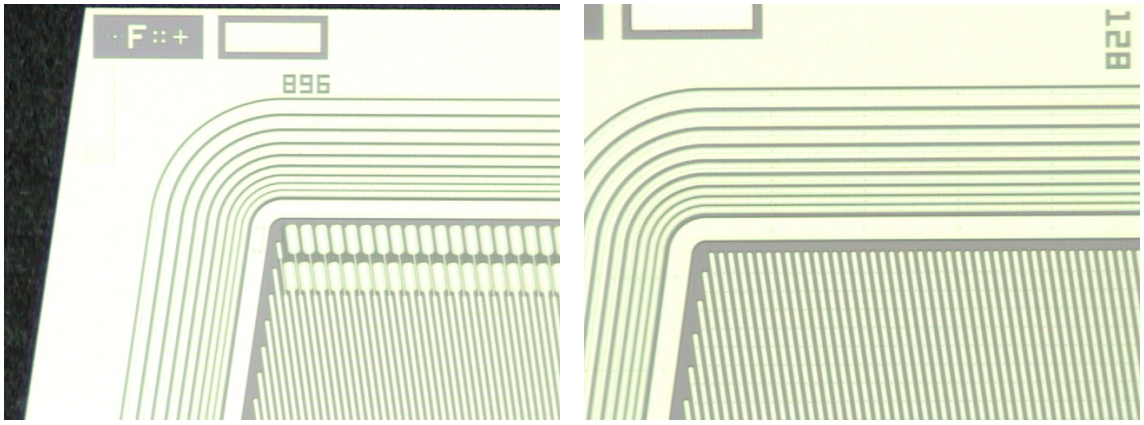
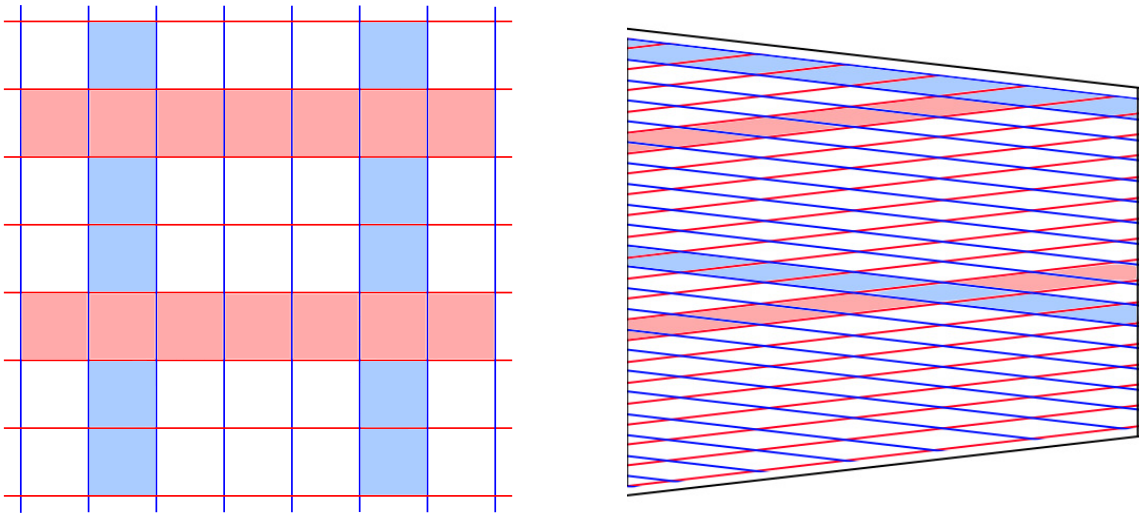


Figure 4.5: A microscope picture of an A (left) and B (right) sensor. The B sensor has bond pads at either end of the strip to enable multi-sensor detector construction. The A sensor is positioned furthest from the readout and only needs bond pads at one strip end. The corners of each sensor are marked with fiducials represented by the + symbol.

Stereo-Angle Strip Geometry

In some cases, such as high rate experiments, it is advantageous to have the strips on opposite faces of the sensor at an angle much less than 90°. This angle is referred to as the stereo-angle α. Consider the case of orthogonal strips where a single strip on one side crosses all the strips on the other side of the sensor. A single strip records one hit and therefore gives an x-coordinate in the direction perpendicular to strip length but no y-coordinate in the direction parallel to the strip length. In order to retrieve the y position it is necessary to examine all hits in all strips on the opposite electrode face. For a system with orthogonal strips; a hit in a given strip can result in a hit in any of the strips on the reverse side, therefore for an example where two protons hit the detector there will be two strips on the top and two on the bottom which are hit and a total of four places where the strips overlap as shown in Figure 4.6a. Therefore there are two real combinations and two ghost combinations. The area covered by two orthogonal strips of length l_1 and l_2 is given by $A = l_1 l_2$. If the strips on the opposing sides are instead orientated at an acute angle (Figure 4.6b), a strip on one side will not cross all of the strips on the other side. Subsequently the area within which hits can be mismatched is reduced and the number of ghost combinations is limited by using strips with a stere-oangle [39].

The stereo-angle of the strips for all four wafers is always 16.23°. Figure 4.7 displays the stereo-angle, strip pitch and the resultant dimensions formed where two strips on opposite sides overlap. The intersection of two strips is approximately



(a) Orthogonal strips.

(b) Non-orthogonal strips.

Figure 4.6: A typical orthogonal strip arrangement, shown in (a), means a strip on one side of the sensor overlaps all strips on the opposite side of the sensor. Using a stereo strip geometry, shown in (b), means that not all strips on one side overlap a single strip on the other side of the detector. The number of ghost hits is reduced by using a stero strip geometry. Red shaded regions represent a hit in a p-strip and blue regions are a hit in an n-strip.

354 μm in length and 51 μm in width. Decreasing the value of the stereo-angle would have two main consequences, firstly there would be a reduced probability of mismatching hits as the possible combinations of strip hits decreases, secondly the strips on opposite faces would become more aligned and the position resolution in the direction parallel to the strip length worsens.

Strip Length

Whereas the strip pitch and stereo-angle have implications for the position resolution, the length of the sensor has been selected in order to increase the detector's angular coverage and improve detector efficiency. Higher energy protons are more forward focussed therefore increasing the length to which the sensor extends beyond the target region will significantly improve experimental efficiencies. Each sensor is constructed from an initial wafer with a six-inch diameter. The desired strip length of the detector must thereby be achieved by ganging together multiple sensors [39]. When deciding upon the maximum strip length, the sensor capacitance and the event rate must be taken into consideration. A longer strip will have a larger capacitance which will result in more noise. Increasing the length of a strip will also

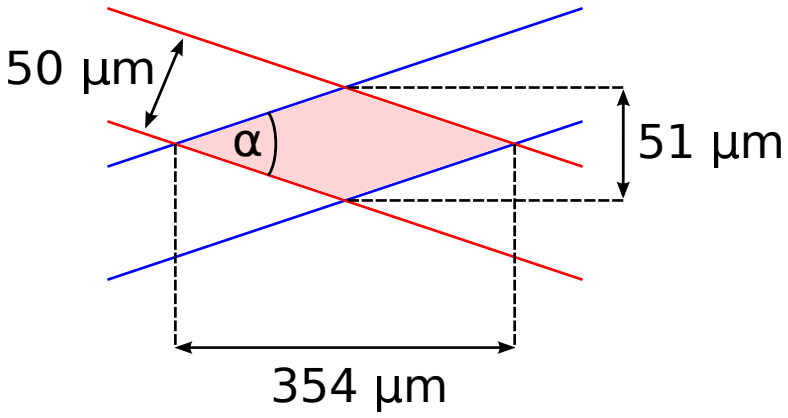


Figure 4.7: Red lines indicate the limits of the sensitive area associated with a strip on the p-side and blue lines represent the limits of the sensitive area of a strip on the n-side. The cross over region of two strips is shaded in red.

result in the strip having a larger solid angle and an increased event rate. The outer detectors have the longest strips which are about 30 cm which results in a total capacitance of about 62 pF when the longest strips of the A, B and C sensors are combined (see section 3.5.3).

4.2 Sensor Quality Assurance

The silicon tracker is constructed from 6 inner detectors and 24 outer detectors. The quantity of each sensor used for the construction is summarised in Table 4.2. A series of quality assurance tests have been performed at the University of Liverpool to ensure which sensors received from the manufacturer are suitable for the final assembly. A sensor is deemed to have qualified for use in the construction of the tracker if the number of defective strips on each side accounts for less than 1% of the total number of strips (9, 15 and 20 strips for an A, B and C sensor respectively). For a three-sensor (outer) detector this results in a dead channel percentage of at most 3%. All sensors have been subjected to the quality assurance process to identify a range of possible defects. The quality assurance process consists of: 1) visual inspection, 2) IV measurement, 3) life test, 4) strip probing. Each stage of the process is outlined and the data is presented.

Table 4.2: The number of each sensor type required for the construction of an inner layer and two outer layers.

Wafer Type	Quantity
A	24
B	30
C	24
D	6

4.2.1 Visual Inspection

The first step of the quality assurance process involved a visual inspection of each sensor to check for any cracks, scratches or chipped edges which could influence the operation of the sensor. An example of silicon sensor quality assurance testing and the results is given in [48] and [49] respectively. Of the sensors received only a very small number showed any defects under visual inspection. A few sensors had minor surface imperfections such as cracks or scratches, an example of a cracked sensor and a scratched sensor are shown in Figure 4.8 but such occurrences were on the order of 1 or 2%.

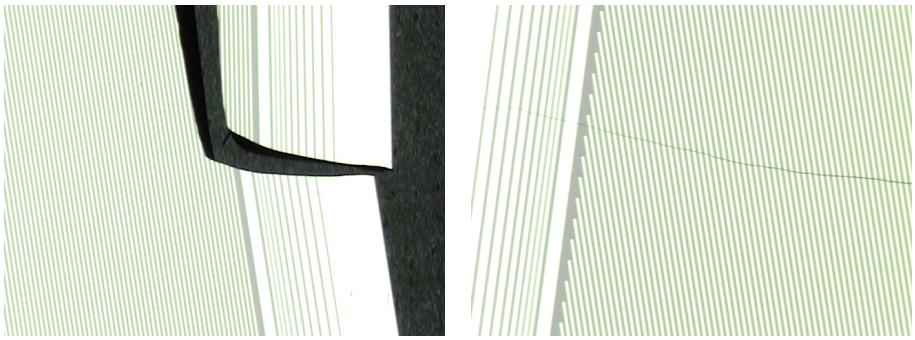


Figure 4.8: A microscope image showing two cracked sensors.

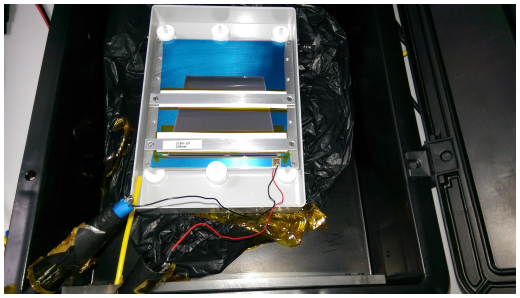
4.2.2 IV Measurement

After the visual inspection has been completed, the conductive properties of the sensor are tested by applying a reverse bias voltage across the sensor and measuring the current flowing through the junction. The total leakage current is a global sensor parameter that is of critical importance for the operation of a microstrip sensor. Small fluctuations of the leakage current represent noise at the detector

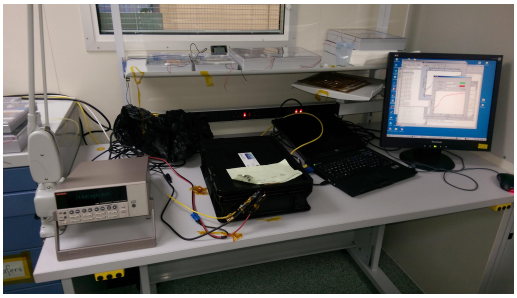
output which must be suitably small to ensure the smallest signal pulse heights can be obeserved. High values for the total leakage current indicate irregularities during the manufacturing process such as incorrect bulk impurity concentrations. An IV measurement is thus performed to confirm the diode conductivity of the sensor and quantify the sensor's global leakage current at $V_{bias} \gg V_{FD}$. The leakage current at each bias voltage is recorded and plotted to construct an IV curve of the sensor.

A reverse-biased sensor has a non-conducting depletion layer across the bulk region. A small reverse current will flow through the sensor, across the p-n junction, due to the motion of thermally generated charge carriers being generated within the silicon bulk. Some impurities can give rise to energy levels within the band-gap which increases the probability of an electron being excited to the conduction band. Large concentrations of such impurities would result in very large global leakage currents. As the bias voltage is increased the size of the depletion region grows with a thickness that is proportional to $\sqrt{V_{bias}}$.

As the depletion region expands, the depleted volume within which electron-hole pairs can be generated becomes larger and therefore the total sensor leakage current increases. When the sensor is fully depleted, the leakage current should reach a roughly constant value as the depletion region does not grow with increasing bias voltage. An IV measurement such as this has two useful purposes; firstly a measure of the total leakage current is obtained and secondly a rough estimate of the depletion voltage can be determined. A good quality sensor is expected to have a total leakage current of the order of 3 μA when the sensor is fully depleted (manufacturer quotes $V_{FD} = 53$ V for all sensor types).



(a) The sensor is placed within a black box during testing.



(b) The voltage supply, light-tight black box and computer are shown.

Figure 4.9: Photographs of the test setup used to carry out global current and voltage meausurements of every silicon sensor. The black and red cables connect the bias rail of either side of the sensor to the voltage supply and the yellow hose delivers dry nitrogen.

An IV measurement was carried out for every sensor whereby the sensor was placed into a light-tight black box with a small hose providing a nitrogen-rich environment as shown in Figure 4.9. The sensor was allowed to acclimatise for 30 minutes prior to beginning the testing. A voltage supply was used to bias the sensor which also recorded the measured leakage current at each voltage and saved the values to a computer for further analysis. Every sensor was reverse biased by connecting the n-side of the sensor to the Keithley k487 voltage supply and grounding the p-side to the same voltage supply. The bias was then slowly ramped up from 0 to 200 V at a rate of 1 V/s in 1 V steps and the leakage current was measured and saved at each step. At the end of the test, the voltage supply was gradually ramped down at a rate of 1 V/s. The IV measurements of all the accepted sensors which were used to construct the outer detectors are shown in Figure 4.10 (A,B and C sensors). Figure 4.11 displays the results of the IV measurements for every sensor used to construct the inner detectors (B and D sensors).

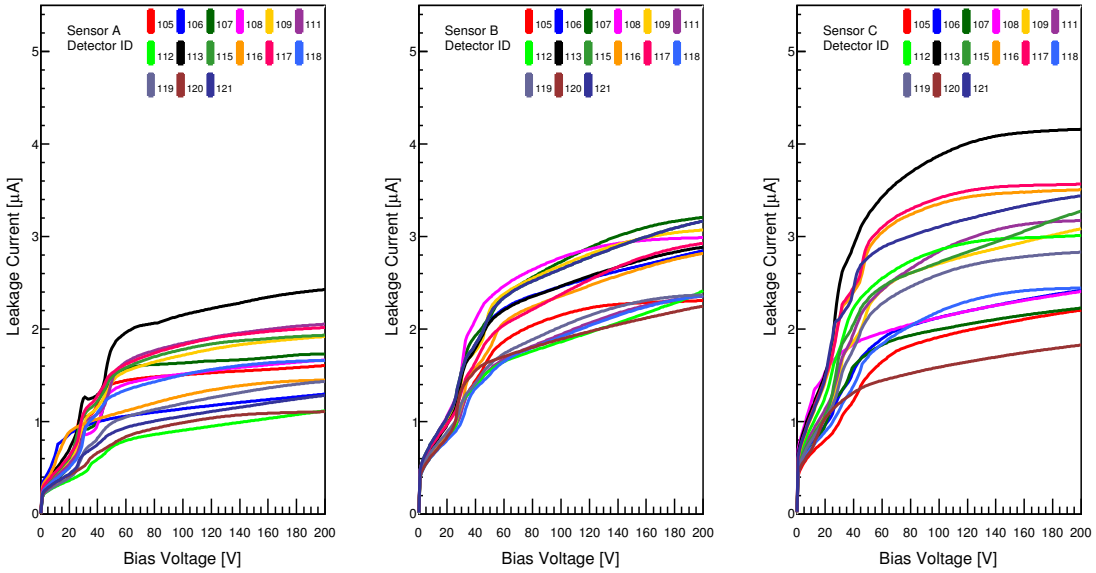


Figure 4.10: The IV curves obtained for all three types of sensor used to construct the outer detectors.

All of the sensors shown exhibit a small reverse current as expected from a reverse-biased p-n junction. It is possible that during the manufacturing process, the p-type and n-type implants of the sensor can become shorted which would result in a resistive IV curve. This measurement confirms that all of the sensors used for the construction of the detectors have a leakage current within the range 0.5-4 μA

when fully depleted and do not appear to show the presence of any p-n shorts. All of the sensors are of the same thickness but each has a different area and thus a different volume. The volumes of the A, B, C and D sensors are approximately 0.93, 1.44, 1.47 and 0.72 cm^3, respectively. A larger depleted volume will result in a larger leakage current meaning the C and B sensors are expected to have similar values for the leakage current when fully depleted and the A and D sensors should have a smaller leakage current in comparison. The data clearly shows that the A and D sensors have the smallest measured leakage currents.

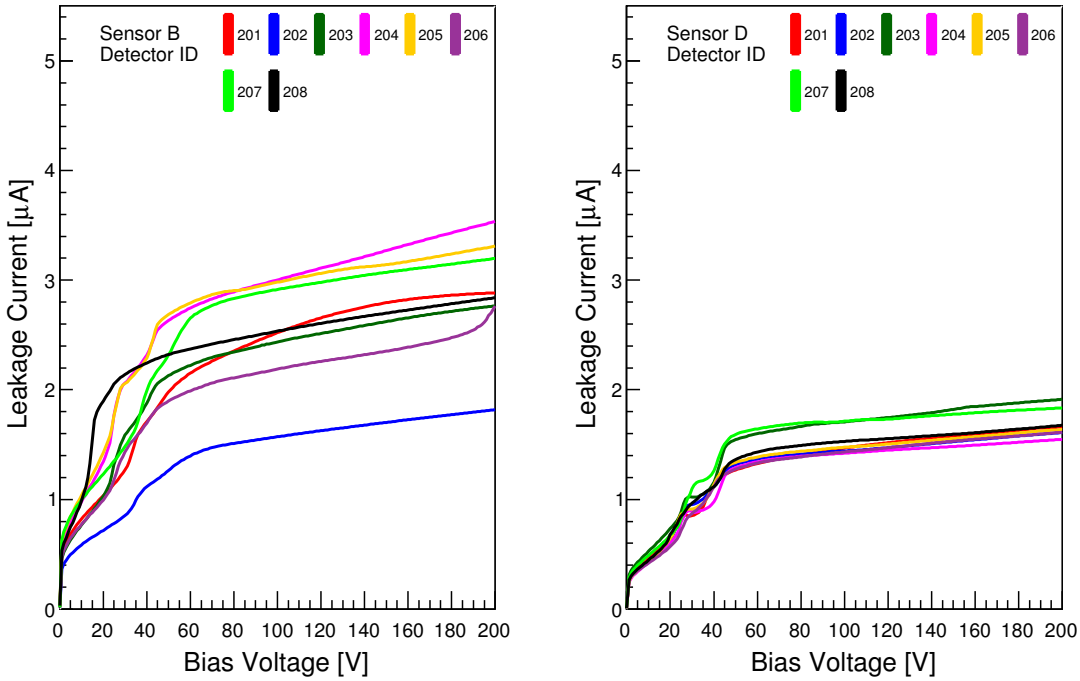


Figure 4.11: The IV curves obtained for the two types of sensor used to construct the inner detectors.

4.2.3 Life Test

It is important to test the sensor's global stability over a much longer time period than the 200 seconds it takes to run an IV measurement. A life test is carried out for every sensor whereby any long term instability can be identified. The sensor is again placed in a light-tight box with a hose supplying nitrogen just as in section 4.2.2. The sensor is then allowed to settle for thirty minutes prior to testing. A bias voltage, supplied by a Keithley k487 supply is slowly ramped up to a voltage of 150

V which ensures the sensor is over depleted. The sensor's leakage current is then recorded once every minute for a total of 72 hours for a bias voltage of 150 V.

Any breakdown effects that occur within the sensor will result in a significant alteration in the global leakage current meaning that the sensor is unusable. The stability of the global leakage current is monitored to verify that no substantial drift occurs over a period of time. Figure 4.12 and Figure 4.13 show the life measurements obtained for all sensors used for the construction of detectors. Over the 72 hour period, the maximum fluctuation in the leakage current of each sensor is typically no greater than $\pm$ 0.5 μA. Several life measurements (for example detector 117 sensor C) show a periodic behaviour which repeats every $\approx$ 24 hours. Such periodicity is probably due to the temperature of the clean rooms. The room temperature sometimes decreases overnight and steadily rises throughout the day resulting in a higher leakage current during the day than at night. This effect is not seen for all life measurements, probably because of the different clean room conditions on different days.

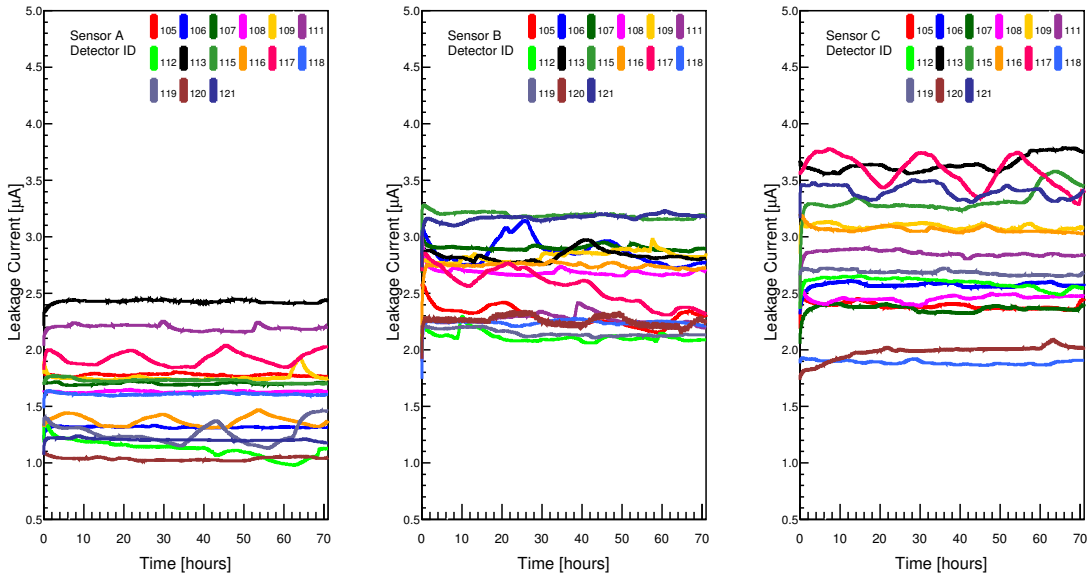


Figure 4.12: The leakage current of each sensor used to construct the outer detectors is shown for a time duration of 72 hours using a fixed bias voltage of 150 V.

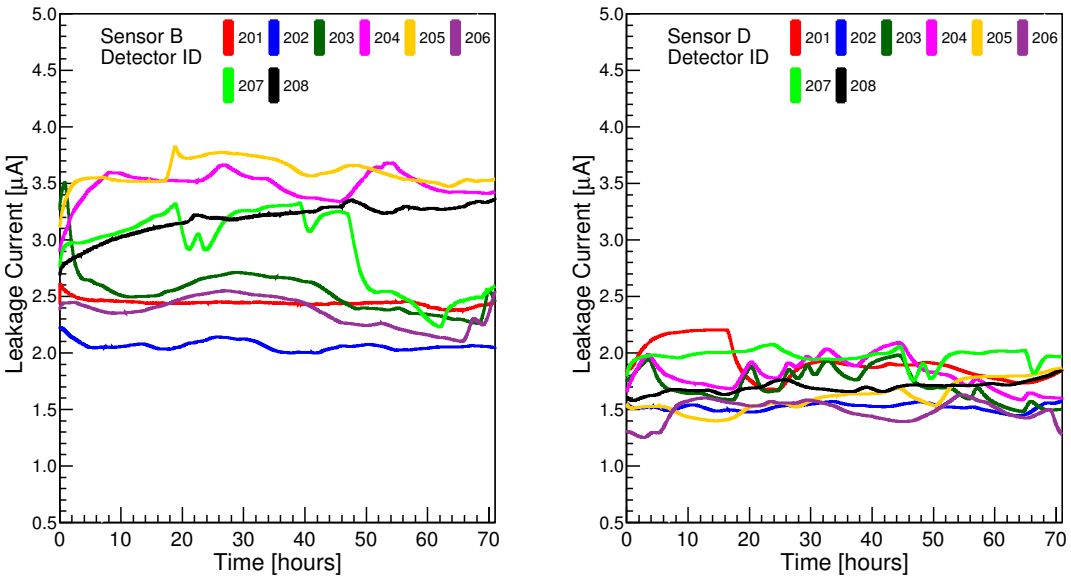


Figure 4.13: The leakage current of each sensor used to construct the inner detectors is shown for a time duration of 72 hours using a fixed bias voltage of 150 V.

4.3 Strip Probing

Provided that a sensor has passed both the visual inspection and the IV measurement, the sensor would pass to the next stage where individual strips are tested. An automated probe station using the National Instruments LabView 7.1 software was used to measure the properties of every strip for each sensor. The previous IV measurement does not eliminate the possible presence of individual high current strips in the sensor. High current strips result in noisy channels that could also inhibit the operation of neighbouring strips.

4.3.1 Measurement Procedure

The probe station was used to measure the leakage current of individual strips for a fully depleted sensor. The probe station was also used to determine the polysilicon bias resistor value for each strip by measuring a voltage drop across the resistor. Individual strips were tested using the probe station to make an electrical contact with the test pad that is located at the end of each strip (test pads previously shown in Figure 4.3).

Strips on both the n-side and p-side were tested. The p-side of a sensor was tested by firstly attaching the sensor's aluminium holding frame to an aluminium

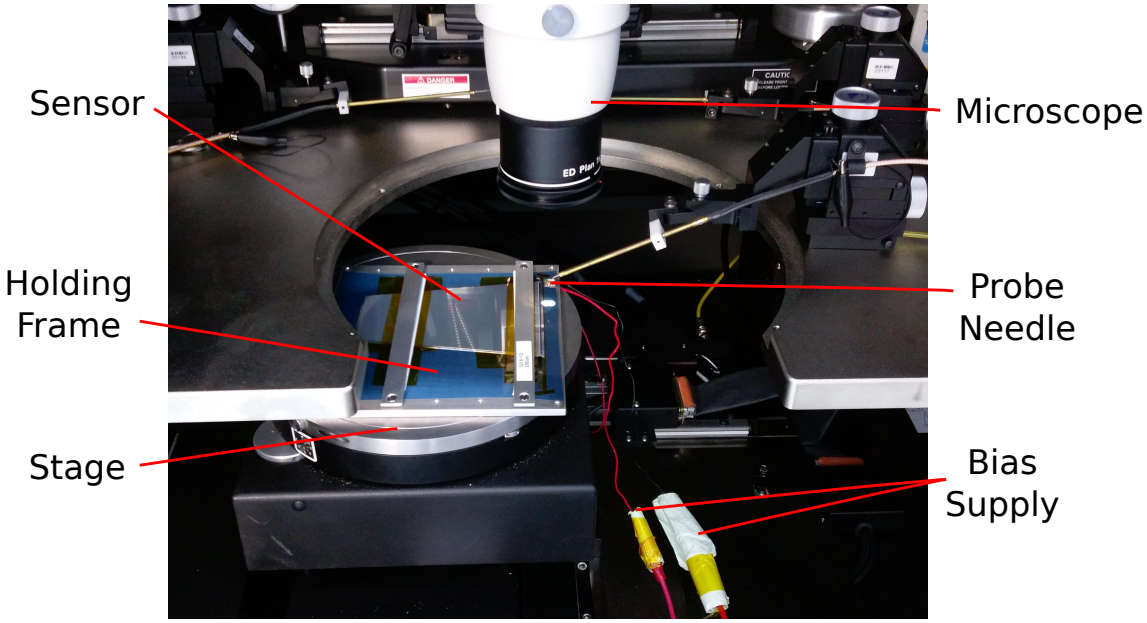


Figure 4.14: A photograph of the probe station interior. A sensor is placed in the holding frame which is positioned on the stage and the probe needle is used to contact the upper surface of the sensor.

test plate with the p-side facing upwards. The aluminium holding frame was then placed on the stage in the centre of the probe station. A vacuum is applied to the stage to ensure no movement of the holding frame occured during probing. A Keithley bias supply was connected to both the n-side and p-side of the sensor in order to ground the bias rail of the p-side and apply a bias voltage of 65 V to the bias rail of the n-side. Alternatively, the n-side is probed by grounding the bias rail on the n-side and applying -65 V to the p-side bias rail. The probe consists of a small tungsten needle which is connected to an ammeter and voltmeter. Figure 4.14 shows a photograph of the holding frame positioned on the stage within the probe station with the probe needle fixture.

Using a microscope and the LabView software, the positions of the first two test pads and the last two test pads were programmed by manually bringing the probe into contact with the pads. From these four reference points, the probe station is able to determine the positions of the test pads for all strips. The probe is then positioned above the first pad and the stage is raised in 5 μm steps to bring the test pad into contact with the probe needle, ensuring that the probe penetrates the oxide layer of the test pad. At this stage, the probe cabinet is closed, the lights are switched off and the bias supply is slowly ramped to 65 V (-65 V for n-side probing). The leakage current of a strip is measured by bringing the probe into contact with

the test pad and then short-circuiting the polysilicon bias resistor with an ammeter that connects the test pad to the grounded bias rail. The measured leakage current is typically of the order of 1-2 nA for a single strip. The value of the bias resistor is obtained by measuring the voltage drop across the bias resistor when the leakage current flows through the resistor. This is achieved by a voltmeter in parallel with the bias resistor. The manufacturers specifications quote an expected value for the bias resistor of 25-300 MΩ. A large range of possible bias resistance values is expected due to the sensitivity of the manufacturing process to small variations in dopant concentration.

The probe station is equipped such that measurements can only be conducted on a single strip at a time, hence it is not possible to measure the interstrip resistance. The manufacturer quotes an interstrip resistance of 50 MΩ for the p-side and 10 MΩ for the n-side. The current collected by a probed strip is free to flow to the bias rail via the ammeter. The neighbouring strips are at a slightly different potential to the probed strip as they are connected to the bias rail via their polysilicon resistors (typically 60 MΩ). Therefore it is possible for small currents to flow from the neighbouring strips into the strip under test.

4.3.2 Strip Defects

When identifying defective strips the two main possibilities are high current strips or shorted strips. A shorted strip occurs when the inter-strip resistance between two neighbouring strips is very small. A low inter-strip resistance can occur due to an electrical short between the aluminium metallisation of neighbouring strips or a short between the implants. A low inter-strip resistance results in two neighbouring strips acting as a single strip thus having a capacitance two times greater than the nominal single strip capacitance $C_{nominal}$ or

$$C_{strip} = N \times C_{nominal} \ , \tag{4.1}$$

for N shorted strips. Two shorted strips will subsequently have a leakage current that is approximately two times greater than the leakage current of an average strip, whilst also having a total polysilicon bias resistance R_{tot} that is approximately half of the average strip bias resistance. Two resistors R_1 and R_2 in parallel have a total resistance given by

$$R_{tot} = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}} \ , \tag{4.2}$$

so that if $R_1 = R_2$

$$R_{tot} = \frac{R_1}{2} = \frac{R_2}{2} \ . \tag{4.3}$$

The presence of shorted strips presents a very low-level risk to the operation of the sensor as part of a complete detector. The strips must still be bonded just like any other well-behaving strips but only one of the strips will be readout by the ASIC during operation of the detector.

Whereas shorted strips are deemed to be a defect with low-level severity, strips with high leakage currents are high risk and can render the sensor unusable. A high-current strip can be identified by observing a large leakage current and large voltage for the same strip. A larger leakage current will produce a larger voltage drop across the polysilicon resistor. High current strips (localised high current) can occur due to reasons such as inhomogenous bulk dopants, faulty strip implants, surface irregularities or non-depleted regions causing inhomogeneities in the electric fields [46]. Leaky strips with moderately high currents mean the front-end channel is very noisy and current signals induced within the strip will most likely be immersed in the noise.

For cases where the leakage current is two to three times greater than the average, the strip is too noisy to readout induced signals but the neighbouring strips should remain largely unaffected. In this situation the strip can still be bonded as per usual but the preamplifier of the ASIC will be configured not to readout the channel thus resulting in a dead channel. Each front-end channel has a preamplifier with a leakage compensation circuit, which can cope with a leakage current of up to 50 nA. If a strip has a leakage current greater than 4-5 times the average then the functionality of neighbouring strips can be disrupted as the leaky strip will draw excessive current from the neighbouring strips. A sensor with just a single high current strip prevents the sensor from being used during the construction as the strip may deteriorate over time and alter the behaviour of the sensor over a much larger region.

Figure 4.15 displays the raw data obtained from probing the n-side of an A sensor with a total of 889 strips. The geometry of an A sensor is such that the first 175 strips run the full length of the sensor and hence are all of equal length. For strip numbers greater than 175, the strips become increasingly shorter due to the trapezoid shape of the sensor, which results in smaller strip capacitances and smaller leakage currents. A reduction in leakage current results in a reduced magnitude of the voltage drop across the polysilicon bias resistor. The measured leakage current reveals an average leakage current of $I_{leak} \approx 2$ nA for the longest strips and an

average bias resistor of $R_{bias} \approx$ 60-65 MΩ for all strips. This particular sensor exhibits two pairs of shorted strips at strip numbers 427-428 and 557-558, which is shown in greater detail in Figure 4.16 for strips 557 and 558.

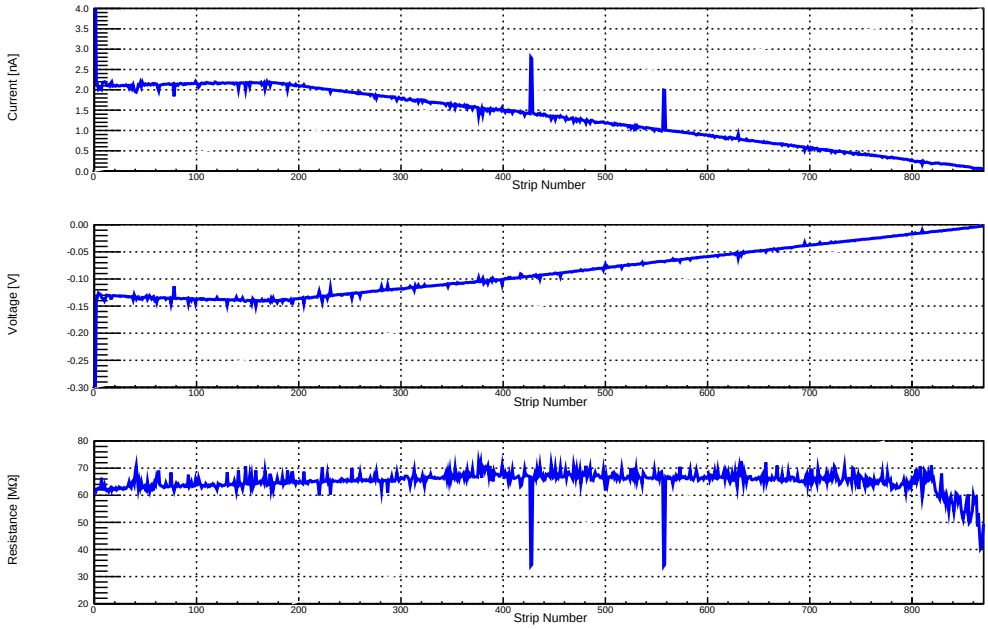


Figure 4.15: The leakage current, voltage and bias resistance obtained from probe testing an A type sensor. Two pairs of shorted strips can be seen and a smaller leakage current is measured for shorter strips.

Figure 4.17 shows an example of a sensor that was rejected due to a single strip with a leakage current that is four times greater than the average. An excessively high current (9.3 nA) was observed at strip number 751 and the bias resistance was similar to the averge strip bias resistance value. This indicates that the strip is not shorted to a neighbouring strip and the large current is due to a defect with strip number 751. The high current in strip 751 means that this strip presents a front-end channel that is too noisy to be read out and over time it may affect the operation of neighbouring strips.

4.3.3 Accepted Sensor Data

The example for an A sensor, shown in Figure 4.15 and Figure 4.16 was accepted and used to construct detector 105 (three-sensor outer detector). The leakage currents measured for every strip, for the three sensors used to construct outer detector 105, are shown in Figure 4.18 for strips on both the p-side and n-side. For a reverse

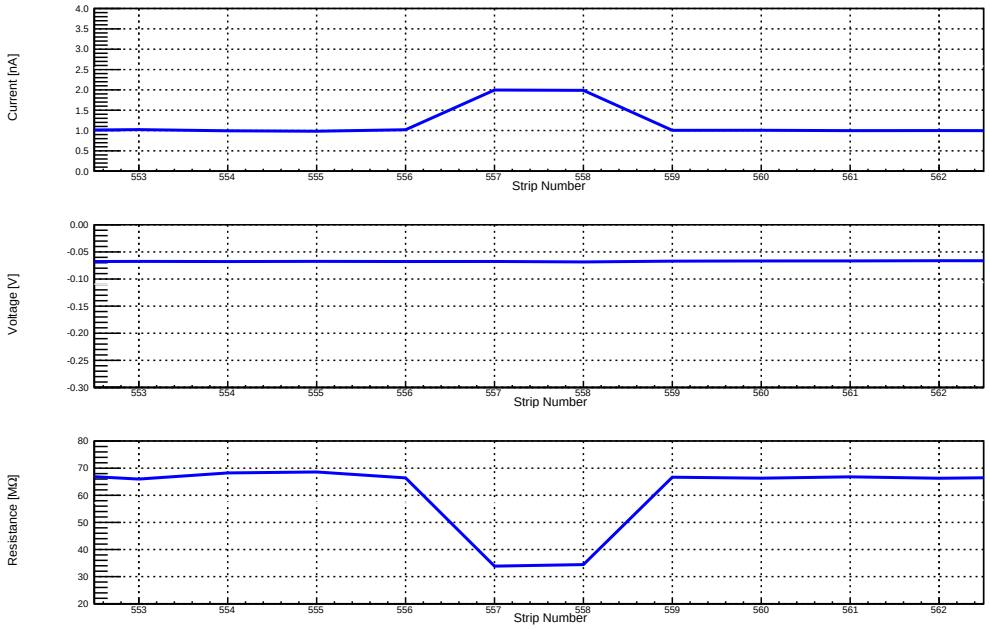


Figure 4.16: Strips numbers 557 and 558 are electrically shorted resulting in a leakage current two times greater than the average strip and a bias resistance that is half of the average.

biased sensor, the electrons are collected at the strips on the n-side and holes are collected on the p-side strips. The leakage current measured on the n-side has a positive polarity and the p-side has a negative polarity. For detector 105, the A sensor has two pairs of shorted strips on the n-side and one leaky strip (2.5 nA) on the p-side. The B sensor has two shorted strips on the n-side and the C sensor has two pairs of shorted strips on the n-side.

The geometry of the sensors is such that the longest strips of the A, B, C and D sensors are approximately $L_{maxA} = 12$ cm, $L_{maxB} = 11$ cm, $L_{maxC} = 8$ cm and $L_{maxD} = 9$ cm. It is expected that that longest strips of the A sensor (strips 1-175) should have a larger leakage current than the longest strips of the B sensor (strips 1-900). The longest strips of the C sensor (strips 1-1570) should have a leakage current that is noticeably smaller in comparison to those of the A and B sensor due to the smaller length. The measured leakage current of the longest strips of the A sensor is $I_{maxA} \approx 2$ nA. Therefore the leakage current of the longest strips of the C sensor I_{maxC} would be expected to be approximately

$$I_{maxC} = I_{maxA} \times \frac{L_{maxC}}{L_{maxA}} \approx 2 \times \frac{8}{12} = \frac{4}{3} \text{ nA} , \tag{4.4}$$

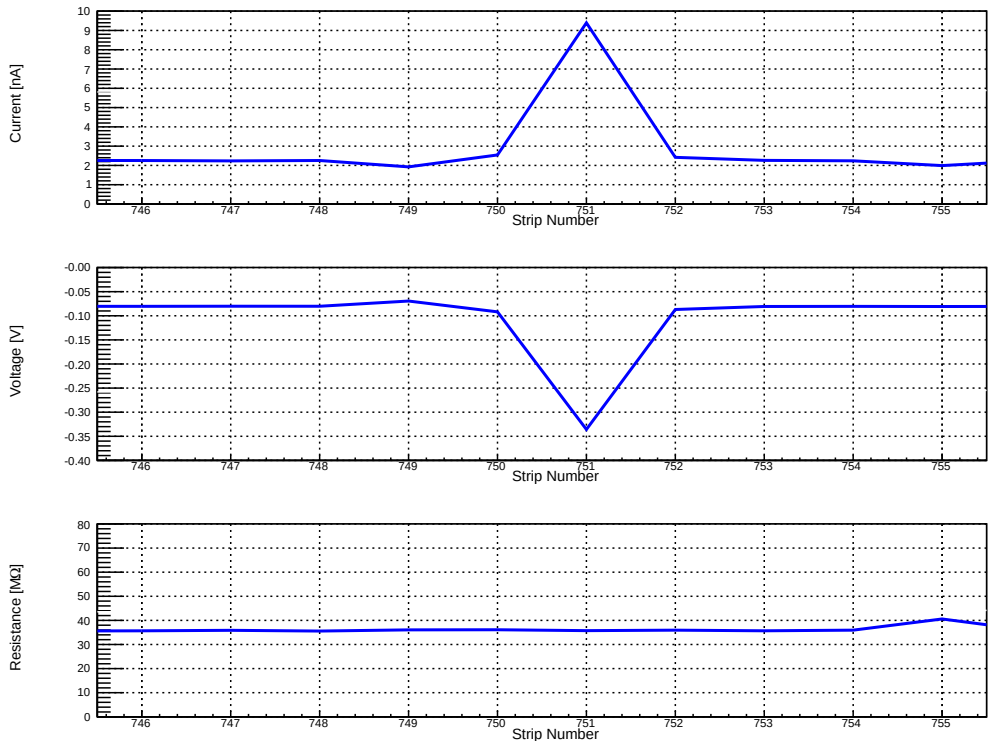


Figure 4.17: An example of a high current strip showing the leakage current, voltage and resistance values measured.

if the leakage current is proportional to strip length. On average, the measured leakage current for the longest strips of the C sensor was $I_{maxC} \approx 1.2$ nA, which confirms that the measured leakage current of a strip is proportional to the strip length.

4.3.4 Depletion Voltage Tests

The large ripples present in the leakage current measured on the strips of the p-side arise due to under depletion causing inhomogeneities in the electric field. The silicon is n-type bulk and as such the depletion region expands from the p-type strips through the bulk towards the strips on the n-side. The measured leakage current for each strip on the n-side exhibits uniform behaviour across the entire sensor. This suggests that the depletion region has fully extended from the p-side to the n-side, across the whole of the sensor bulk, when reverse biasing the sensor at 65 V. If the depletion region had not extended all the way to the n-side, then the measured leakage current would be very small on the strips of the n-side. The leakage current measured for each strip on the p-side shows large variation across localised areas.

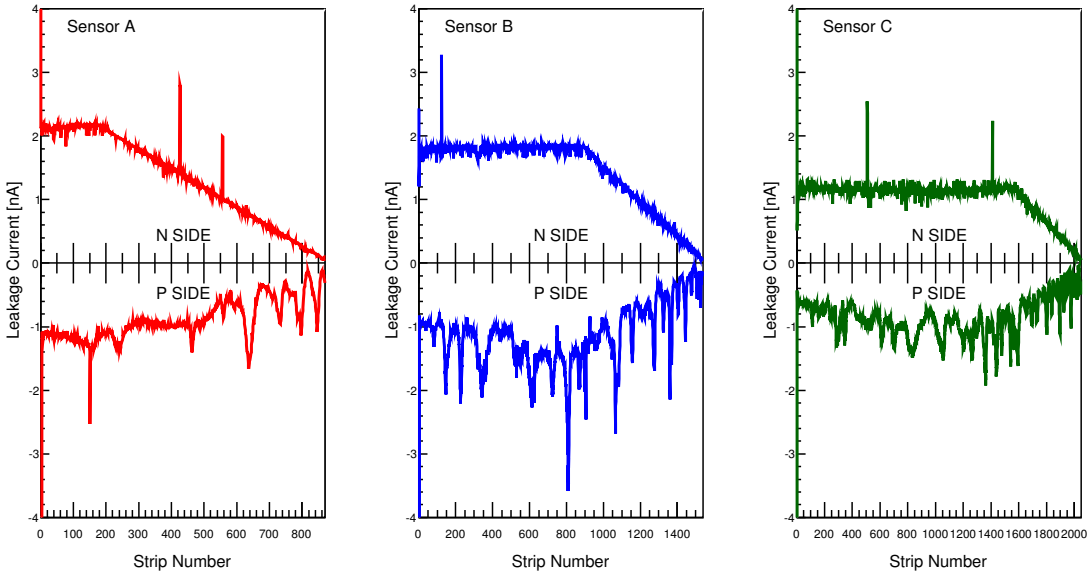


Figure 4.18: Leakage current for individual strips obtained during probing measurements of the sensors for outer layer detector 105. All data was gathered using a reverse bias voltage of 65 V applied to the opposite side of the sensor.

This suggests that undepleted regions exist, within the bulk volume, that are near to the p-type implants, which cause some strips to collect more charge than others. It is possible that a bias voltage of 65 V does not result in complete lateral depletion between strips on the p-side.

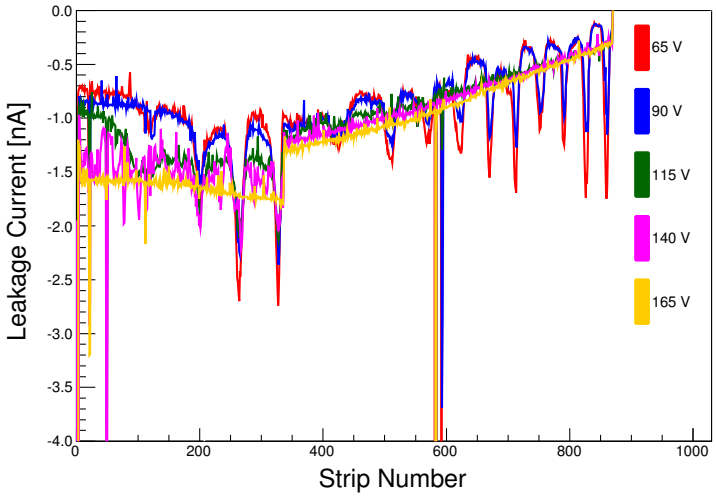
A test was done whereby a defective D sensor was probe tested using different voltages to understand what effect this had on the leakage current measured on the strips of the p-side. The voltages used for testing were 65, 90, 115, 140 and 165 V. The resultant leakage current, voltage and bias resistance values for each strip are plotted in Figure 4.19 for the different bias voltages. Increasing the bias voltage clearly removes the localised ripples in the measured leakage current on the p-side and results in all strips having similar values of leakage current proportional to their length. As expected, the measured bias resistance is the same for all voltages that were tested.

At 65 V, the localised non-uniformities are due to the sensor not having full lateral depletion. The depletion region grows from the p-type implants but the small volume between adjacent p-type implants is evidently not fully depleted at 65 V. For larger voltages of around 165 V, the depletion region is such that full lateral depletion between adjacent implants is achieved and the sensor shows no localised

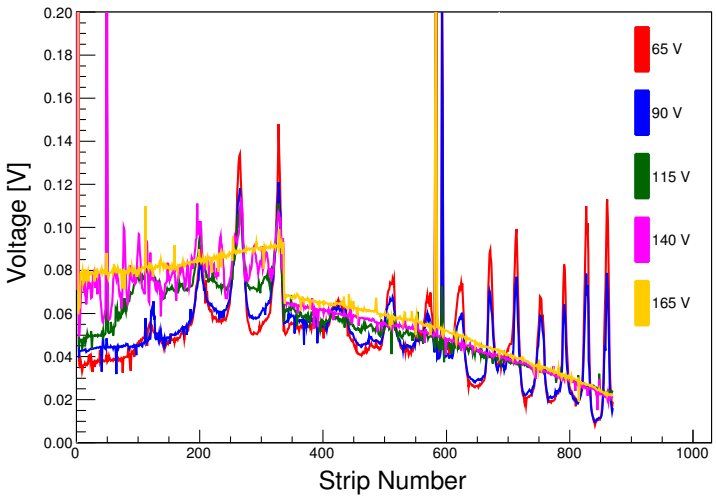
regions of high or low leakage current. The issue of incomplete lateral depletion was not fully understood when initial probe testing commenced. Consequently, all quality assurance probe testing data has been gathered using a bias voltage of 65 V. It appears that using a voltage of 65 V still enables the identification of high current defective strips.

4.3.5 Probing Results

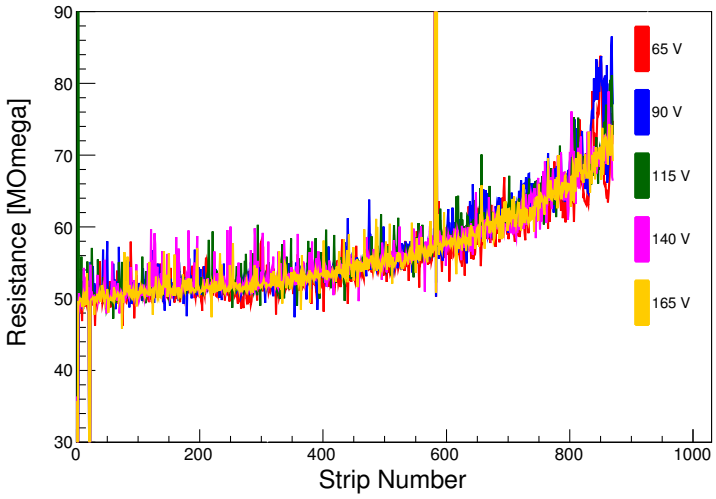
The results of all of the sensors that passed the probe testing requirements and which were subsequently used for the construction of outer detectors are shown in Figure 4.20, Figure 4.21 and Figure 4.22 for the A, B and C sensors respectively. The results of the measurements for spare detectors are included within the plots. The probe results for the sensors that have been used to construct inner detectors are shown in Figure 4.23 and Figure 4.24 for the B and D sensors respectively. The localised ripples can be observed on the strips of the p-side for all sensors, but strips with slightly larger values of leakage current can still be identified. For all the sensors that have been used for detector construction, there are no strips with a leakage current exceeding 6 nA. There are a relatively small number of leaky strips ($I_{leak} \approx$ 3-5 nA) which present a very low level risk. These slightly more leaky strips will be bonded to the front-end electronics and during detector operation, the readout for individual strips can be disabled if certain strips have too much noise.



(a) Leakage current.



(b) Voltage.



(c) Bias resistance.

Figure 4.19: The leakage current, voltage and resistance values obtained by probing each strip of a D sensor are plotted for different reverse bias voltages.

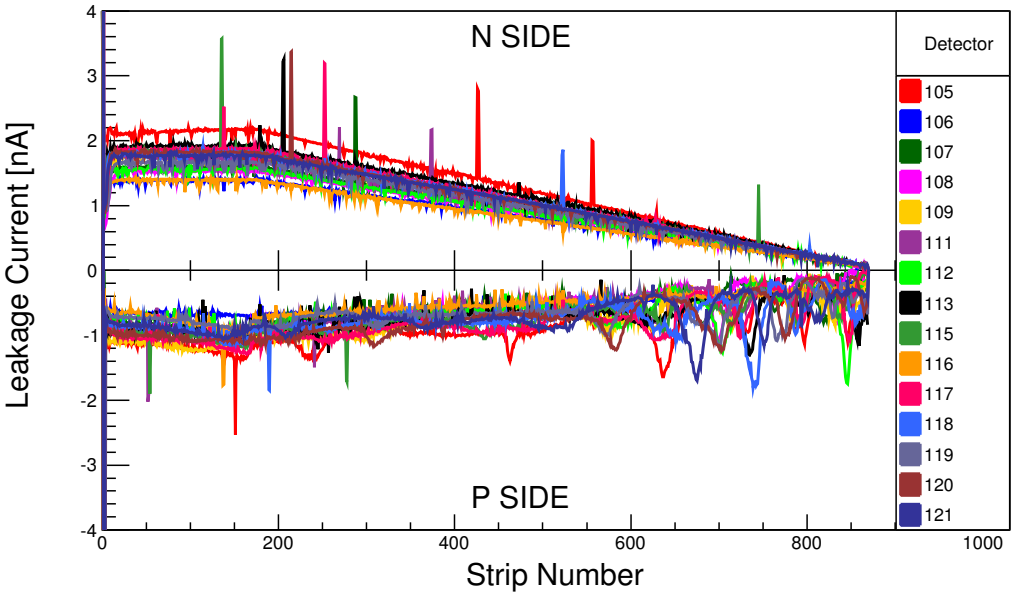


Figure 4.20: The leakage current measured for individual strips of all the A type sensors that have been used for construction of the outer layer detectors when applying a reverse bias of 65 V.

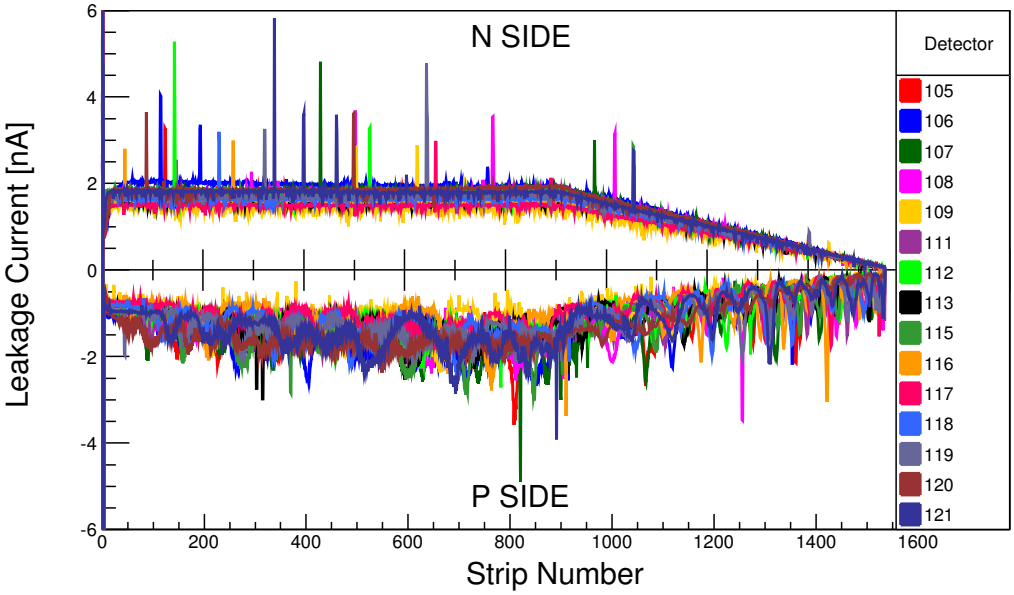


Figure 4.21: The leakage current measured for individual strips of all the B sensors that have been used for construction of the outer layer detectors when applying a reverse bias of 65 V.

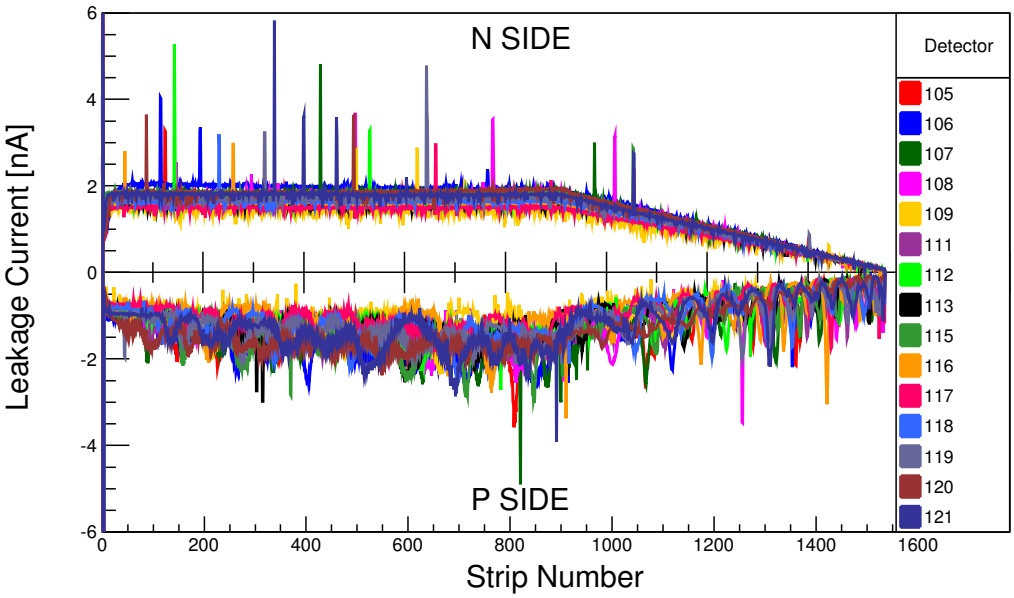


Figure 4.22: The leakage current measured for individual strips of all the C sensors that have been used for construction of the outer layer detectors when applying a reverse bias of 65 V.

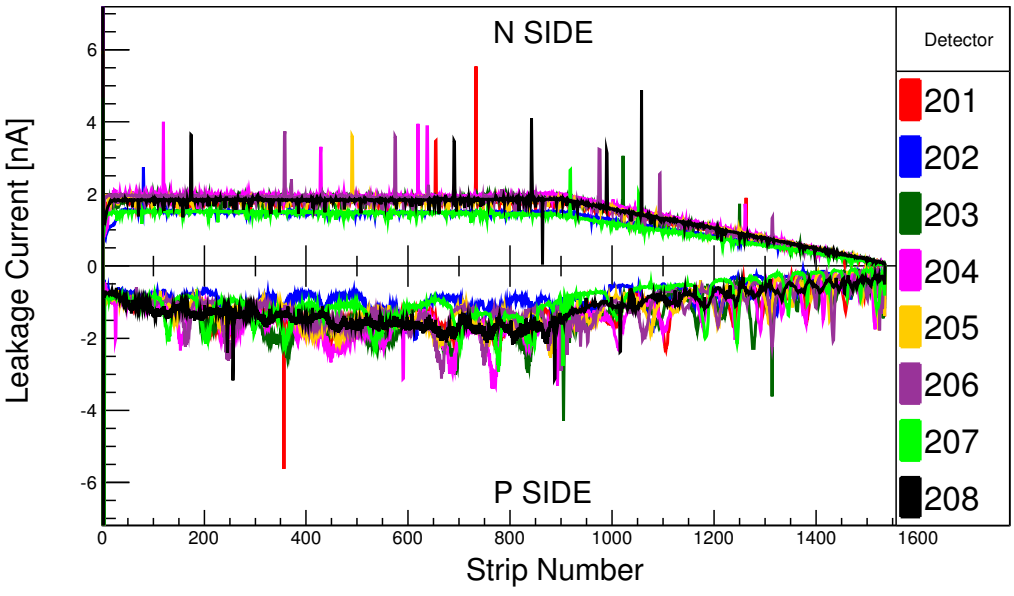


Figure 4.23: The leakage current measured for individual strips of all the B sensors that have been used for construction of the inner layer detectors when applying a reverse bias of 65 V.

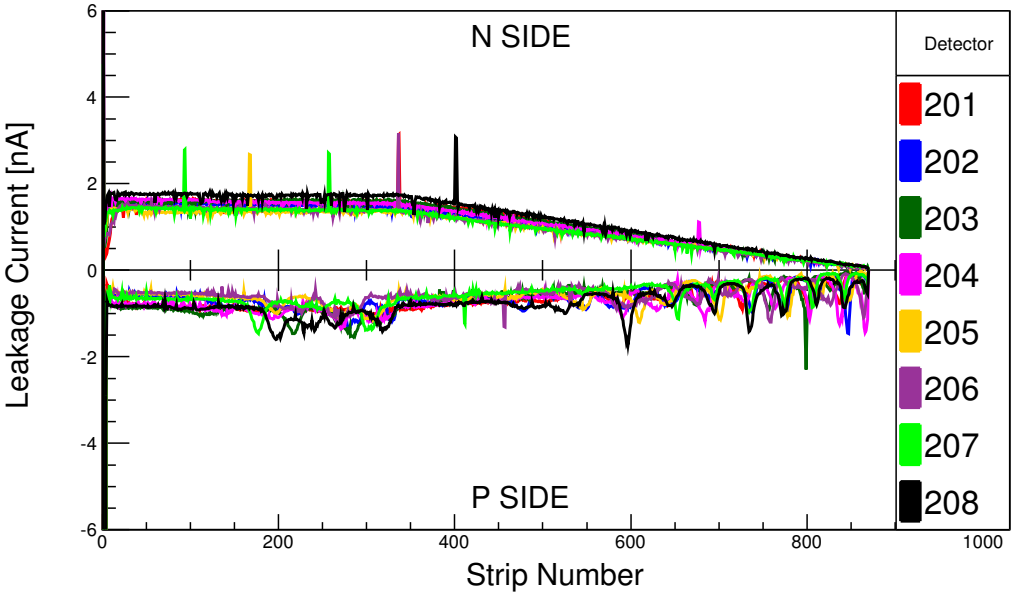


Figure 4.24: The leakage current measured for individual strips of all the D sensors that have been used for construction of the inner layer detectors when applying a reverse bias of 65 V.

4.4 Detector Construction

If a sensor satisfies all of the quality assurance requirements then it is suitable to be used for the construction of a detector. For the construction of an outer detector, three sensors must be combined. Two sensors are combined to produce an inner detector. A complete detector is composed of a silicon assembly and ASIC assembly which are independently constructed and then combined at a later stage.

4.4.1 Silicon Assembly Construction

When selecting sensors to combine it is desirable to match sensors so that the defective strips can be distributed to avoid dead areas accumulating in one area of the detector. Defective strips which are identified during probe testing represent a dead area of the sensor. For an outer detector, one strip from the A sensor is bonded to one strip of the B sensor which is then bonded to one strip of the C sensor. This results in the formation of a single straight strip, running the length of the detector, which is comprised of three smaller strips. A single defective strip in one sensor will result in the two strips from the other sensors also being unusable. The total number of defective strips for an outer module N_{Outer} is given by the sum of the number of defective strips for the three sensors A, B and C such that

$$N_{Outer} = N_A + N_B + N_C \ , \tag{4.5}$$

where N_A, N_B and N_C are the number of defective strips for an A, B and C sensor, respectively. The large number of sensors used means it is possible match certain sensors so that the bad strips on one sensor are separated geometrically from the bad strips of another sensor. Every defective strip is recorded during probing and the values can be passed to a programme which plots the geometry of a detector and the resultant dead areas due to defective strips. Figure 4.25 shows an example of how the visualiser programme has been used to match the sensors for outer detector 112.

After the sensors have been matched, they are then aligned with respect to each other by locating the fiducials at the corners of each sensor. Once aligned their positions are fixed by applying a vacuum to the underside which allows the entire sensor assembly to be aligned with an insulated carbon fibre frame. A thin glue layer is applied to the carbon frame which is then brought into contact with the upward facing side of the silicon sensors. The combination of silicon sensors glued

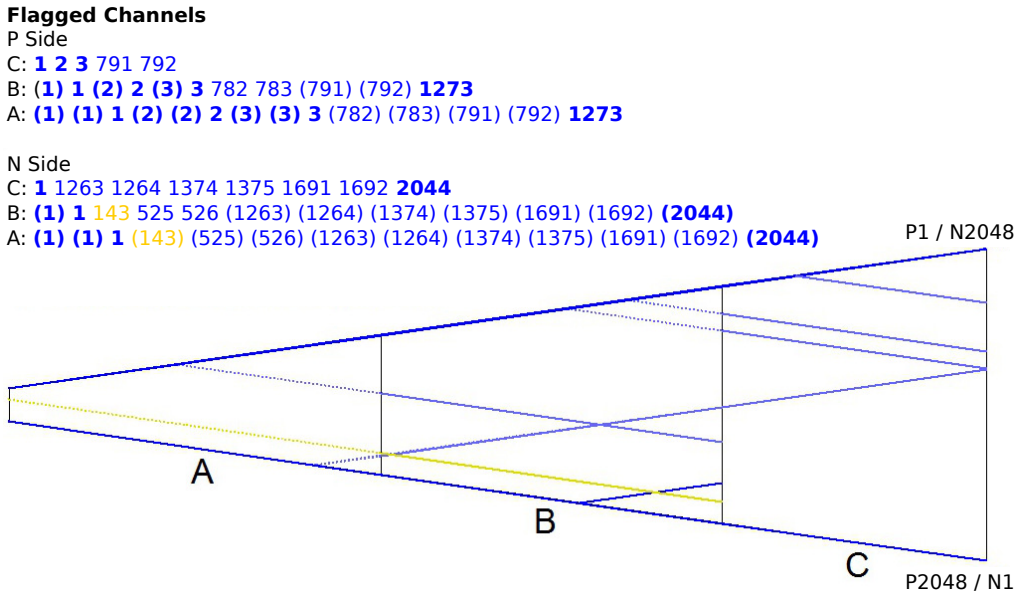


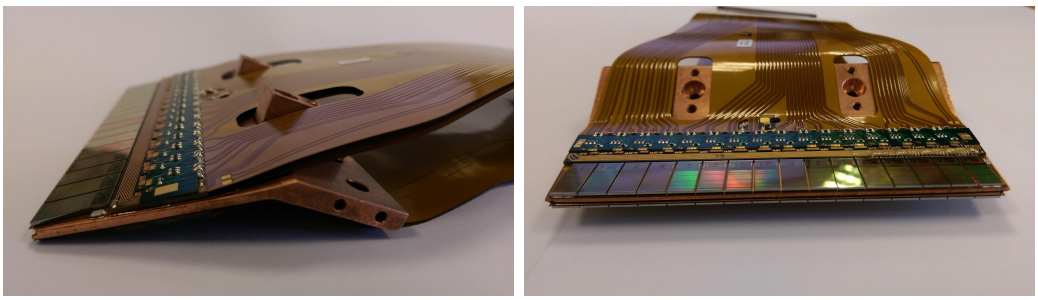
Figure 4.25: The defective strip numbers for each sensor are shown for both sides. Light blue lines indicate pairs of shorted strips, dark blue lines indicate leaky strips with a current roughly two times the average. The yellow lines indicate a strip with a leakage current three or more times greater than the average leakage current. There are a total of four shorted strips and four moderately high-current strips on the p-side. There are eight shorted strips, two moderately high current strips and one high current strip on the n-side.

to a carbon fibre frame is herein referred to as a silicon assembly. Once the glue has set, the sensors are initially ganged together via bonds connecting only the bias rails, which allows the global leakage current of the entire assembly to be tested by applying a voltage via the bias rail. This initial IV test will reveal any possible shorts between the sensor and the carbon fibre frame. The strips of each sensor are then bonded to the corresponding strips of the neighbouring sensor on both the n-side and p-side. After all strips have been connected on both sides, an IV measurement of the entire assembly is repeated to ensure no change of the global leakage current has occurred due to possible damage during bonding. A completed silicon assembly has a carbon fibre frame with the silicon sensors glued to the frame where the strips of each sensor are bonded to the strips of the next sensor.

4.4.2 ASIC Assembly Construction

The ASIC assembly provides the job of cooling and supporting the ASIC chips and connects the ASIC to a flexible printed circuit board (PCB). The ASIC assembly

is required to position the ASIC chips close to the sensors so that signals can be extracted from the sensor's strips. The digitised signals from each ASIC are then passed to the PCB which is connected to the buffer card. An ASIC assembly, shown in Figure 4.26a, is firstly constructed by glueing the underside of a flexible printed circuit board to a copper block. Using a vacuum chuck, 16 ASICs (12 for an inner detector) are glued to the upperside of the flexible PCB. The opposite face of the copper block is also glued to another PCB with ASICs glued to the opposite side. Figure 4.26b shows the ASIC assembly from the side which connects to the silicon assembly, where all 16 ASICs can be seen on one side. The result is an ASIC assembly consisting of two PCBs with a copper block sandwiched between them. By cooling the copper block, the heat generated from each ASIC will be dissipated and the ASIC temperature can be regulated.



(a) (b)

Figure 4.26: A photograph of an ASIC assembly for an outer detector showing the PCB, copper block and the 16 ASICs on the one side.

Each ASIC is equipped with a total of 87 back-end bond pads (see Figure 4.27) which are used to electrically connect the ASIC and the PCB to transfer signals and enable the ASIC to be controlled. Figure 4.28 shows a microscope image of the back-end and front-end bond pads prior to bonding the ASIC to the PCB and sensor. Some of the most important back-end bond pads include: clock line (SCLK), data line (SDAIN, SDAOUT), digital supply (VDDD), digital ground (GNDD), analogue supply(VDDA), analogue ground (GNDA), 100 MHz timestamp clock, 128 channel OR (HitOr128P). The bond pads labelled RENIn, RENOut, DAVIn and DAVOut are required for the daisy chain control that sequences the readout of data off each chip. The daisy chain readout structure is explained in detail in section 5.8. A full outer detector has an ASIC assembly consisting of 32 ASIC (16 on each side) that are all wire bonded to the PCB. The device is tested by powering up all of the ASIC and examining each ASIC with a thermal camera. The readout of each chip is then

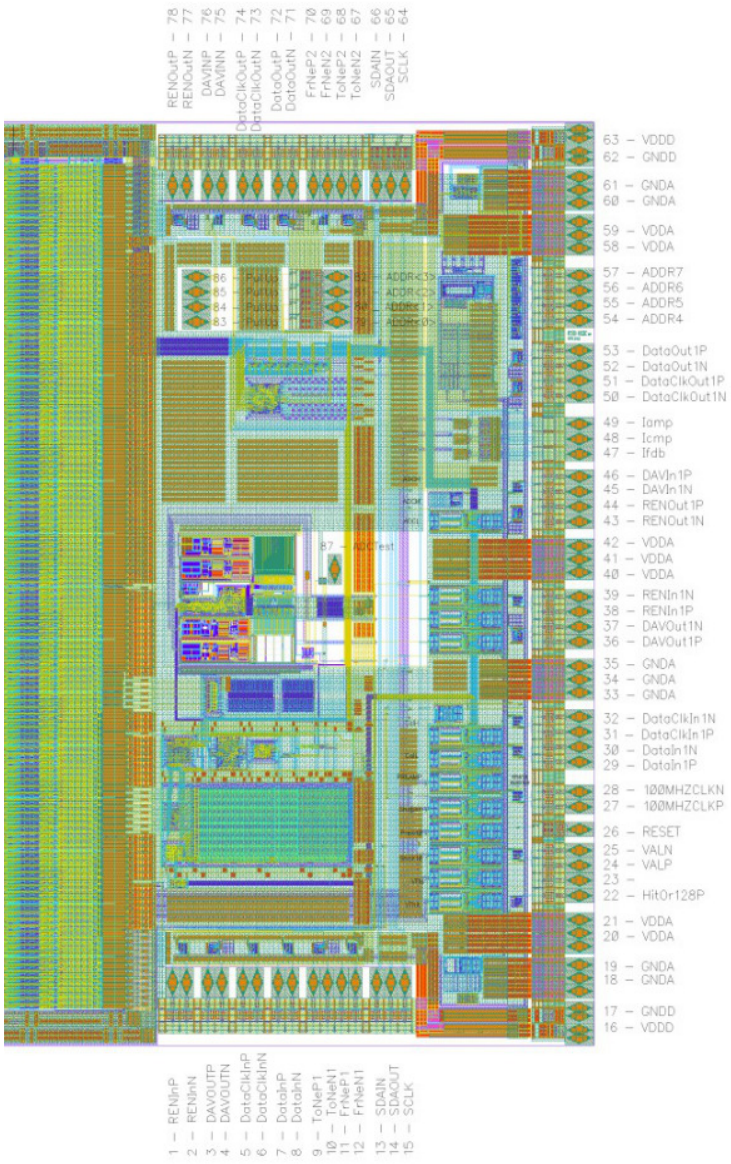
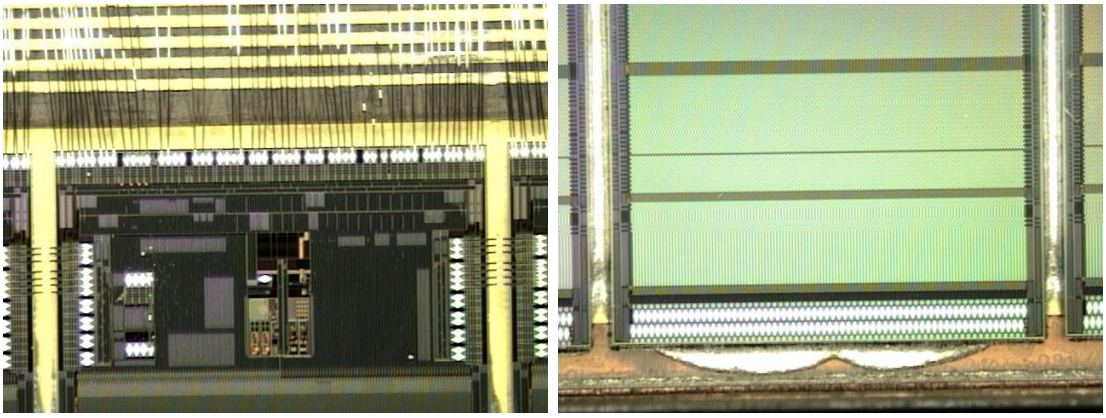


Figure 4.27: A diagram of the ASIC back-end showing all possible bond pads.

tested by applying a test pulse to four channels.

4.4.3 Completed Detector

A complete detector is formed by connecting the ASIC assembly to the silicon assembly. The two assemblies are unified by glueing the copper block to the two inward facing sides of the carbon fibre frame. Each ASIC has 128 front-end bond pads which are wire bonded to the individual strips of the sensor to produce a complete



(a) Back-end bond pads. (b) Front-end bond pads.

Figure 4.28: A picture taken with a microscope showing the different bond pads of the ASIC.

detector. An example of a completed outer detector is presented in Figure 4.29. For an outer detector, the 2048 strips (one side) of a C sensor are each bonded to an ASIC front-end bond pad. For an inner detector, a total of 12 ASIC are bonded to the 1536 strips (one side) of a B sensor. Signals induced within the silicon sensor result in a current within a strip that is extracted by the ASIC which is DC connected to the strip. The ASIC processes and digitises the signals of each strip which are then passed to the buffercard, via the flexible PCB, and then on to the μ-TCA crate before being eventually stored.

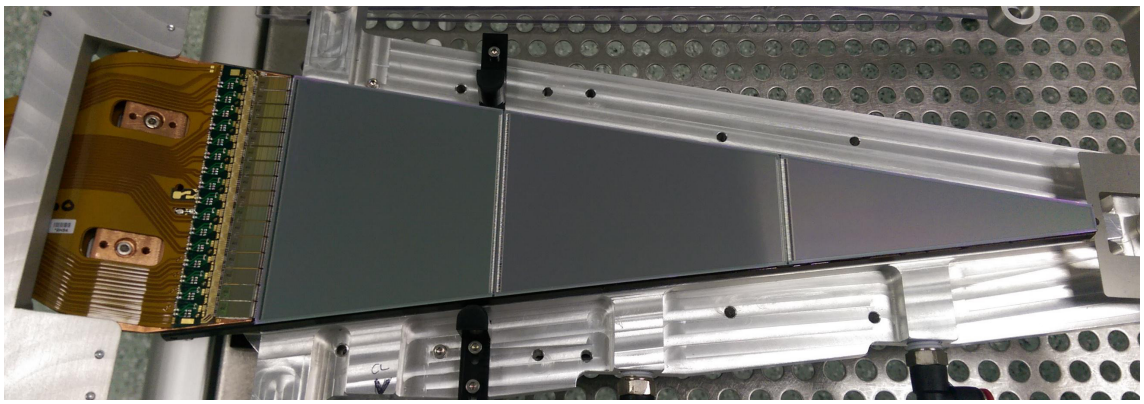


Figure 4.29: A photograph of a completed outer detector.

4.5 Final Detector IV

A completed detector has all of its strips bonded to an ASIC where every ASIC is bonded to the PCB. All previous quality assurance tests were conducted by biasing the strips via the bias rail. The inclusion of bias resistors was primarily designed to enable initial testing of sensor properties by biasing the bias rail. A completed detector can be biased by applying a voltage directly to each strip by virtue of the ASIC's DC connection with the bond pad.

As a final quality assurance test, the IV properties of each completed detector have been tested by reverse biasing each detector up to 80 V. The detector is reverse biased by applying a voltage to each ASIC on the n-side and grounding all ASIC on the p-side. A final IV measurement is carried out to ensure that no significant changes have occured in the measured global leakage current due to connecting the two assemblies. The final IV measurement should thus be very similar to the IV measured for a lone silicon assembly. Figure 4.30 shows the characteristic IV measurement for all of the completed outer detectors. For all completed inner detectors, the final IV measurement is shown in Figure 4.31. All completed detectors show an IV relationship that is expected for a reverse biased p-n junction, with no apparent shorts between the n-side and p-side. The global leakage current of an outer detector is expected to be significantly larger than that measured for an inner detector due to the outer detector having one more sensor and hence a significantly larger volume.

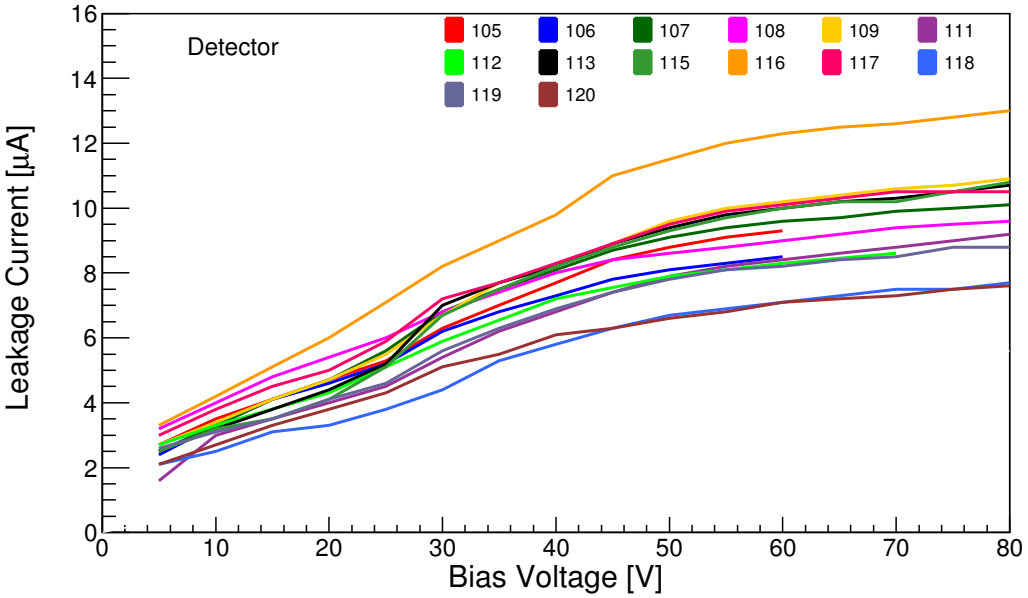


Figure 4.30: The final IV measurement for all completed outer detectors.

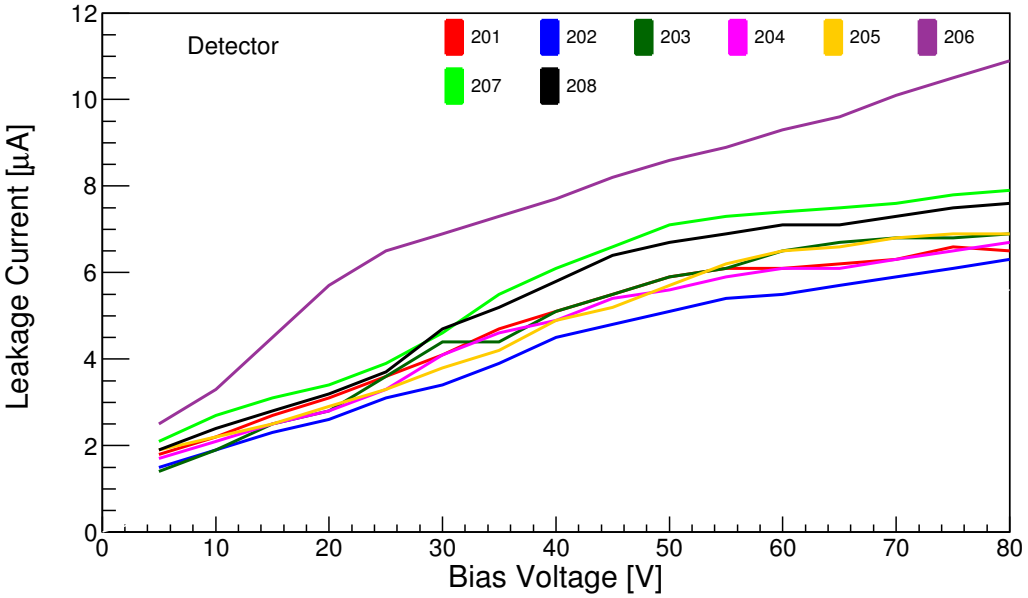


Figure 4.31: The final IV measurement for all completed inner detectors.

Chapter 5

R^3B ASIC Architecture

The main functions of the R^3B Application Specific Integrated Circuit (ASIC) are described and the design specifications are included. A breakdown of the ASIC's functional blocks and their signal processing properties is given. The signal processing steps by which the ASIC determines the energy and time of an input pulse are explained using analogue electronic principles. The theoretical gain of each of the ASIC's pulse processing stages is calculated and used to determine the entire front-end gain for a single channel. The results of theoretical calculations will be used for comparison with real data in Chapter 6. The data format and readout logic are discussed.

5.1 ASIC Specifications

The silicon tracker has a very large number of strips contained within a small volume where the signals from each strip must be individually read out. Such a fine strip pitch requires a high density front-end electronics, which is achieved via the custom designed R^3B ASIC. The layout of the R^3B ASIC is shown in Figure 5.1, where the functional blocks are labelled. The R^3B ASIC has been designed for the purpose of reading out, processing and digitising the individual signals from all 116736 channels of the R^3B silicon tracker with 8 keV (RMS) energy resolution and up to 5 ns timing precision.

The ultimate purpose of the ASIC is to measure the charge at the preamplifier input and display it in the form of a 12-bit binary number whilst concurrently displaying the time of the hit in the form of a 15-bit binary number. The time and energy information for each channel have an associated channel identification

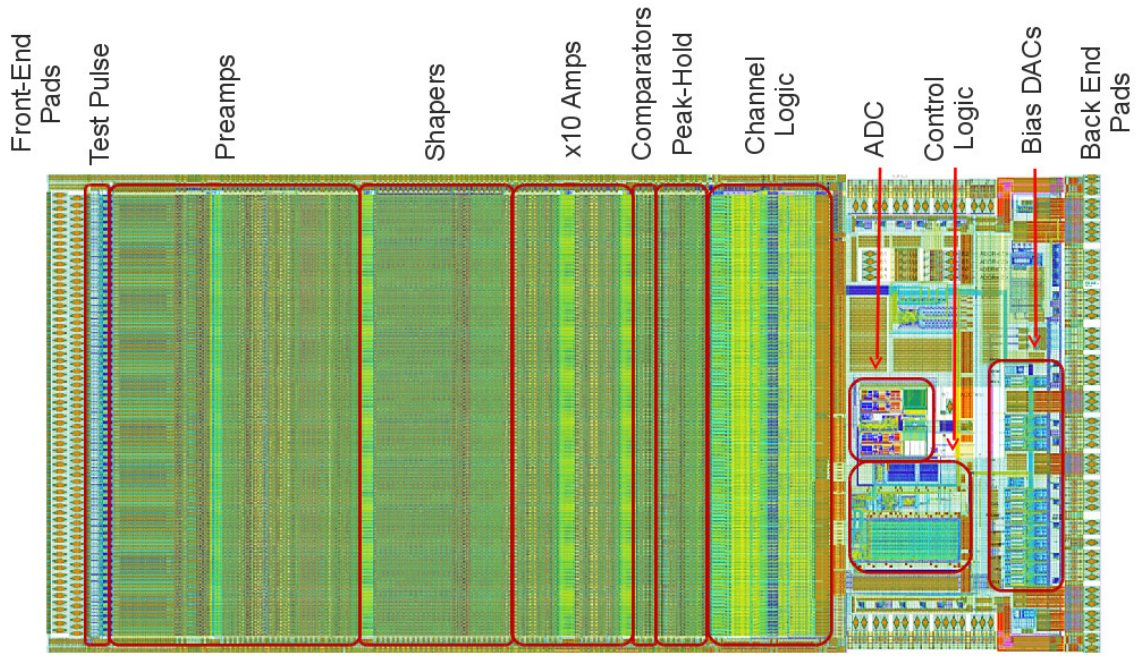


Figure 5.1: The layout of the R^{3}B ASIC's functional blocks.

number which corresponds to a strip and hence a position. The channel address is identified by a 7-bit number and each ASIC has a unique 10-bit chip address. A single R^{3}B ASIC supports the operation of 128 independent front-end channels. Each individual ASIC channel is connected to one strip of the sensor via a front-end bond pad.

Each ASIC has a size of 12.9×6.2 mm^2 and is glued to a PCB (Printed Circuit Board), which is cooled on the underside by a copper block. The ASIC design specifications are outlined in Table 5.1. In total, 32 ASIC are required to operate both sides of a complete detector for the outer layers and 24 ASIC are needed to read out both sides of a detector for the inner layer.

A charge signal is extracted from a strip of the sensor and passed to the preamplifier input. The ASIC has been designed to process both positive and negative signals at the preamplifier input. The role of the ASIC is to process the signal and identify a hit. A negative charge signal is collected at the n-side strips and a positive signal is collected at the p-side strips. The ASIC has two possible configurations: "hole mode" is used to process positive input signals and "electron mode" processes negative input signals. Processed signals are either discarded or digitised and read out depending on the amplitude of the input signal. Charge sharing between adjacent strips will result in small amplitude signals in strips neighbouring a hit strip.

Table 5.1: The main specifications of the R^{3}B ASIC.

Input Signal Polarity	negative or positive
Coupling to Detector	DC
Detector Leakage Current	0-100 nA
Detector Capacitance	few pF to $\approx$ 80 pF
Maximum Data Rate	5 kHz/channel
Energy Range	0.04 - 50 MeV
Energy Resolution	8 keV (RMS)
Timestamp	100/200 MHz clock
Peaking Time	0.5 μs - 8.0 μs

The ASIC has been designed to read out the charge from channels adjacent to a hit channel, irrespective of the neighbouring channel's signal amplitude.

The variable length of the detector strips requires that the ASIC be able to cope with a large range of input capacitance. For an outer detector, the longest strips of the A, B and C sensors result in a maximum strip capacitance of up to about 60 pF (according to calculations in section 3.5.3). Each channel of the ASIC can accommodate a maximum input capacitance of about 80 pF. For an input capacitance greater than 80 pF, the larger rise time of the preamplifier results in greater power consumption of the preamplifier. The ASIC has a total power consumption of approximately 1 W to allow regulation of the ASIC temperature during operation under vacuum using the tracker's electronic cooling system.

The majority of experiments will require the readout of signals generated by protons with an energy in the range 50-400 MeV and with a rate on the order of 10^2 Hz/ch. Experiments using a dense liquid hydrogen target are also envisaged where a data rate of several kHz is necessary and the smallest measured signal is expected to have a signal amplitude of approximately 100 keV. The ASIC has been designed with a large dynamic range due to the wide range of experiments that are possible at R^{3}B which may require the detection of sllow heavy ions.

Each channel within the ASIC consists of a charge-sensitive preamplifier, programmable shaper, peak-hold, two gain amplifiers, two comparators and a control logic as well as test pulse injection circuitry. A block diagram depicting the signal processing stages for a single channel of the R^{3}B ASIC is shown in Figure 5.2. All of the channels within a single ASIC share an analogue multiplexer, ADC and data buffer. The charge signal is initially extracted from a strip of the sensor by the preamplifier. The preamplifier of every front-end channel is DC connected to a strip of the sensor. The ASIC copes with detector leakage currents of both polarities

by virtue of a leakage compensation circuit which removes the leakage current that would otherwise have been integrated by the preamplifier.

After amplification the signal is then passed to a programmable shaper (slow signal path) as well as a $\times 10$ gain amplifier (fast signal path). The slow signal that is passed to the programmable shaper is processed to obtain a pulse height measurement, which is proportional to the energy loss in the sensor. The fast signal that is passed from the preamplifier to the gain amplifier and then to a comparator, can provide a high precision measurement of the time at which the charge pulse occurred by measuring the rising edge of the preamplifier output.

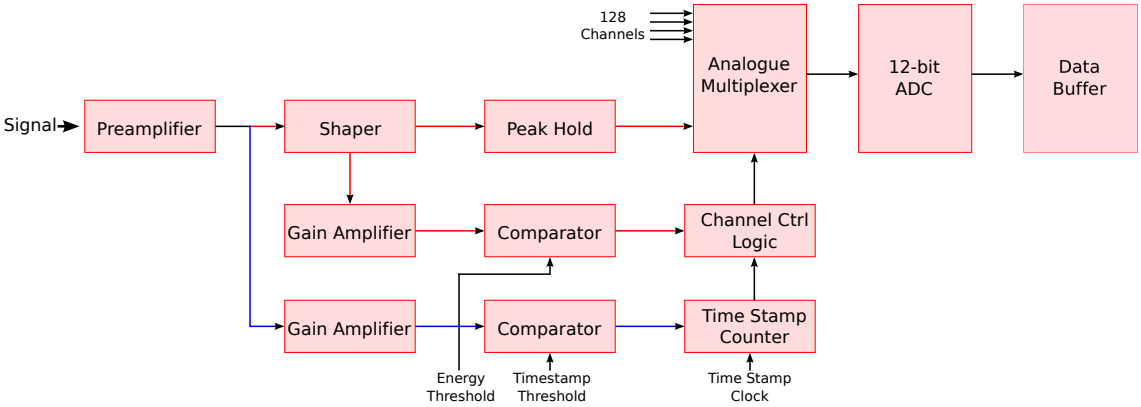


Figure 5.2: A block diagram of the R^{3}B ASIC's signal processing stages for a single channel. Blue lines represent the slow signal path whereby pulse the pulse height is measured. Red lines indicate the fast path used for timing measurements.

5.2 Preamplifier

The output signal from the strip of a silicon sensor is always of very low amplitude (order of pC) and of very short duration (order of ns). A signal such as this would be strongly perturbed by even low level noise whereby measurement of the signal's amplitude and time would result in large errors. The preamplifier forms the first stage of the signal processing chain of the R^{3}B front-end electronics. The preamplifier allows for extraction of the signal from the sensor without significantly degrading the signal to noise ratio. The preamplifer must be situated near to the electrode to minimise noise pick-up and provide well controlled amplification of the input signal with minimum interference from external noise sources.

The preamplifier of the R^{3}B ASIC is a charge-sensitive preamplifier. This is the most common choice of amplifier for reading out signals from detectors as its

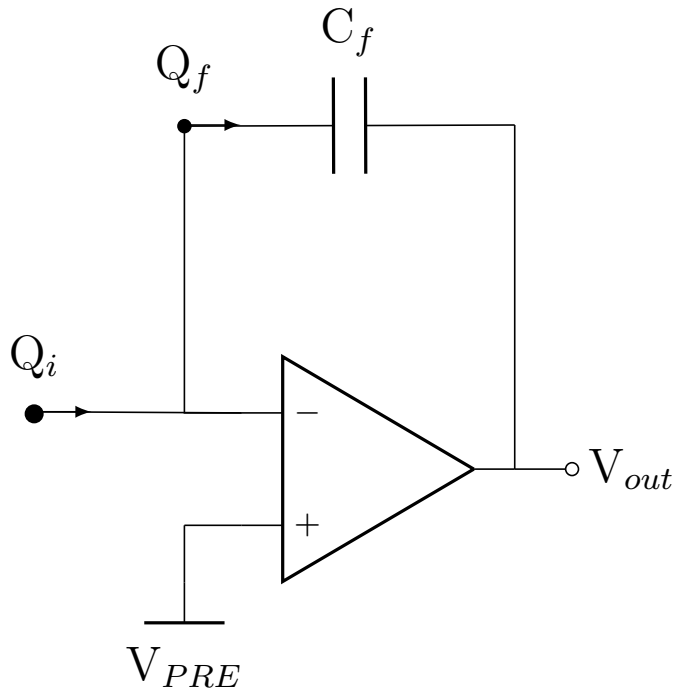


Figure 5.3: A circuit diagram of a charge-sensitive preamplifier with feedback capacitance C_f. A charge Q_i is extracted from the detector and passed to the amplifier input.

operation is independent of detector capacitance. Detector capacitance can vary depending on factors such as applied bias voltage (see section 3.3). A circuit diagram showing the case for a signal charge Q_i, from a sensor strip, at the input of a charge-sensitive preamplifier is displayed in Figure 5.3. The charge-sensitive preamplifer consists of an operational amplifier with a capacitor C_f in negative feedback. The operational amplifier has a differential input and a single ended output. The inverting input is denoted by a "-" and the non-inverting input is represented by the "+" symbol. The negative feedback configuration is where the output of the amplifier is connected with the inverting input of the amplifier. A charge Q_i can be extracted from a strip of the detector and passed to the inverting input of the preamplifier. The non-inverting input of the preamplifier is connected to a programmed reference voltage V_{PRE}. A typical operational amplifier compares the voltages at its two inputs and then outputs a signal V_{out} that is proportional to the difference between the two input signals. If a voltage difference V_{in} is applied across an operational

amplifier's differential input, the amplifier output will be

$$V_{out} = -A \times V_{in} \ , \tag{5.1}$$

where A is the amplifier gain. The negative feedback configuration results in a fraction of the output signal V_{out} being passed back to the inverting input. Negative feedback allows the gain of the amplifier to be controlled and prevents the amplifier output from saturating.

A resistor R_f in negative feedback can be included (in parallel with C_f) to provide a resistive feedback element which allows the capacitor to discharge and determines the exponential decay constant of the preamplifier output $\tau_f = R_f C_f$. An example of an output pulse from a preamplifer with a capacitor and resistor in negative feedback is shown in Figure 5.4. Alternatively, the resistor can be replaced by a switch which allows the preamplifier to be reset. Using a reset switch in place of a feedback resistance will result in a preamplifier output with no exponential decay component.

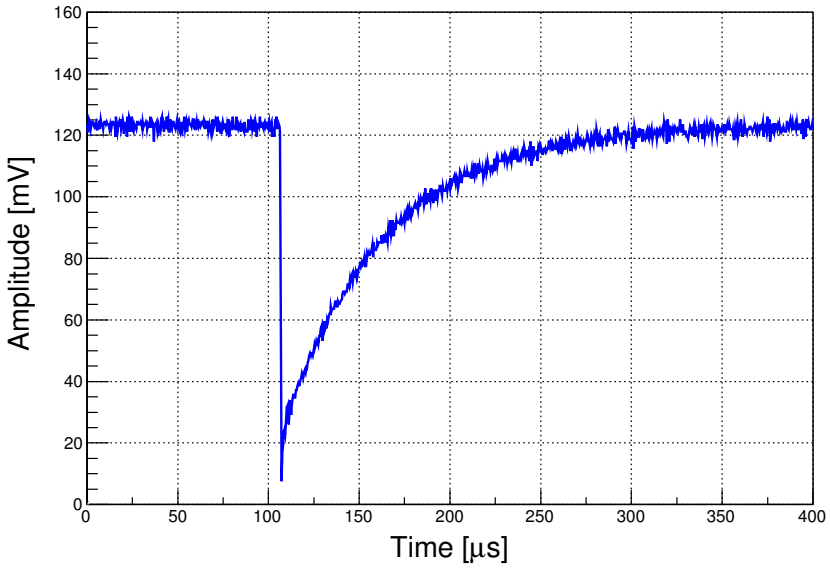


Figure 5.4: A typical output pulse from a preamplifier with a resistive feedback element. The output has a fast rise time and gradual decay tail.

A charge-sensitive amplifier is characterised by a high input impedance and a low output impedance. For simplicity (and for ideal calculations) the input impedance can be assumed to be infinite which results in no current flow into the amplifer input. All charge at the amplifier input Q_i instead flows through the feedback

circuit. Therefore, a charge-sensitive amplifier connected to a strip of the detector, will extract the signal charge which is then integrated onto the feedback capacitor. The amplifier gain is thus dependent upon the feedback capacitance of the amplifier. If all of the charge at the input of the amplifier Q_i charges up the feedback capacitor then the charge integrated onto the feedback capacitance is $Q_f = Q_i$. The charge Q_f leads to a voltage V_f across the feedback capacitor with a corresponding preamplifier output voltage

$$V_{out} = V_f = -\frac{Q_i}{C_f} \ . \tag{5.2}$$

The amplifier gain is thus determined by the feedback capacitor, an easily controlled component.

The output of a charge-sensitive preamplifier is a voltage signal with a short rise time and a sharp peak that is proportional in amplitude to the quantity of integrated charge. Therefore, the amplitude of the output signal is representative of the initial energy deposited in the detector by the detected radiation. A real charge-sensitive preamplifier extracts a small signal (order of fC or pC) from a strip of the detector, provided that the input signal is short in duration compared to the preamplifier decay time-constant $R_f C_f$, the output voltage signal will have an amplitude proportional to the charge integrated on the feedback capacitor. If the input signal is significantly shorter than the preamplifier decay time, this ensures that all of the charge at the preamplifier input is integrated onto the feedback capacitor before it discharges.

The R^{3}B ASIC has a preamplifier with a feedback capacitance of $C_f = 1.41$ pF. The inverting input of the preamplifier is connected to a single strip of the detector and a programmable reference voltage V_{PRE} is applied to the non-inverting input. When operated in electron (hole) mode, the output of the preamplifier is positive (negative) going and the reference voltage V_{PRE} is set to 0.7 V (2.3 V). The preamplifier has a programmable reset switch which is programmed by the channel control logic. The preamplifier reset is typically 2 μs in duration and the time at which the reset occurs can be programmed within the range 2-17 μs after the signal's rising edge. The inclusion of a leakage compensation circuit, connected in negative feedback across the preamplifier, allows the ASIC to function with leakage currents of up to 100 nA.

The resultant voltage signal from the preamplifier output is passed to a shaper as well as a gain amplifier so that the pulse can be further processed to obtain amplitude and time information.

5.3 Test Pulse Injection

The input signal to the preamplifier can be accurately reproduced by a voltage test pulse with a fast rising edge. The R^{3}B ASIC is equipped with a test pulse injection system where a well controlled quantity of charge can be injected into a channel via a test capacitor $C_T = 2.9$ pF in series with the input. Figure 5.5 shows a possible circuit digram for injecting test pulses into the inverting input of a preamplifier. A voltage step of amplitude V_{test} charges up the test capacitor and results in a charge Q_i at the input of the preamplifier.

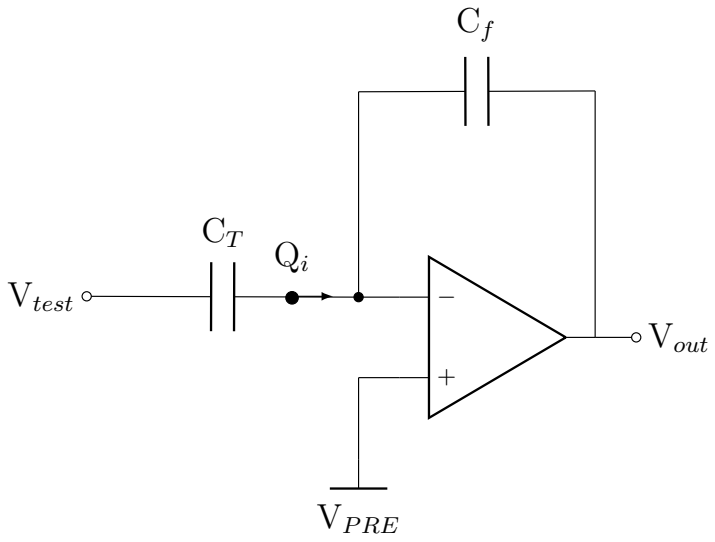


Figure 5.5: A circuit diagram outlining the principles of test pulse injection by applying a voltage step of amplitude V_{test} to a capacitor C_T.

An ideal operational-amplifier is assumed to experience no time delay for capacitor charging and discharging and thus does not result in any alteration of the time profile of the input pulse. A real preamplifier typically has an associated time constant resulting in a rise time for the input signal of the order of tens of ns. All calculations herein refer to an ideal operational amplifier system.

The result of injecting a step voltage of amplitude $V_{test} = 1.00\ V$ into an ideal preamplifier with $C_f = 1.41$ pF is shown in Figure 5.6. The resultant charge at the preamplifier input due to a 1.00 V test pulse is given by

$$Q_i = C_T V_{test} = 2.90 \times 10^{-12} \times 1.00 = 2.90 \text{ pC} . \tag{5.3}$$

As the charge collects on the feedback capacitor, the voltage difference V_f across the feedback capacitor increases. All of the injected charge is integrated on to the feedback capacitance ($Q_i = Q_f$) resulting in a preamplifier output with a maximum voltage of

$$V_{out} = -\frac{Q_i}{C_f} = -\frac{2.90 \times 10^{-12}}{1.41 \times 10^{-12}} = -2.06\ V\ . \tag{5.4}$$

The resultant amplitude of the output pulse from the preamplifier V_{out} is in proportion to the quantity of test charge seen at the preamplifier input and the preamplifier gain for an injected test pulse is given by

$$A = \frac{C_T}{C_f} = 2.06\ . \tag{5.5}$$

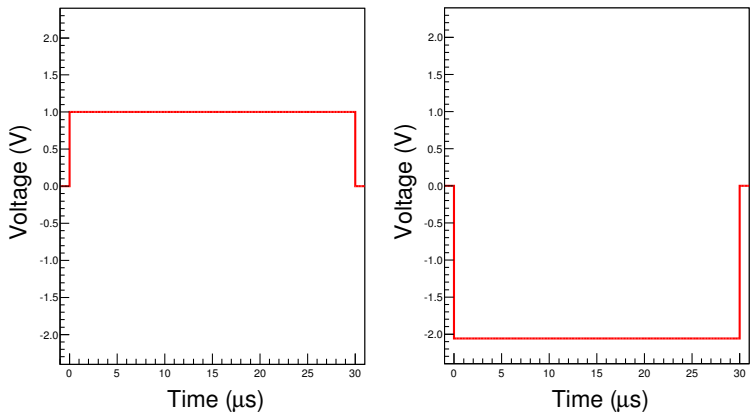


Figure 5.6: A step pulse injected into a test capacitor at t = 0 μs is shown on the left. The response of an ideal preamplifier to the step voltage input is shown on the right. The amplification is given by the ratio of the feedback capacitance to the test capacitance.

Every channel of the R^{3}B ASIC is equipped with a test pulse injection circuit at the preamplifier input. Figure 5.7 shows a diagram of the test pulse circuitry and the preamplifier for one channel of the ASIC. The amplitude of the test pulse is programmed via two 8-bit numbers (0-255 decimal) that select the values of $VCal_{low}$ and $VCal_{high}$. Prior to being injected into a preamplifier, the step pulse is passed to the calibrate block, which is programmed with voltages determined by $VCal_{low}$ and $VCal_{high}$. The voltage pulse $VCal$ leaving the calibrate block will have a positive polarity if the chip is in hole mode and negative if the chip is in electron mode. The magnitude of $VCal$ has 255 possible programmable values ranging from 0-2 V.

Therefore the smallest test pulse amplitude is given by

$$V_{test} = \frac{2}{255} = 7.8 \text{ mV} \ . \tag{5.6}$$

The amplitude of an injected test pulse is given by

$$V_{test} = 7.8 \text{ mV} \times VCal \ , \tag{5.7}$$

where $VCal$ is a digital number (DN), the value of which is given by

$$VCal = VCal_{high} - VCal_{low} \ . \tag{5.8}$$

The test pulse charges the test capacitor, which results in a charge Q_i that is integrated onto the preamplifier's feedback capacitance. The quantity of charge seen at the preamplifier input is proportional to the amplitude of the voltage test pulse. The test pulse amplitude (and charge Q_i) can be represented in units of electronvolts according to

$$E_{test}(\text{eV}) = \frac{C_T V_{test}}{e} \varepsilon_{pair} \ , \tag{5.9}$$

where e is the charge of an electron, and ε_{pair} is the electron-hole pair creation energy in silicon (3.6 eV). This relationship will be adopted for converting measurements of charge to units of eV in Chapter 6. Equation 5.3 and equation 5.4 confirm that the smallest programmable test pulse amplitude of 7.8 mV equates to a 509 keV signal and a 1 V test pulse equates to 65.250 MeV, which results in a preamplifier ouput voltage of 2.06 V. Therefore the calculated ideal preamplifier gain for test pulse injection can be quoted as 31.57 mV/MeV.

5.4 Timing Measurement

The R^{3}B ASIC utilises a fast signal path for timing measurements. Timing measurements are obtained by measuring the arrival time of the fast leading edge of the preamplifier output. This is achieved by passing the preamplifier output signal directly to the input of a $\times$10 gain amplifier and avoiding the shaper which causes significant timing delays. The $\times$10 gain amplifier, like the preamplifier, consists of an operational amplifier with a differential input and a feedback capacitance. The $\times$10 gain amplifier has an input capacitance of $C_i = 1.1$ pF and a feedback capacitance of $C_f = 110$ fF, resulting in a gain of $A = 10$. A circuit diagram of a $\times$10 gain

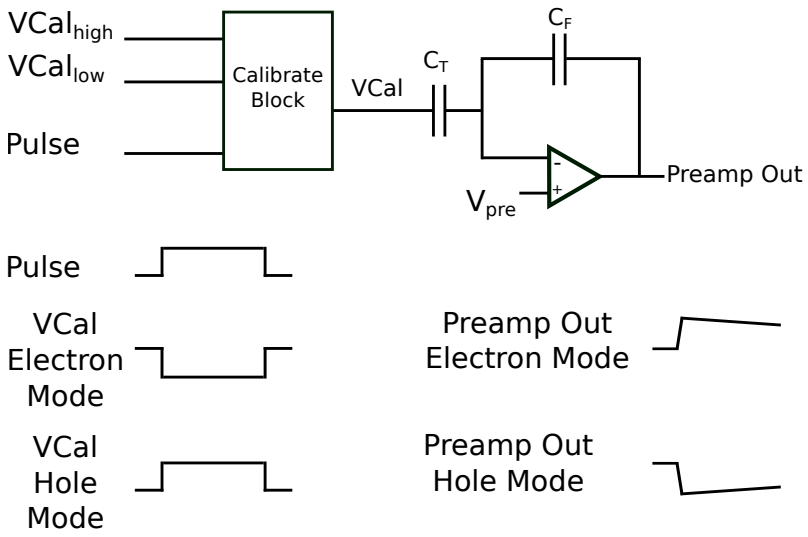


Figure 5.7: A schematic of the R^{3}B ASIC test pulse injection circuitry for electron and hole mode. The programmable registers $VCal_{high}$ and $VCal_{low}$ determine the amplitude of the test pulse $VCal$ which charges the test capacitance C_T.

amplifier is shown in Figure 5.8. For timing measurements, the preamplifier output signal forms the input the voltage signal V_{in} to the $\times$10 gain amplifier. The output signal of the $\times$10 gain amplifier is then passed to a fast comparator referred to as the time comparator.

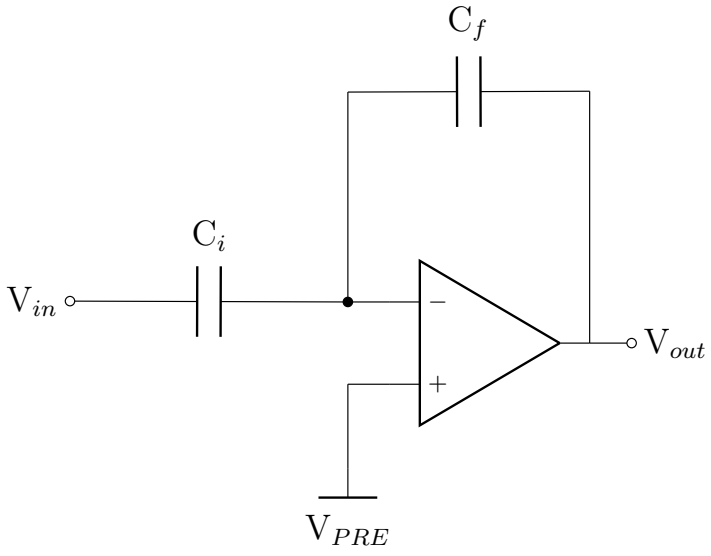


Figure 5.8: A circuit diagram for a $\times$10 gain amplifier with input capacitance C_i and a feedback capacitance C_f. The gain is determined by the ratio of the two capacitances such that C_i is ten times greater than C_f.

5.4.1 Comparator

A comparator is an electronic circuit that utilises the two inputs of an operational amplifier to compare two analogue voltage signals and generate a corresponding output signal depending on which of the two input signals is larger. Comparators are commonly used in the front-end electronics of detector systems to reject uninteresting signals and select only interesting pulses for further processing. The basic structure of a comparator, utilising an operational amplifier, is outlined in Figure 5.9. The non-inverting input of the amplifier is connected to a reference voltage V_{Tth} and the inverting input is connected to an input signal V_{in}. The circuit amplifies the difference between V_{in} and V_{Tth} and outputs the difference as

$$V_{out} = A(V_{in} - V_{Tth}) \ . \tag{5.10}$$

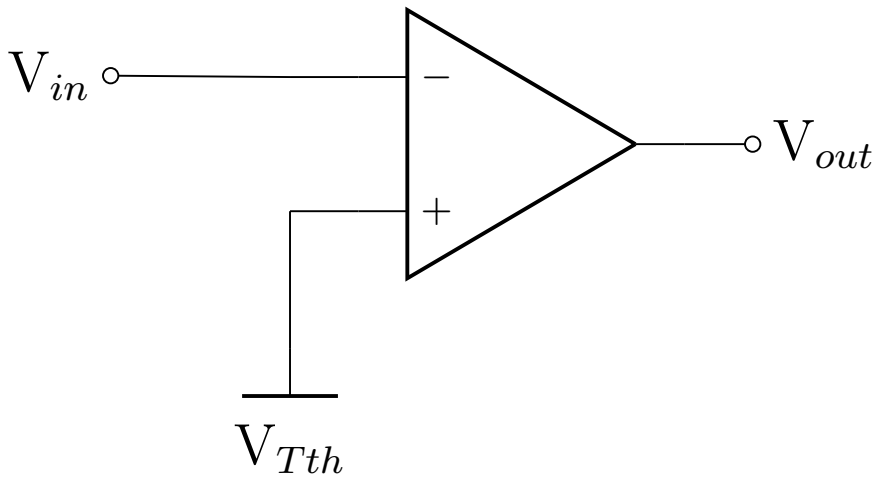


Figure 5.9: An operational amplifier configured for use as a comparator which outputs either a high or low signal. An input signal V_{in} is compared to a programmable threshold voltage V_{Tth} and the polarity of the output V_{out} changes depending on which signal is larger.

If V_{in} is greater than V_{Tth} then V_{out} is positive and alternatively V_{out} is negative if V_{Tth} is greater than V_{in}. In this configuration the amplifier has no negative feedback circuit. This results in a very high open-loop gain that causes the output of the amplifier to saturate at the amplifier's positive bias or negative bias voltage. This results in the output of the comparator being either a logical high or logical low, as values between these limits are not possible. Consequently, the comparator is

a useful device for taking two analogue signals at its input and outputing either a yes or no signal depending on which is larger. The comparator thereby has useful applications concerning threshold detection when a fixed threshold voltage is applied to one of the input terminals. If the signal at the inverting input V_{in} exceeds the threshold voltage V_{Tth} then the output signal will be a logical high and for input signals less than V_{Tth}, the comparator output will be a logical low.

5.4.2 Timestamp

The R^{3}B ASIC makes use of a comparator's threshold capabilities to generate a timestamp value for each hit. A timestamp is a digital number that is generated every time the comparator output is a logical high, also known as when the comparator fires. The fast rising edge of the preamplifier signal is passed to the comparator (via the $\times$10 gain amplifier) and a programmable threshold voltage is applied to the comparator's non-inverting input. When a signal from the $\times$10 gain amplifier exceeds the threshold, the output of the comparator fires. When the comparator fires, the logical high signal is passed to the timestamp counter which then prompts the generation of a 15-bit number depending on the 200 MHz clock (a 100 MHz clock may be used instead). The 15-bit timestamp is representative of the time at which a hit occurs.

If the signal from the preamplifier is lower than the threshold, the output of the comparator remains low and no timestamp is generated. The 15-bit timestamp thus represents the time of the hit with 5 ns resolution (10 ns if using 100 MHz clock). The wrapping time of the timestamp clock is 163,840 ns (or 3,276,780 ns for a 100 MHz clock). An additional timestamp value, generated from a second timestamp counter, is later included which extends the timestamp to 64-bit so that hits from a broader time window can be distinguished.

The timestamp is passed to the channel control logic before ultimately being passed to the data buffer where it is stored along with the associated energy measurement.

5.5 Energy Measurement

Energy measurements are obtained by firstly shaping the preamplifier output pulse and then sampling the maximum pulse height. The maximum amplitude of the shaper output is stored by a peak-hold circuit which is then passed to a 12-bit

ADC (Analogue to Digital Converter) whereby a digital number is obtained that represents the pulse height.

5.5.1 Pulse Shaping

A voltage signal from a preamplifier can be filtered by a CR-RC shaper network to improve the signal-to-noise ratio and transform a sharp peak of the detector pulse to a broader peak. Shaping a pulse can also remove the long decay tail produced by some preamplifiers, which can reduce dead time due to signal processing. The shaper is comprised of a differential amplifier with a resistor and capacitor in series with the input, as well as a resistor and capacitor in negative feedback across the amplifier. Such a shaping configuration is shown in Figure 5.10, which is the basic assembly for a CR-RC shaper.

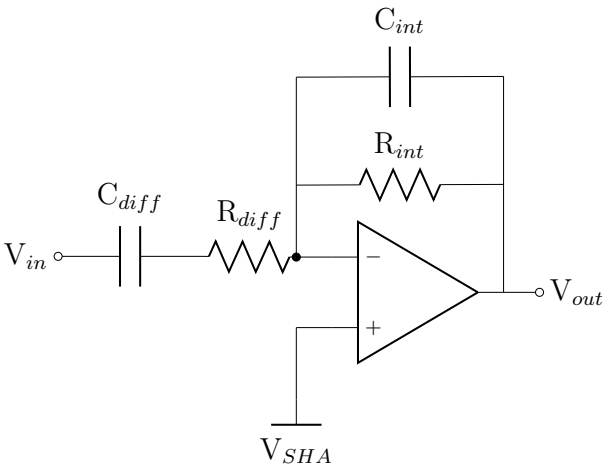
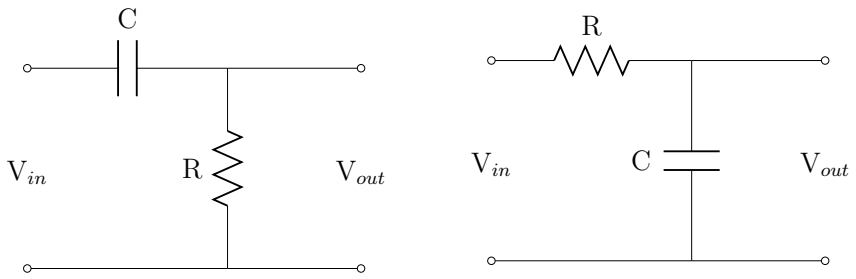


Figure 5.10: An example of a typical CR-RC shaper circuit utilising a differential amplifier. The differentiator stage is at the amplifier input (left) and the integrator stage is in negative feedback. A reference voltage V_{SHA} is applied to the amplifier's non-inverting input.

The capacitor and resistor in series with the input is known as the differentiator network. The differentiator allows the fast rising edge of a pulse to pass through unaltered but then rapidly restores the signal to the baseline to prevent the possibility of pulse pile-up occurring. The duration of the shaped signal's tail is dependent upon the differentiator time-constant τ_{diff}. The capacitor and resistor in negative feedback is known as the integrator network. This network integrates the input pulse's fast rising edge on to a capacitance C_{int} to produce a more gradual rising

edge. The result of passing a preamplifier output through a differentiator followed by an integrator is a pulse with a longer rise time and a decay tail resulting in a well rounded peak with a shortened pulse duration.

Pulse shaping is a compromise between obtaining complete information and minimising interference from noise and overlapping pulses. Detecting the entire duration of the preamplifier pulse can take a long time resulting in one pulse arriving before the previous pulse has been fully processed (pulse pile-up). This means the system is not restored to its baseline before the arrival of the next pulse which distorts the height measured for the next pulse. The dead-time of a detector refers to the time immediately following an intial signal during which the detector is unable to process another signal. For some systems, the dead-time may be reduced if the long decay tail of the preamplifier output pulse is shortened. As well as a long tail, the preamplifier output pulse has a very fast rising edge with a very sharp peak. In order to easily measure the maximum amplitude of the pulse it is beneficial to form a pulse with a more gradual peak. A voltage pulse can be shaped in different ways by CR (differentiator) and RC (integrator) networks, where the time-constant $\tau = RC$ plays a critical role. If R is in ohms and C is in farads, τ has units of seconds.



(a) CR differentiator. (b) RC integrator.

Figure 5.11: Differentiator and integrator pulse processing circuits.

CR Differentiator

A differentiator, also known as a high pass filter, consists of a capacitor connected across a resistor so that the capacitor discharges through the resistor (see Figure 5.11a). A differentiator allows the passage of high frequencies whilst inhibiting low frequencies and may be referred to as a high pass filter. If an initial step voltage

V_{in} charges the capacitor, the output voltage V_{out} due to the capacitor discharging through the resistor is given by

$$V_{out} = V_{in}\ e^{-\frac{t}{RC}}\ , \tag{5.11}$$

where t is time. When the differentiator time-constant $\tau_{diff} = R_{diff}C_{diff}$ is long in comparison to the pulse duration T ($T \ll RC$), the differentiator yields an output that is equivalent in amplitude to the input

$$V_{out} = V_{in}\ , \tag{5.12}$$

such that the fast rising edge of a pulse passes through unaltered. However, if the differentiator time-constant is short in comparison to the pulse duration ($T \gg RC$); the network will differentiate the pulse such that $V_{out} = 0$ for large values of T, which results in a differentiated tail.

The consequence of this is that the differentiator network will allow the fast rising edge of a preamplifier pulse to pass through unaltered whilst the long tail from the preamplifier will be differentiated thereby shortening the pulse whilst preserving the rising edge. The result of passing a step pulse (fast rising edge) to a differentiator network is shown in Figure 5.12 for different time-constants.

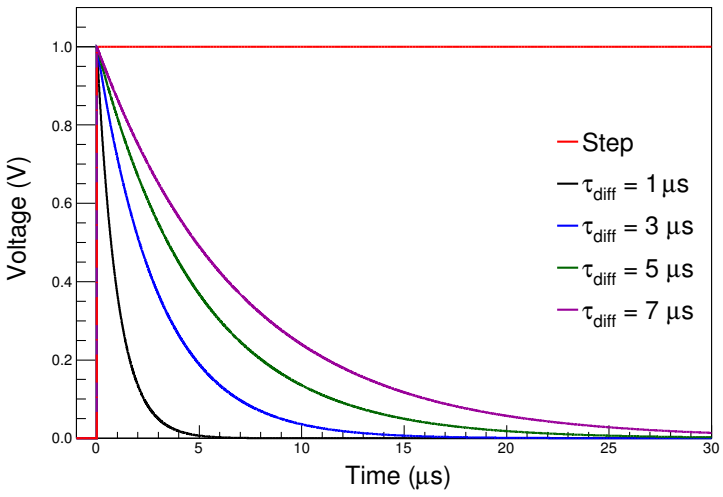


Figure 5.12: The response of a differentiator to a step input of amplitude 1.0 V for different differentiator time-constants τ_{diff}.

RC Integrator

An integrator network consists of a capacitor that is charged by applying a voltage to a resistor (see Figure 5.11b). An integrator allows the propagation of low frequencies whilst restricting the flow of high frequencies and is often referred to as a low pass filter. If an initial step voltage V_{in} is applied to the resistor, the output voltage V_{out} as the capacitor charges is given by

$$V_{out} = V_{in}(1 - e^{-\frac{t}{RC}}) \ . \tag{5.13}$$

For the case where the integrator time-constant $\tau_{int} = R_{int}C_{int}$ is very large relative to the pulse duration ($T \ll RC$); the pulse is integrated. If the integrator time-constant is short compared to the pulse duration ($T \gg RC$); the conditions for integration are not met and the waveform passes through with little alteration so that

$$V_{out} = V_{in} \ . \tag{5.14}$$

An integrator network will integrate the fast rising edge of a preamplifier output whilst allowing the long tail to pass through unaltered. The result of passing a step pulse (fast rising edge) to an integrator is shown in Figure 5.13 for different integrator time-constants τ_{int}.

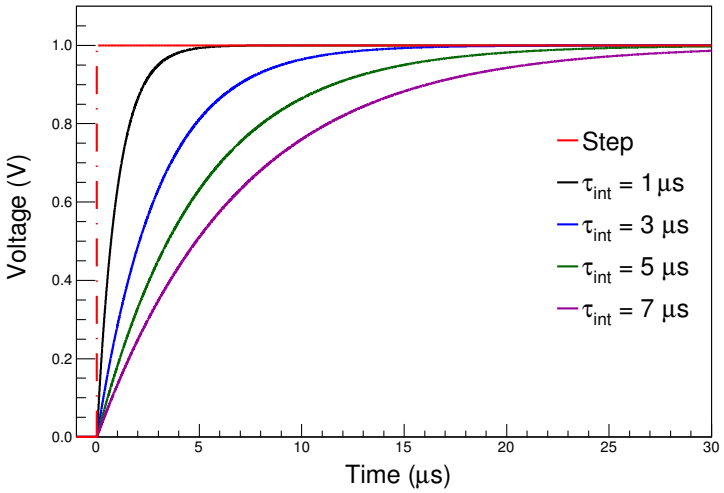


Figure 5.13: The response of an integrator to a step input of amplitude 1.0 V for different integrator time-constants τ_{int}.

CR-RC Shaping

The output pulse from a lone differentiator or integrator is not attractive as the maximum pulse amplitude is only maintained for a brief period of time, which is not conducive to easy pulse-height sampling. A stage of CR differentiation followed by an RC integration step results in a shaped pulse with a rounded peak for which the maximum amplitude can be more easily sampled. The inclusion of an operational amplifier allows both networks to operate without influencing each other thereby allowing filtering of high frequency and low frequency noise. The ouput response V_{out} of the combined CR-RC network to a step-voltage input of amplitude V_{in} is given by

$$V_{out} = -\frac{C_{diff}}{C_{int}} \cdot V_{in} \cdot \frac{\tau_{diff}}{\tau_{diff} - \tau_{int}} [e^{-\frac{t}{\tau_{diff}}} - e^{-\frac{t}{\tau_{int}}}] \ , \tag{5.15}$$

where τ_{int} and τ_{diff} represent the integrator and differentiator time-constants and t is time [21]. The shape of the output signal will vary for different combinations of τ_{diff} and τ_{int}. It is not uncommon for components to perform CR-RC shaping with equal time-constants for the differentiator and integrator. For the case where $\tau_{diff} = \tau_{int} = \tau$ the previous equation is indeterminant and the solution is given by

$$V_{out} = -\frac{C_{diff}}{C_{int}} \cdot V_{in} \cdot \frac{t}{\tau} e^{-\frac{t}{\tau}} \ . \tag{5.16}$$

When $\tau_{diff} = \tau_{int}$, the output from the shaper is a pulse with a rounded peak at $t = \tau_{peak}$, where $t = 0$ is the time at which the shaper output starts to rise. Therefore the peaking time τ_{peak} has the same value as the shaping time-constant τ, when the integrator and differentiator time-constants are the same.

The choice of shaping time-constant is a complex balance between pulse pile-up and signal-to-noise. It is advantageous to keep the differentiator time-constant short to allow the shaped waveform to return to the baseline quickly and reduce the system dead time. Figure 5.12 demonstrates how the value of the differentiator time-constant can be selected to significantly shorten or lengthen the duration of the shaped waveform. The rise time of the pulse can be controlled by altering the integrator time-constant, as shown in Figure 5.13, where a larger integrator time-constant results in a longer rise time.

As well as the pulse's time profile, pulse shaping also affects both the total noise and the peak signal amplitude at the shaper output. Firstly, there are two main sources of noise to consider, parallel noise and series noise. Parallel noise is of lower frequency than series noise, therefore a high pass filter (differentiator) can

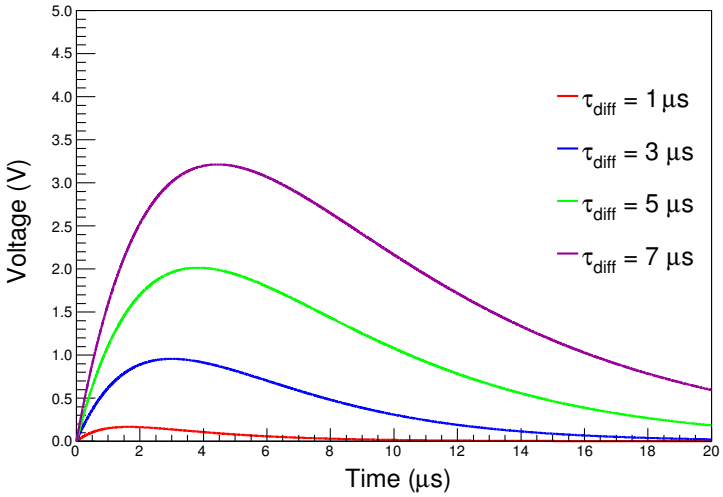


Figure 5.14: The calculated output of a shaper with an integrator time-constant of 3 μs and variable differentiator time-constants for a step voltage input of amplitude 1.0 V. A larger differentiator time-constant results in a larger signal amplitude. The differentiator time-constant has been altered using a fixed resistance and changing the capacitance.

remove low frequency parallel noise and a low pass filter (integrator) can block the high frequency series noise. The differentiator properties control the lower cut-off frequency and the integrator properties control the upper cut-off frequency [39]. Increasing the differentiator time-constant will decrease the lower cut-off frequency and increase the parallel noise at the shaper output. Increasing the integrator time-constant will decrease the upper cut-off frequency and decrease the total series noise at the shaper output. The bandwidth of the CR-RC shaper is thus minimised by adopting a smaller differentiator time-constant and a larger value of integrator time-constant.

The signal amplitude is also influenced by the choice of differentiatior and integrator time-constants. Figure 5.14 and Figure 5.15 show the dependence of the pulse amplitude on the differentiator and integrator time-constants, respectively. The maximum signal amplitude is thus obtained by having a large differentiator time-constant and a small integrator time-constant. The noise spectra tends to have a greater frequency bandwidth than the signal and so the signal-to-noise ratio can be optimised by tailoring the frequency response of the shaper network. For a system where the noise follows a Gaussian distribution; the noise can be quantified by repeatedly measuring a signal of constant amplitude. In a system with no noise such a measurement would return the same amplitude every time. If a constant signal

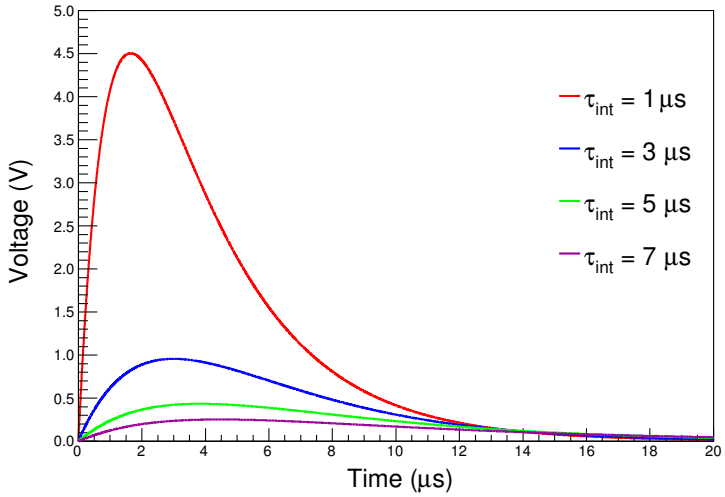


Figure 5.15: The calculated output of a shaper with a differentiator time-constant of 3 μs and variable integrator time-constants for a step voltage input of amplitude 1.0 V. A smaller integrator time-constant results in a larger signal amplitude. The integrator time-constant has been altered using a fixed resistance and changing the capacitance.

is superimposed on a noisy baseline, the repeated measurement will return a Gaussian distribution for the signal amplitude which has a full-width-at-half-maximum (FWHM) that is related to the rms noise level σ by

$$\text{FWHM} = 2.35\sigma \ . \tag{5.17}$$

A choice of shaping time-constant is ultimately decided upon depending on whether the key requirement is rate capability or signal-to-noise ratio. A short shaping time-constant is used for high rate capabilities and a long shaping time-constant is ideal for achieving a good signal-to-noise ratio. The need to limit the pulse duration, requires τ to be small, which decreases the noise at the shaper output but more importantly decreases the pulse amplitude. If dead-time is not an issue then a larger value for τ_{diff} can be used resulting in a longer pulse with a larger peak amplitude and the resultant increase in noise at the shaper output will be negated due to the large pulse amplitude leading to an improved signal-to-noise ratio.

R^{3}B ASIC Programmable Shaper

The R^{3}B ASIC has a shaper consisting of two resisitors and two programmable capacitor arrays to provide variable differentiation and integration of the signal. A circuit diagram for the R^{3}B programmable shaper is shown in Figure 5.16. The capacitor array at the input of the amplifier provides differentiation and the capacitor array in feedback integrates the signal. The differentiator and integrator time-constants can be altered by selecting different combinations of the programmable capacitor arrays whilst the resistance remains constant. Each capacitor has an associated switch which allows many different combinations of capacitors resulting in different time-constants. Altering the differentiator and integrator time-constants allows a programmable shaping time-constant with a peaking time of τ_{peak} = 0.5, 1.0, 1.5, 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0, 5.5, 6.0, 6.5, 7.0, 7.5 or 8.0 μs (see Table 5.2 for capacitor array configurations). A reference voltage V_{SHA} is applied to the inverting input of the differential amplifier.

Table 5.2: All possible programmable shaper capacitor and resistor configurations are shown. The ratio of C_{diff}/C_{int} is the same for all configurations such that shaper gain A_{sha} is the same for all peaking times.

τ_{peak} [μs]	C_{diff} [pF]	C_{int} [pF]	C_{diff}/C_{int}	τ_{diff} [μs]	τ_{int} [μs]	A_{sha}
0.5	1.3	0.5	2.6	0.4999	0.5000	0.96
1.0	2.6	1.0	2.6	0.9970	1.0000	0.96
1.5	3.9	1.5	2.6	1.4996	1.5000	0.96
2.0	5.2	2.0	2.6	1.9994	2.0000	0.96
2.5	6.5	2.5	2.6	2.4993	2.5000	0.96
3.0	7.8	3.0	2.6	2.9991	3.0000	0.96
3.5	9.1	3.5	2.6	3.4990	3.5000	0.96
4.0	10.4	4.0	2.6	3.9988	4.0000	0.96
4.5	11.7	4.5	2.6	4.4987	4.5000	0.96
5.0	13.0	5.0	2.6	4.9985	5.0000	0.96
5.5	14.3	5.5	2.6	5.4984	5.5000	0.96
6.0	15.6	6.0	2.6	5.9982	6.0000	0.96
6.5	16.9	6.5	2.6	6.4981	6.5000	0.96
7.0	18.2	7.0	2.6	6.9979	7.0000	0.96
7.5	19.5	7.5	2.6	7.4978	7.5000	0.96
8.0	20.8	8.0	2.6	7.9976	8.0000	0.96

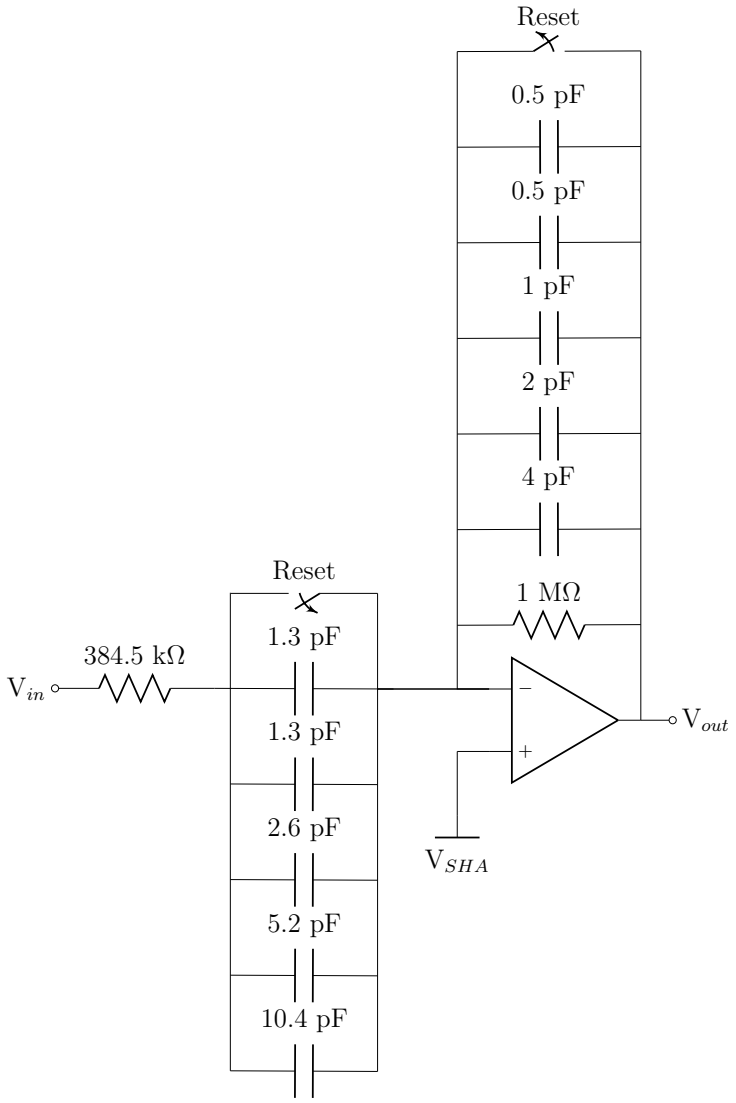


Figure 5.16: The R^{3}B ASIC's programmable CR-RC shaper network. The integration and differentiation time-constants can be programmed by selecting different combinations of the capacitor arrays. Two reset switches are controlled by the channel control logic.

For electron mode, a reference voltage $V_{SHA} = 2.4$ V is applied and the output signal is negative going. For hole mode, $V_{SHA} = 0.6$ V and the output signal is positive going. The shaper is equipped with two reset switches, which allow the shaper output to be restored to the baseline prior to the arrival of the next signal. By default, the shaper reset is 3 μs in duration and is only ever reset after the preamplifier is reset. The reset sequence ensures that no unwanted signals, which may arise during the preamplifier reset, are shaped and passed to the energy com-

parator thus protecting against possible false triggering of the comparator. Figure 5.17 shows the response of an ideal shaper, for a step voltage input, for the full range of possible shaping time-constants of the R^{3}B ASIC, according to equation 5.15 using the values outlined in Table 5.2. The maximum amplitude of the shaper pulse is the same for every time-constant.

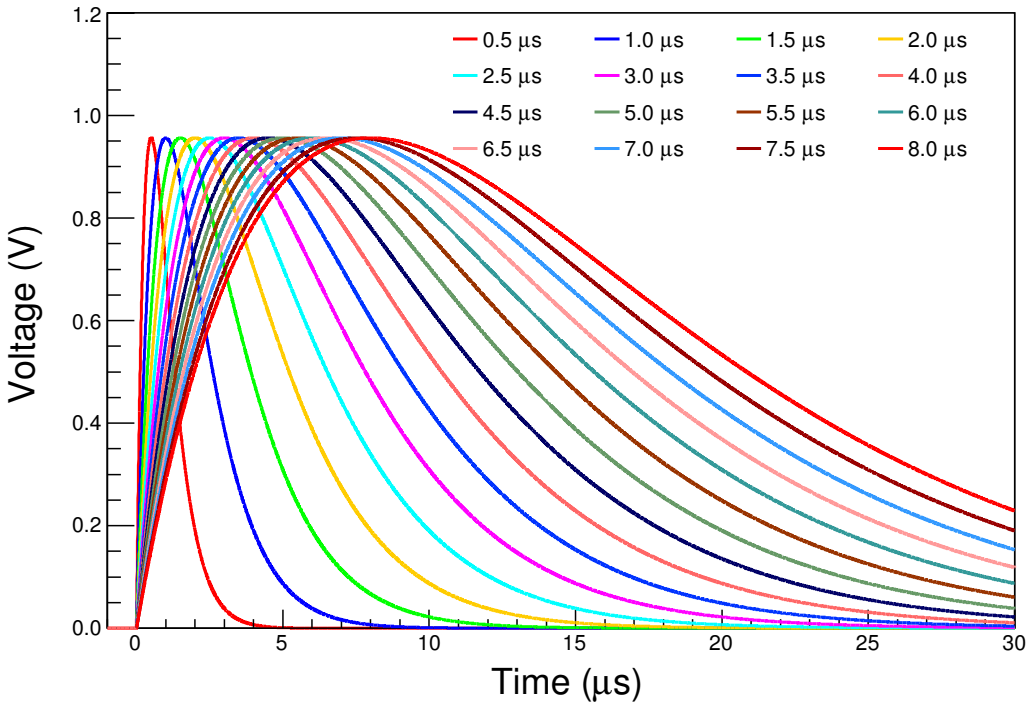


Figure 5.17: The response of the R^{3}B ASIC shaper for a step input of amplitude 1.0 V for all possible programmable shaping time-constants. The shaper gain is the same for all time-constants.

The ratio of the differentiator capacitance to integrator capacitance is proportional to the gain of the shaper. For every possible shaping time-constant, the R^{3}B shaper has a ratio of

$$\frac{C_{diff}}{C_{int}} = 2.6 \tag{5.18}$$

so that the gain A_{sha} of the front-end is independent of the shaping time-constant. If the value of C_{int} is kept constant, increasing the value of C_{diff} would result in greater amplification. Conversely, if C_{diff} is constant, increasing C_{int} would reduce the amplification. If the values of C_{int} and C_{diff} increase whilst the ratio remains constant, the pulse will peak at a later time and the maximum amplitude does not change.

Shaper Gain

The differentiator and integrator capacitor arrays have specifically selected capacitances such that the ratio should remain constant for all programmed shaping time-constants. Consider the example of a shaping time-constant of 8.0 μs which has the capacitances $C_{diff} = 20.80$ pF and $C_{int} = 8.00$ pF. The tolerances of the shaper capacitances are quoted as being $\pm$ 15%. The maximum shaper gain would be achieved for C_{diff} + 15% and C_{int} - 15%, conversely the minimum shaper gain is given by C_{diff} - 15% and C_{int} + 15%. In Figure 5.18, the difference in maximum pulse amplitude due to different shaper capacitances has been calculated using the ideal shaper equation (see equation 5.15). An initial step voltage input of $V_{test} = 0.1$ V was used at the preamplifier input, resulting in a 0.206 V amplitude step pulse at the shaper input. It has been deduced that the theoretical shaper gain A_{sha}, given by the maximum amplitude of the shaper output V_{shaout} divided by the maximum amplitude of the preamplifier output V_{preout}, for the exact capacitances is

$$A_{sha} = \frac{V_{shaout}}{V_{preout}} = \frac{V_{out}}{V_{in}} = \frac{C_{diff}}{C_{int}} \cdot \frac{\tau_{diff}}{\tau_{diff} - \tau_{int}} [e^{-\frac{t}{\tau_{diff}}} - e^{-\frac{t}{\tau_{int}}}] = 0.96 \ . \qquad (5.19)$$

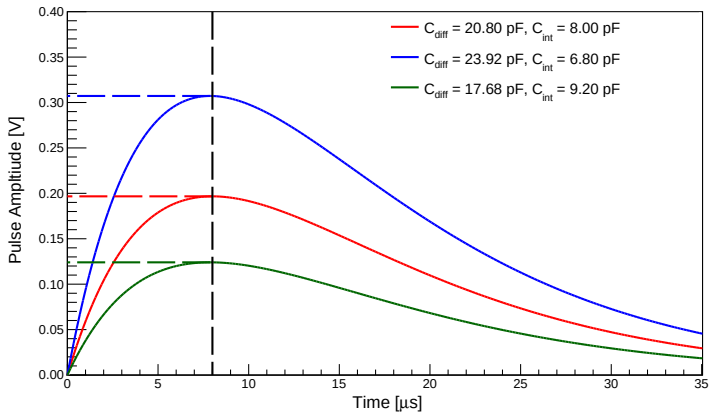


Figure 5.18: A 0.1 V step pulse at the preamplifier input results in a 0.206 V step pulse being passed from the preamplifier to the shaper input. The maximum amplitude of the shaped pulse varies if the values of the differentiator capacitance or integrator capacitance are changed by $\pm$ 15%.

The output signal from the shaper is then passed to a gain amplifier as well as a peak-hold circuit for further processing.

5.5.2 Peak Hold Circuit

The peak-hold circuit is an analogue device which samples the voltage at its input and holds the maximum value (peak) for a controlled period of time. The use of peak-detect-and-hold circuits is common in nuclear electronics pulse processing when digitisation of the entire waveform is unnecessary [50]. An example of a peak-hold circuit, for positive input signals only, using an operational amplifier and p-MOSFET is depicted in Figure 5.19. The input voltage V_{in} is connected to the amplifier's inverting input and the output of the amplifier is connected to the gate of a p-MOSFET with a voltage V_{dd} applied to the source. The non-inverting input of the amplifier is connected to the drain of the p-MOSFET as well as a hold capacitor C_{pkh}. In this configuration, the p-MOSFET can act as either a charging or switching element depending upon the magnitude of the input signal in relation to the hold voltage V_h across the hold capacitor, which is connected to the amplifier's non-inverting input.

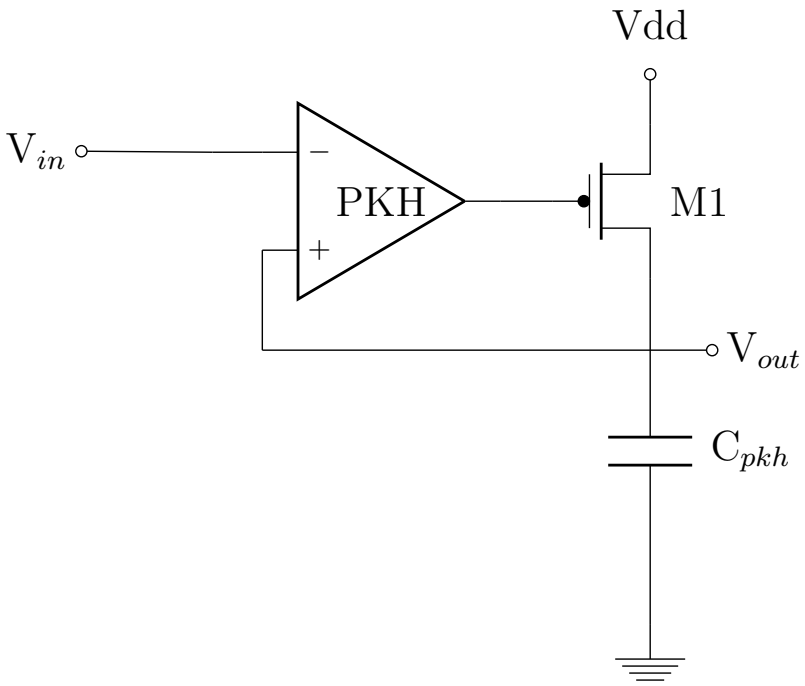


Figure 5.19: An example of a peak-hold circuit. The capacitor C_{pkh} stores the peak voltage corresponding to the maximum amplitude of an analogue input signal V_{in}.

When an input pulse arrives at the amplifier's inverting input, an error signal V_e

is established that is given by

$$V_e = V_h - V_{in} \ . \tag{5.20}$$

If the amplitude of the input signal is greater than that of the hold signal then the error signal will have a negative polarity which gives rise to a sudden negative transition of the gate voltage V_g at the amplifier output. A negative gate voltage switches on the p-MOSFET, causing a drain current I_d to flow that charges the hold capacitor. The presence of a feedback loop means that the gate voltage is constantly adjusted to produce a drain current which is dependent upon V_{in}. The drain current is given by

$$I_d = C\frac{d}{dt}V_{in} \ , \tag{5.21}$$

which subsequently charges up the hold capacitor. This leads to a setup where the voltage stored across the hold capacitor increases with the amplitude of V_{in}. The condition where

$$V_h = V_{in} \ , \tag{5.22}$$

is satisfied until V_{in} reaches its peak value V_{peak}. When $V_{in} = V_{peak}$ the time derivative of V_{in} in equation 5.21 is zero. Consequently the input signal is no longer greater in amplitude than the hold signal and the error signal becomes positive. This results in a sharp positive transition of the gate voltage which switches off the p-MOSFET. The falling edge of the shaper output, which is of smaller amplitude than the peak, will generate a positive gate voltage which prevents switching on of the p-MOSFET. The end result is a voltage V_h stored across the hold capacitor, that retains the peak value of the input signal, which can be passed for further analysis.

5.5.3 Energy Comparator

As well as the peak-hold circuit, the signal from the shaper output is also passed firstly to a $\times 10$ gain amplifier and then a comparator. This results in amplification of the signal prior to being compared to a user defined threshold voltage. The energy comparator operates via the same principles as the comparator used for timing measurements outlined in section 5.4. If the input signal is greater than the comparator's applied reference voltage, then the signal is deemed to be a hit. A hit occurs when the output of the comparator is high. A hit results in a signal being sent, via the channel readout logic, which samples the peak-hold circuit and passes the analogue voltage to the ADC. Any signal above the specified energy threshold

will also trigger the readout of any neighbouring channels. When a hit occurs in a channel, the readout timing logic for the channel is initiated (see section 5.6).

5.5.4 Analogue to Digital Conversion

The maximum voltage obtained by the peak-hold circuit is firstly passed to an analogue multiplexer. There is one analogue multiplexer per ASIC. The analogue multiplexer is controlled by the channel readout logic, which outputs the voltage from each hit channel, and its neighbouring channels, to a 12-bit successive approximation ADC. The ADC converts each analogue voltage to a 12-bit binary number which may be represented as a digital number from 0-4095. The limited number of digital output codes results in a quantisation process which introduces a minimum resolution. As the number of bits increases, the number of possible digital output codes increases and hence the analogue voltage range associated with the least significant bit (LSB) decreases. The least significant bit corresponds to the width of one ADC bin (step width) and represents the total number of divisions of the analogue input range. For the R^{3}B ASIC, the 12-bit ADC has an analogue signal input range of 2 V resulting in the following relation

$$1 \text{ LSB} = \text{ADC Bin Width} = \frac{2}{2^{12}} = 0.488 \text{ mV} . \tag{5.23}$$

A high reference voltage of $V_{refh} = 2.5$ V and a low reference voltage of $V_{refl} = 0.5$ V are applied to the ADC so that the ADC has a 2 V dynamic range.

The successive approximation ADC was chosen as it has a sampling frequency that is adequate for the ASIC readout. The ADC continuously runs at a rate of $1{\times}10^6$ samples/s and data is only written to the data buffer when the ADC output contains hit data (when the signal amplitude is greater than the reference threshold voltage set for the energy comparator). See section 5.7 for data format.

The main constituents of a successive approximation ADC are an analogue comparator, a digital-to-analogue converter (DAC) and a successive-approximation register (SAR). An N-bit successive approximation ADC requires an N-bit DAC. The R^{3}B ASIC has a 12-bit ADC with a DAC that allows a 12-bit binary number to be selected, for which the corresponding analogue voltage is compared to the input voltage (from the peak-hold circuit) at the comparator. The peak-hold voltage and the DAC voltage are passed to the two inputs of the comparator whereby the output of the comparator will attain either a logical high or logical low depending

on whether the DAC voltage is smaller or greater than the peak-hold voltage. The analogue signal, passed from the DAC to the comparator, can be varied by selecting different digital numbers using the successive approximation register.

When all 12-bits of the DAC have a value of 1, the DAC output voltage is 2.5 V. A successive-approximation ADC begins by turning on the most significant bit (MSB), which sets the DAC output voltage to be half of the maximum possible value. Turning on only the MSB of a 12-bit ADC equates to a binary number of 1 followed by eleven 0s. The voltage stored on the hold capacitor of the peak-hold circuit is passed to one of the comparator inputs where it is compared with the DAC voltage input. If the hold voltage V_{in} is greater than the DAC output, the successive-approximation register keeps the MSB on (1). For a hold voltage which is less than the DAC output, the successive-approximation register turns off the MSB (0). This process is repeated for the next MSB, which equates to a quarter of the maximum DAC output, and for every bit of the register until the least significant bit (LSB). By trialling different DAC outputs from MSB to LSB, an approximation of the input voltage is obtained which is presented as a binary number.

A 12-bit successive approximation ADC typically requires four clock cycles for sampling and twelve clock cycles for conversion. The R^{3}B ADC has a clock frequency which is not fixed so as to allow greater settling time during conversion of the most significant bits, but the total time taken to convert one sample is always 1 μs. A higher resolution ADC (more bits) requires a longer time for the DAC to settle and therefore the total time taken for sampling and conversion is longer.

5.5.5 Front-End Gain

The signal at the ADC input is obtained from the peak-hold circuit which is connected to the shaper network and finally the preamplifier. The theoretical preamplifier gain is $A = 2.06$ and the shaper gain is $A_{sha} = 0.96$, and assuming that the peak-hold circuit has an associated gain of 1. The voltage at the ADC input can easily be related to the charge at the preamplifier input using values of A, A_{sha} and equation 5.2. Therefore the ADC value for a given input charge can be calculated, using ideal equations, and the theoretical front-end gain can be determined.

The calculations used in Figure 5.18 are repeated for all possible test pulse amplitudes within the 0-50 MeV dynamic range. The result of plotting the theoretical ADC, corresponding to the shaped maximum pulse amplitude (according to equation 5.23), against injected test pulse amplitude is displayed in Figure 5.20. The

calculation using exact capacitances yields a calculated slope of

$$\text{Front-End Gain} = 0.06174 \text{ ADC/keV} . \tag{5.24}$$

The parameters and the results of the three configurations are summarised in Table 5.3 where the dependence of slope on the shaper capacitances is evidently clear. It is therefore possible to measure a difference in the front-end linearity when comparing data taken with different shaping time-constants.

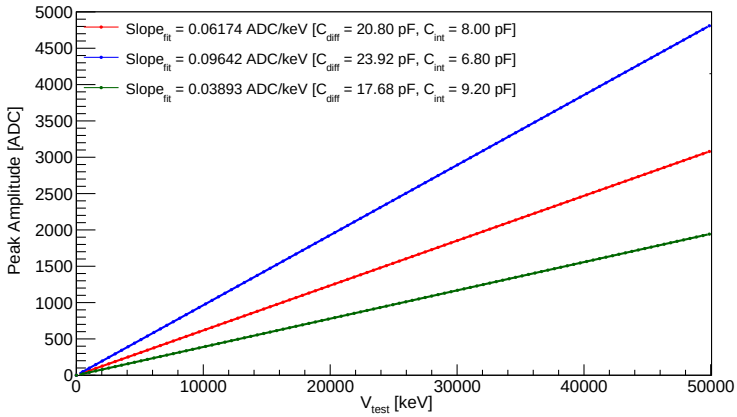


Figure 5.20: The ideal slope (gain) is shown in red using exact capacitances. The slope can vary if the values of the differentiator capacitance or integrator capacitance are changed.

Table 5.3: The shaper capacitances for an 8 μs shaping time-constant are shown along with $\pm$ 15% tolerance limits. The calculated shaper gain and theoretical slope (front-end gain) is shown for each configuration. The exact capacitance values of C_{diff} = 20.80 pF and C_{int} = 8.00 pF, yield a shaper gain of 0.96.

C_{diff} [pF]	C_{int} [pF]	C_{diff}/C_{int}	A_{sha}	Slope [ADC/keV]	Peaking-Time [μs]
20.80	8.00	2.60	0.96	0.06174	7.9988
23.92	6.80	3.52	1.50	0.09642	7.8783
17.68	9.20	1.92	0.60	0.03893	7.8782

It has been shown that slight differences may occur in the front-end gain due to small changes in differentiator and integrator capacitances. Furthermore it has been deduced that the theoretical ADC bin width can be related to the preamplifier

input signal according to the following relationship

$$\text{Bin Width} = \frac{1}{0.06174} = 16.20 \text{ keV} \ . \tag{5.25}$$

This can be shown alternatively as, a 0.488 mV signal at the ADC input arises due to a 0.508 mV signal at the preamplifier output, and a 0.508 mV preamplifier output is generated by a test charge of 16.20 keV. Therefore, using ideal equations, the energy resolution of the ASIC is limited to 16.20 keV due to the ADC resolution.

5.6 Readout Timing Logic

The ASIC has a programmable input clock of either 100 or 200 MHz and data is read off each chip at a rate of 50 Mbits/s. A 1 MHz clock is generated from the input clock which controls the channel readout logic. The channel readout logic determines the sequence of signals which occur once a hit has been detected.

The signal at the preamplifier output is passed to two separate signal paths. Only the signal that is passed to the the energy comparator is able to trigger a hit and initialise the channel readout logic. The energy comparator output signal is high (comparator is fired), if the signal amplitude exceeds the programmed energy threshold *Eth*. The high output signal is passed to the channel control logic which then synchronises the hit with the ASIC's readout system on the next rising edge of the clock. All timing of the readout logic is referenced to this initial clock rising edge.

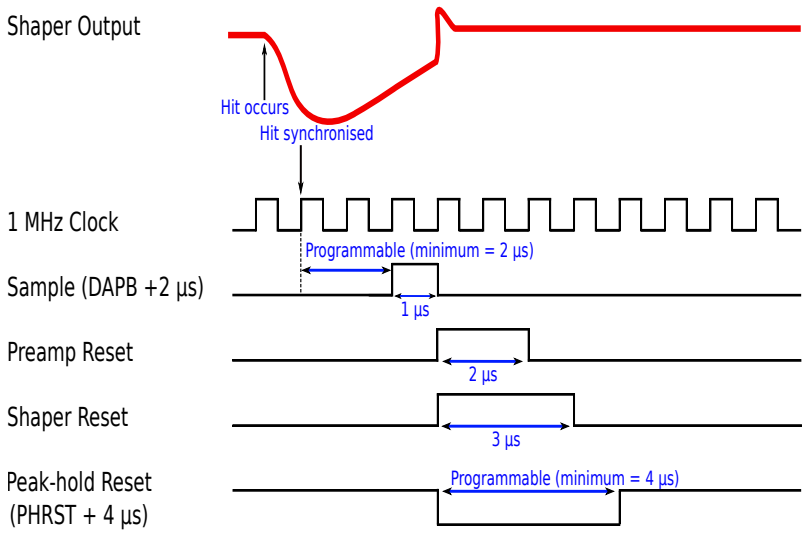


Figure 5.21: The channel readout logic timing of the R^{3}B ASIC.

The timing of the readout logic for a single channel is shown in Figure 5.21. The readout sequence can begin once the hit is synchronised with the 1 MHz clock of the channel readout logic. The channel readout logic first issues a signal which enables sampling of the peak-hold circuit to obtain the maximum amplitude of shaper output. The time from when the hit is synchronised to when the shaper output is sampled can be programmed. This ensures that a programmable value can be selected so that the peak-hold circuit is only ever sampled after the pulse has peaked (after the peaking time). The delay-after-peak-bit (DAPB) setting can be used to determine the time at which the signal is sampled. The minimum sampling time is two clock cycles (minimum sampling time = 2 μs) after the time at which the hit was synchronised. The maximum sampling time is 17 clock cycles (DAPB = 15 μs, maximum sampling time = 17 μs) after the hit was synchronised. The analogue voltage measured by the peak-hold circuit is passed to the analogue multiplexer. The analogue multiplexer receives the analogue amplitude data and cycles through all 128 channels at a rate of 1 MHz, reading out the data of only the hit channels. The analogue multiplexer passes the peak-hold voltage to the ADC whereby a 12-bit number is generated corresponding to the pulse amplitude. The channel control logic will then guarantee that the 12-bit ADC value is latched to the corresponding 15-bit timestamp value and channel address. The readout logic also generates a trigger signal of all 128 channels which can be transmitted off the chip as a 128-bit trigger pulse.

The readout logic can only be initiated by a logical-high energy comparator output. If both the energy comparator and time comparator outputs are high, a hit occurs where the timestamp is generated by the logical-high time comparator output. It is possible for the ASIC to process a signal where the time comparator does not fire but the energy comparator does. This situation is possible depending on the threshold settings of the energy and time comparators and the amplitude of the signal. Under these circumstances, the high output of the energy comparator is used to generate a timestamp. The channel readout logic will sample the timestamp counter to generate a 15-bit timestamp. A timestamp generated in this way (not using the time comparator) will not be as accurate as a timestamp produced via the timestamp comparator but an offline correction can be applied to account for the timing delays introduced due to the shaping process.

5.7 Data Format

Each ASIC has the ability to store up to 32 hits on chip by virtue of the 48-bit wide, 32 deep FIFO. Each hit is composed of 48 bits in total. A buffered hit consists of: 2 start bits (11), 10-bit chip address, 7-bit channel address, 15-bit timestamp, 12-bit ADC, 1-bit hit-bit,and 1 stop bit (0). The hit-bit has a value of 1 if both the energy and time comparators fired and a value of 0 if only the energy comparator fired. If the hit-bit has a value of 0, an offline correction will be applied to the timestamp value. Once the buffer is fully occupied, it is not possible to write any more data to the chip until the buffer is read out off the chip. If the data buffer becomes full, the chip will keep a count of the number of hits that have been blocked during this period.

Data packets from the data buffer of each chip are loaded into a data register which enables the data to be transmitted off the chip. The data packet is transmitted off chip with the 2 start bits first followed by the chip address, channel address, timestamp, ADC, hit-bit and finally the stop bit. A 50 MHz clock governs the data transfer rate. A total of 960 ns is required to transmit one data packet off chip.

5.8 Daisy Control

The readout of data off the ASIC and from ASIC to ASIC is based on a daisy chain control sequence, where four ASICs constitute one chain. It is not possible to drive a single lone ASIC. Figure 5.22 shows a schematic of a single chain of four ASICs. When constructing a detector, every fourth ASIC is connected to form a chain that is spread across the detector. Therefore, ASIC 1, 5, 9 and 13 will form a chain for an outer detector. The first ASIC (ASIC1) is the master chip which generates the 50 MHz clock used for transmitting data. The master chip always initiates the readout of the chain by receiving data valid signals (DAV) from other chips within the chain. If a DAV signal is generated, due to an event in any ASIC, the DAV signal is passed to the master chip. Upon receiving a DAV signal, the master transmits its own data (DataOut) as well as the 50 MHz readout clock to the neighbouring chip (ASIC5), which then passes its own data and the data from ASIC1 as well as the 50 MHz clock to ASIC9. Once a chip has finished sending a DataOut signal, it passes a read enable (REN) signal to the next chip in the chain. The REN signal transmitted by each chip remains high until the final chip in the chain has been read out and subsequently passed the REN signal to the master chip. When the

read enable signal reaches the final chip (slave), the last chip outputs the data to the internal buffer card and then sends the read enable signal back to the master chip. Upon receiving a REN signal from the last chip, the master transmits a REN signal to all the chips which resets the REN signal of every chip in the chain.

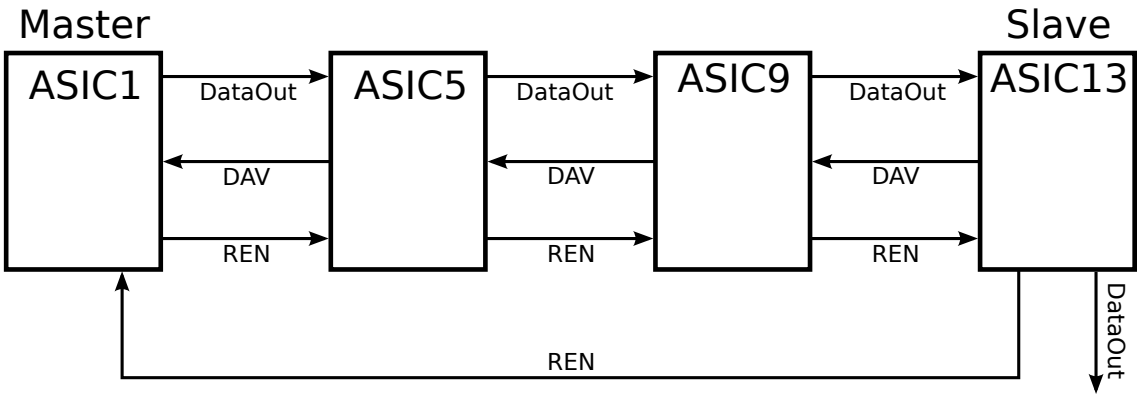


Figure 5.22: A schematic outlining the ASIC daisy chain structure.

Chapter 6

ASIC Version Two Functionality Testing

A range of tests have been carried out on the pre-production version of the R^3B ASIC (version two) to identify and test key operational properties. Calculations for the response of an ideal operational-amplifier, CR-RC shaper and ADC have also been included to fully understand the ASIC behaviour from a theoretical perspective.

The aim of the testing was to verify the ASIC specifications, characterise programmable parameters and reveal any issues which can be addressed for the final production version ASIC (version three). Tested parameters include; peaking time (τ_{peak}), sampling time (DAPB), peak-hold reset (PHRST), energy threshold (Eth) and timestamp threshold (Tth). All tests have been conducted using noise generated hits or the ASIC's test pulse injection system where the amplitude (V_{test}), time duration (T) and rate of the pulses are programmable. The ROOT data analysis framework has been used throughout the analysis where the value labelled RMS is the calculated standard deviation σ.

6.1 Test Setup

The test setup consists of four bare ASIC with no silicon sensor connected. Figure 6.1 shows a picture of the bare ASIC test board where the ASIC are glued to a PCB and housed in a light-tight casing. The digitised signals from the ASIC are passed off the ASIC to an internal buffer card (situated within vacuum for experimental setup) via a PCB. The internal buffer card is then connected to an external buffer card (outside of vacuum chamber for experimental setup) via a vacuum chamber connector.

Signals are then passed from the external buffer card to a Micro Telecommunications Computing Architecture (μ-TCA) crate [51] for further processing. A picture of the test setup is shown in Figure 6.2. All ASIC testing was carried out under standard temperature and pressure conditions. The buffer cards provide impedance matching and isolation of the data signals from the front-end whilst allowing control signals, clocks and analogue and digital supply voltages to be passed to the ASICs. The internal buffer card has a heat sink on the underside which will be connected the silicon tracker's vacuum chamber wall to aid heat dissipation.

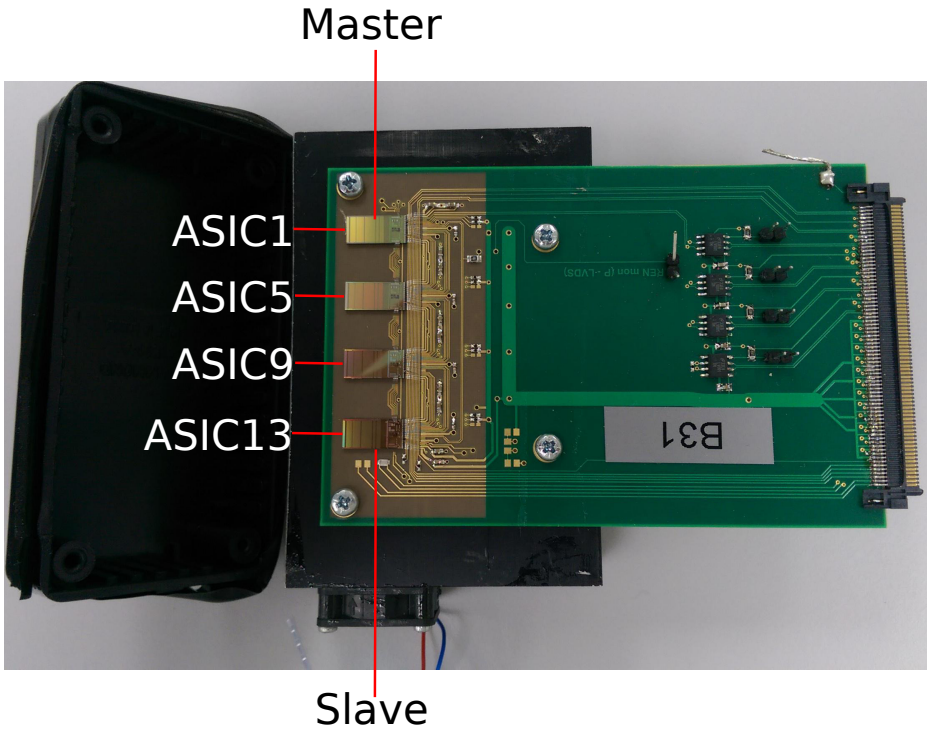


Figure 6.1: A photograph of the ASIC test board showing the four ASICs that form a single chain.

All testing was carried out by firstly applying a bias voltage (3.3 V) to the ASIC and then configuring the register settings for either hole mode or electron mode. The hole mode configuration is capable of processing positive going signals whereas the electron mode processes negative going signals. The default reference voltage that is applied to the preamplifier, shaper and $\times 10$ gain amplifiers is different depending on the mode for which the ASIC is configured. The test pulse injection is a voltage pulse with a rise time of approximately 25 ns that will be considered as a step function for ideal calculations. The test pulse parameters such as $VCal_{low}$, $VCal_{high}$ and number of pulses are all programmable.

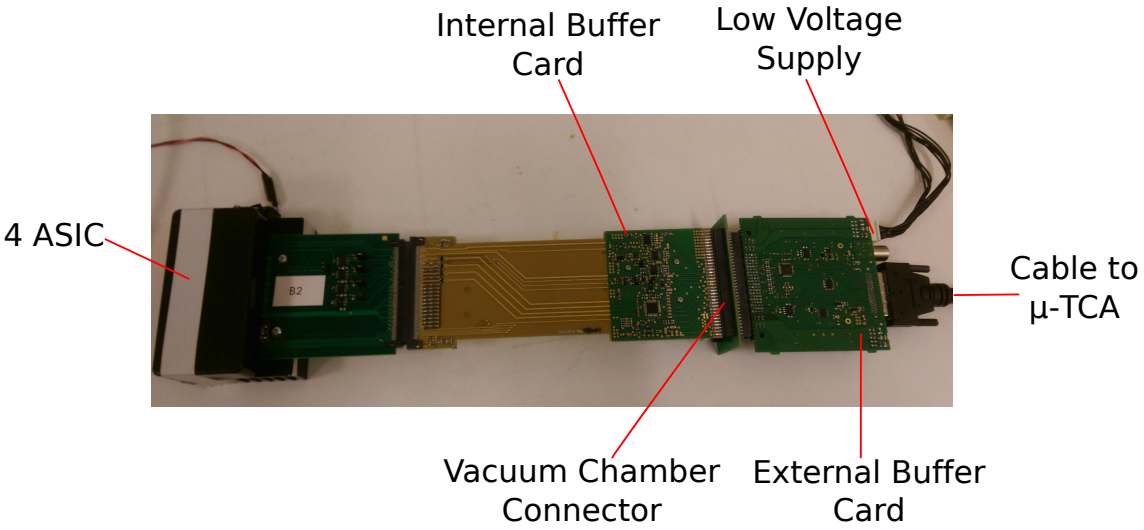


Figure 6.2: A photograph of the test setup used for testing of the bare ASIC.

Table 6.1: The default values of the ASIC registers and their functions.

Register	Function	Default (DN)	emode (V)	hmode (V)
0	page registers	-	-	-
1	e/h mode	176 (emode) 48 (hmode)	- -	- -
2	daisy chain, clock	92 (master) 44 (slave) 192 (other)	- - -	- - -
3	peak-hold-reset (PHRST)	16	-	-
4	τ_{peak}, (DAPB)	255	-	-
5	data packet readout	128	-	-
6	PCB address, readout buffer	-	-	-
7	blocked data count	-	-	-
10	preamp bias V_{PRE}	13	0.6	2.4
11	shaper bias V_{SHA}	243	2.4	0.6
12	$\times$10 gain amp bias V_{PRE1}	128	1.5	1.5
13	$\times$10 gain amp bias V_{SHA1}	128	1.5	1.5
14	timestamp threshold Tth	64	1.0	2.0
15	energy threshold Eth	192	2.0	1.0
16	test pulse high $VCal_{high}$	160	1.7	1.7
17	test pulse low $VCal_{low}$	96	1.2	1.2
18	low reference voltage V_{refl}	0	0.5	0.5
19	mid reference voltage V_{refm}	128	1.5	1.5
20	high reference voltage V_{refh}	255	2.5	2.5

The energy threshold, peaking time, delay-after-peak-bit and peak hold reset are all programmed using 8-bit global registers. In total the ASIC has 128 global

registers and four page registers. Global registers are applied collectively across all the channels of an ASIC whereas page registers can be specifically programmed for each channel. The most important registers used during testing and their functions are shown in Table 6.1. Registers 0-5 control the overall operation of the ASIC whereas registers 6 and 7 are only readable. Register 1 allows the ASIC to be configured in either hole mode or electron mode and register 2 is dependent upon the ASIC's position within the four ASIC chain. All measurements in this work have been carried out with a 100 MHz input clock from which several lower rate clocks are generated. Registers 10-20 control the reference voltages for the different functional blocks with 8-bit resolution. The 8-bit registers subsequently have a range of digital values from 0-255 that allow voltages only within the range 0.5-2.5 V. The ASIC's signal processing chain can only process signals within the range 0.5 to 2.5 V. Registers 80-95 allow the channels of the ASIC to be powered off or on in groups of eight.

Throughout this chapter, if not stated, all register values assume the default values in Table 6.1. Once the registers are programmed for either electron or hole mode, the data acquisition can commence. The test pulse injection circuitry is enabled whereby a test pulse can be applied to a test capacitance and charge is injected into the preamplifier. Pulses were injected simultaneously into 16 non-adjacent channels at a time. After receiving the pulses, the 16 channels were then powered off and another block of 16 non-adjacent channels were powered up prior to receiving the test pulses. This process of pulsing individual channels is repeated until all channels of the ASIC are pulsed. Various aspects of the ASIC performance have been studied using this technique as well as noise generated hits. Injecting pulses into all 128 channels simultaneously may have caused cross-talk issues and the large number of test capacitors connected to the test pulse circuitry would have lengthened the pulse rise time ($\approx$ 80 ns and 500 ns for simultaneously pulsing 16 and 128 channels, respectively).

6.2 Stability Over Time

It is important that results taken with the same system at different times are consistent in order to obtain meaningful comparisons and conclusions. Understanding whether results can be reliably reproduced for independent tests on different days is thus crucial to the ASIC's performance.

Table 6.2: The parameters used to test the reproducibility of the ASIC performance.

DAPB [μs]	τ_{peak} [μs]	Eth [DN]	V_{test} [DN] [MeV]	Width [μs]	Delay [μs]
15.0	4.0	160	[26] [13.2]	10	600

6.2.1 Measurement Technique

A particular peaking time, sampling time and energy threshold were selected. The register settings for this test are outlined in Table 6.2. A total of 512 test pulses were injected into each of the 128 channels of the ASIC using the same register settings. The number of measured pulses (entries) and the corresponding ADC value was recorded and the process was then repeated within several minutes using the same settings. At a later date, the ASIC was configured using the same register settings and another data set was taken to provide a comparison over a longer period of time. This process was repeated for both the electron mode and hole mode.

The electron mode and hole mode configurations operate with different parameters and some different circuitry, it is therefore expected that the response of the two modes will be different but similar. The aim of this test is not to compare the two modes but to verify the consistency of each mode separately.

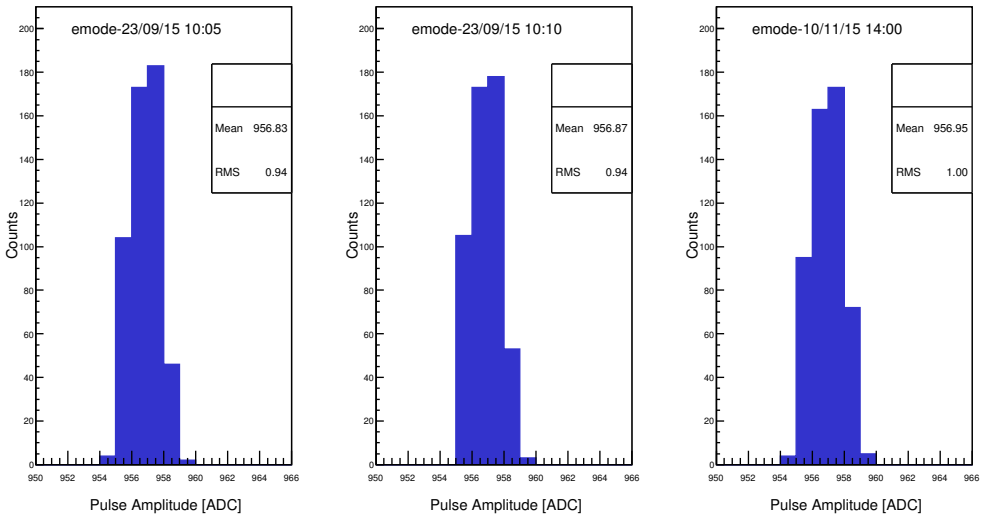
6.2.2 Results

Analysis of the measured ADC values was undertaken so as to obtain a mean and RMS value for each channel ($\sigma = \text{RMS} = \frac{\text{FWHM}}{2.35}$). The mean ADC values for 512 pulses in a single channel (channel 10) in electron mode are shown in Figure 6.3a for the three repeat measurements. The results of three repeated measurements for the hole mode configuration are shown in Figure 6.3b. The date and time of each data set is shown.

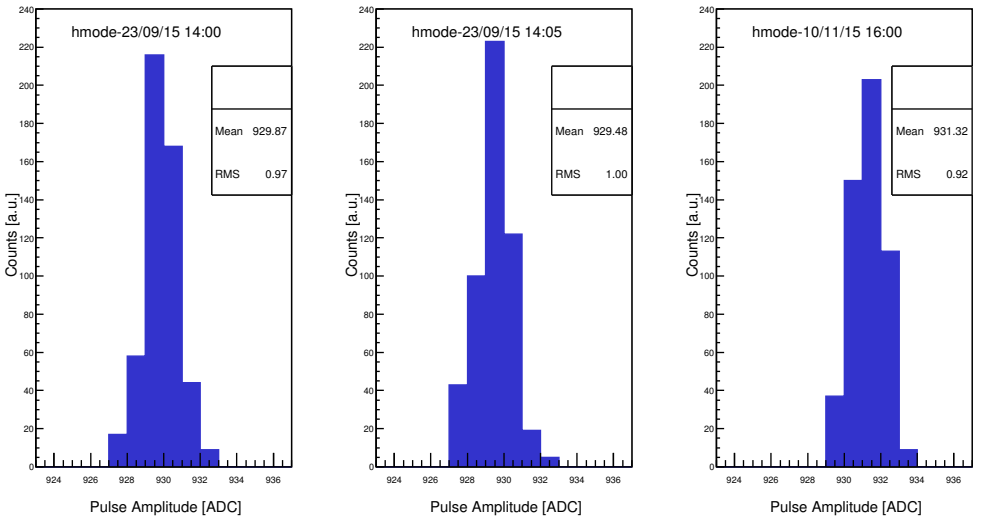
The calculated mean and RMS values for the three data sets are presented in Table 6.3 for electron and hole mode. The condition for two independent measurements of the same quantity to be consistent is

$$|\overline{x_1} - \overline{x_2}| < 3\sqrt{\Delta x_1^2 + \Delta x_2^2}\ . \tag{6.1}$$

In this equation, $\overline{x_1}$ represents the mean ADC measured by channel 10 for measurement 1, $\overline{x_2}$ is the mean ADC value measured for the same channel for measurement 2, Δx_1 is the standard error on the mean ($\text{RMS}/\sqrt{N}$) for measurement 1 and Δx_2 is the standard error on the mean for measurement 2, where $N = 512$ is the number



(a) Electron mode.



(b) Hole mode.

Figure 6.3: Three histograms displaying the measured ADC values, for three independent measurements, where 512 pulses were injected into the channels of the ASIC. Only the recorded ADC values for channel 10 are plotted and the values of the mean and standard deviation of each distribution are shown.

of injected pulses. The mean ADC and RMS values for all independent measurements in electron mode are consistent with each other, as shown in Table 6.4. The measurements taken for the hole mode setting reveal a larger variation in measured ADC and do not meet the consistency criteria. For hole mode, the data sets taken

Table 6.3: Mean and RMS ADC values obtained for repeated measurements of channel 10 for electron and hole mode.

	Electron Mode		Hole Mode	
	Mean [ADC]	RMS [ADC]	Mean [ADC]	RMS [ADC]
23/09/15 10:05	956.83	0.94	929.87	0.97
23/09/15 10:10	956.87	0.94	929.48	1.00
10/11/15 14:00	956.95	1.00	931.32	0.92

on the same day show a much smaller variation in measured ADC in comparison to the data set taken several weeks later.

The mean ADC value for channel 10 in electron mode is different to the mean value obtained for channel 10 in hole mode. It is expected that the two modes will have different ADC values for the same test pulse parameters. This is due to the two configurations using different circuitry and different operating voltages for some parts of the signal processing chain. A rough estimate for the expected ADC value, can be calculated, for a 13.2 MeV test pulse. The previously calculated value for the theoretical front-end gain is stated in equation 5.25 as 0.06174 ADC/keV. Using a test pulse of $V_{test} = 26$ DN (13.2 MeV), a minimum ADC value of approximately

$$13.2 \times 1000 \times 0.06174 \approx 815 \text{ ADC} \tag{6.2}$$

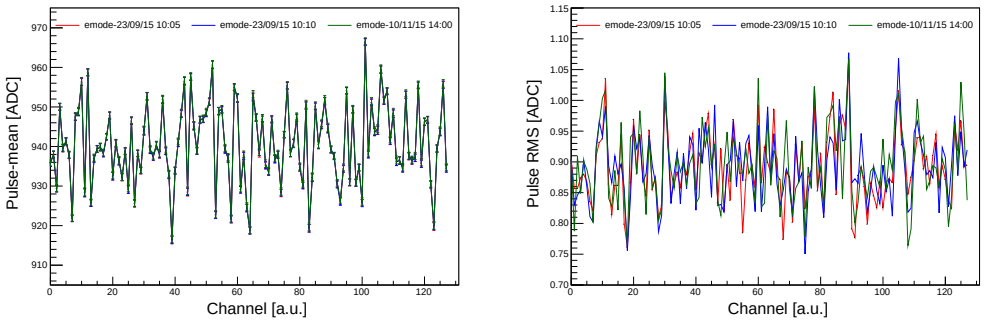
would be expected. When accounting for the added ADC offset due to the shaper reference voltage V_{SHA}, a maximum of about 1050 ADC (influenced by shaper reference voltage variation) would be expected for a 13.2 MeV test pulse. This calculated value is comparable with the measured ADC values. The RMS ADC values for all measurements are about the width of one ADC bin and thus the RMS noise can be quoted as approximately 16 keV (1 ADC) for channel 10 for the settings used in this test.

The same principles outlined above for a single channel have been implemented to calculate the mean and RMS ADC for all 128 channels of one ASIC. The mean ADC values for all the channels for three independent repeated measurements are displayed in Figure 6.4a and the corresponding RMS is shown in Figure 6.4b for electron mode. In Figure 6.5a and Figure 6.5b the mean and RMS values recorded for the hole mode configuration are plotted. All channels recorded a mean ADC value within the range 909 - 966 for both modes using the same pulse settings. The ADC for every channel shows good reproducibility, with all three of the repeated measurements having measured values within 5 ADC of each other. The recorded

Table 6.4: The independent measurements for electron mode are consistent whereas measurements for hole mode are shown to be inconsistent according to the relationship outlined in equation 6.1. The calculated value for the standard error on the mean is used for Δx_1 and Δx_2.

Electron Mode			
$\overline{x_1}$	$\overline{x_2}$	$\lvert\overline{x_1} - \overline{x_2}\rvert$	$3\sqrt{\Delta x_1^2 + \Delta x_2^2}$
956.83	956.87	0.04	0.18
956.83	956.95	0.12	0.18
956.87	956.95	0.08	0.18
Hole Mode			
$\overline{x_1}$	$\overline{x_2}$	$\lvert\overline{x_1} - \overline{x_2}\rvert$	$3\sqrt{\Delta x_1^2 + \Delta x_2^2}$
929.87	929.48	0.39	0.18
929.87	931.32	1.45	0.18
929.48	931.32	1.84	0.18

RMS values are also very similar for all measurements and very few channels have an RMS ADC value greater than 1.0 ADC ($\approx$ 16 keV). In order to quantify the extent to which the repeated measurements differ it is beneficial to subtract the mean ADC values of one measurement from those of another measurement.



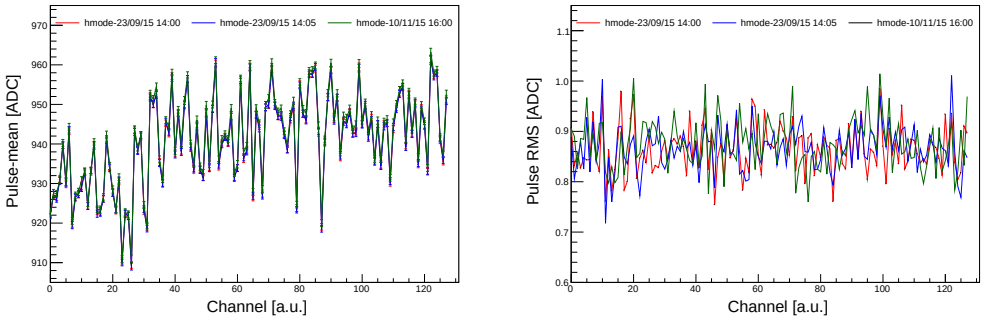
(a) Mean ADC. (b) RMS ADC.

Figure 6.4: The measured mean pulse amplitude and RMS is shown for three measurements that were carried out using the same register settings in electron mode.

In Figure 6.6 the difference between the mean ADC measured by each channel for the three different repeat measurements is calculated for electron and hole mode. The difference between the mean ADC ΔMean for two separate measurements is given by

$$\Delta\text{Mean} = \overline{\text{ADC}_{\text{meas1}}(x)} - \overline{\text{ADC}_{\text{meas2}}(x)} \; . \tag{6.3}$$

The symbol $\overline{\text{ADC}_{\text{meas1}}(x)}$ is the mean ADC measured for channel x for measure-



(a) Mean ADC. (b) RMS ADC.

Figure 6.5: The measured mean pulse amplitude and RMS is shown for three measurements that were carried out using the same register settings in hole mode.

ment 1 and $\overline{\mathrm{ADC}_{\mathrm{meas2}}(x)}$ is the mean ADC measured for the same channel for measurement 2. For both modes, all measurements are consistent across all channels with a mean ADC within 4.5 ADC counts for the same channel for all independent measurements. The greatest consistency is obtained for the electron mode data sets that were taken on the same day. Comparing measurements on the same day, the electron mode data sets show an ever so slightly smaller ADC difference compared to the hole mode measurements. All measurements taken on the same day showed a variation of ADC value of less than 1 ADC, for all but seven channels. The least consistent measurements are for the hole mode data sets that were taken on different days but the difference in the measurements never exceeds 2 ADC counts (30 keV) for any channel.

This allows the conclusion to be made that measurements taken on the same day yield a variation in the mean ADC that is approximately $\leq$ 16 keV (1 ADC) for all channels for both modes. Measurements taken on different days are typically within 2 ADC when comparing independent data sets for the same channel. The remainder of this work will only make direct comparisons between data sets that have been taken on the same day.

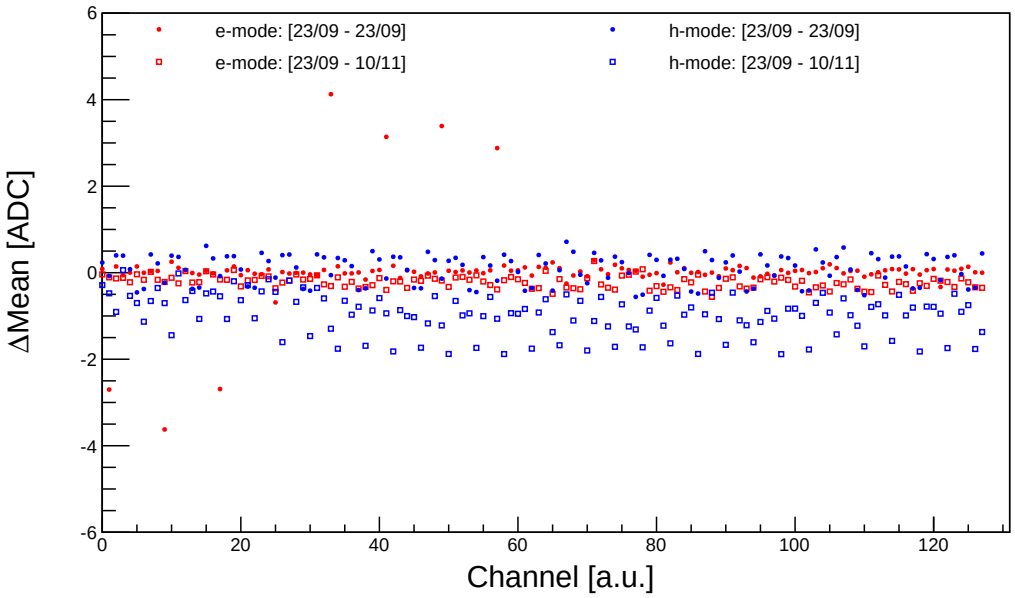


Figure 6.6: The mean ADC of the 512 pulses received by each channel is compared for three independent measurements for electron and hole mode to quantify the change in measured ADC for repeated measurements. The data sets are labelled according to the date on which they were taken (dd/mm). For each mode, two data sets were taken on the same day 23/09 and a third data set was taken on 10/11.

6.3 Channel Readout Logic Timing

The timing of the channel readout logic is outlined in section 5.6. The channel readout logic determines the sequence by which a single channel of the ASIC samples a signal and resets prior to the arrival of the next signal. It is important to test and understand the timing of the readout logic signals and which combinations of settings should be avoided to ensure accurate and reliable data readout.

6.3.1 Measurement Technique

The channel readout logic operates using a 1 MHz clock that is derived from the 200 MHz clock. The ASIC's timing logic can be manipulated by controlling either the delay after peak bit (DAPB) register or the peak-hold reset (PHRST) register. The DAPB setting determines the time at which the signal is sampled in relation to when the signal was first synchronised (t=0 μs) by the clock. The clock frequency means that the time taken between the energy comparator firing and the hit being synchronised is never more than 1 μs.

The time difference between when the signal is synchronised and the time at which a signal is sampled is given by the value of the DAPB (in μs) plus an additional 2 μs. This is because it takes a minimum of two clock cycles from the time at which the hit is synchronised before sampling can be initiated. The DAPB setting can range from 0-15 μs which results in a range of sampling times from 2-17 μs. The time duration required to sample a pulse is 1 μs. The DAPB register should be set to sample the shaped pulse after the peaking time to ensure the maximum pulse amplitude is measured. After the signal has been sampled, the start of the preamplifer reset, shaper reset and PHRST signals occur simultaneously. The duration of the PHRST is programmable for which there is a minimum value of 4 μs, the other reset signals are not programmable. The time at which all of the reset signals begin is dependent upon the programmed DAPB setting. The PHRST setting can be programmed to range from 0-15 μs resulting in an actual reset duration between 4 and 19 μs (PHRST+4 μs).

Altering the values of the DAPB and PHRST settings as well as altering the time duration of the injected pulse (pulse width) provide a means by which the timing logic can be investigated. Tests using a fixed DAPB and PHRST setting have been carried out while the width of the injected pulse was varied from 0.5 to 25.0 μs in increments of 0.5 μs. This test alters the time at which the falling edge of the test pulse occurs in relation to the different timing signals of the ASIC.

Table 6.5: Parameters used for testing the readout logic timing.

DAPB [μs]	τ_{peak}[μs]	PHRST [μs]	Eth [DN]	V_{test} [DN] [MeV]	Width [μs]	Delay [μs]
9.0	4.0	8.0	138	[64] [32.6]	0.5 - 25.0	600

Therefore, a range of pulse widths will probe the effect of the falling edge of the test pulse coinciding with the rising and falling edges of the sample, preamplifier reset, shaper reset and PHRST. This will provide an understanding of where to position the falling edge of the test pulse for future measurements whilst understanding the timing logic of the ASIC.

6.3.2 Results

Data was gathered for a range of pulse widths using the following settings; τ_{peak} = 4.0 μs, DAPB = 9 μs (sampling time of 2+9 μs) and a PHRST = 8 μs (see table 6.5). A schematic of the resulting timing logic for these settings is shown in Figure 6.7. For these settings, the signal is sampled at t = 11 μs after the synchronisation occurs and the reset functions all begin at t = 12 μs with the last signal being the peak hold reset falling edge at t = 24 μs. A total of 512 pulses were injected to each channel for each pulse width and the recorded ADC values were stored. The mean ADC of every channel is plotted against the injected pulse width in Figure 6.8a for hole mode.

The measured ADC data shows the rising edge of the sampled pulse which peaks at t $\approx$ 4.5 μs. Due to the programmed peaking time, it is expected that the measured ADC values should reach a maximum for pulse widths greater than or equal to 4 μs. For pulse widths greater than the peaking time, the peak-hold circuit ensures that only the maximum ADC is stored and as such the falling edge of the shaped pulse is not observed. As the pulse width is increased further, a sharp fluctuation of the measured ADC occurs for some channels at t = 13-14 μs. At t = 20 μs, some channels measure an ADC value that is approximately 60% of the peak amplitude. At t $\geq$ 21 μs, all 128 channels measure an ADC that is roughly 60% of the maximum.

The sharp changes in the measured ADC can be better understood by analysing the dependency of the number of measured pulses on the pulse width, as shown in Figure 6.8b. For t = 0.5-12.5 μs the number of pulses recorded is equal to the number of pulses injected. However, from t = 13-14 μs it can be seen that more pulses are measured than are injected. At t = 20 μs some channels measure twice as many pulses as expected and for t $\geq$ 21 μs all of the channels record twice the

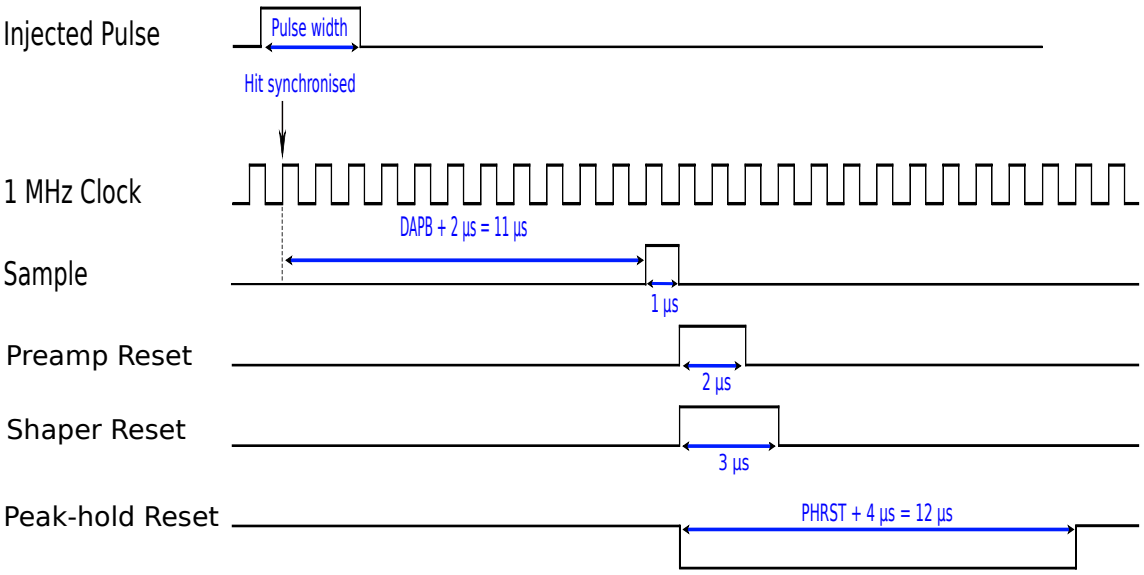
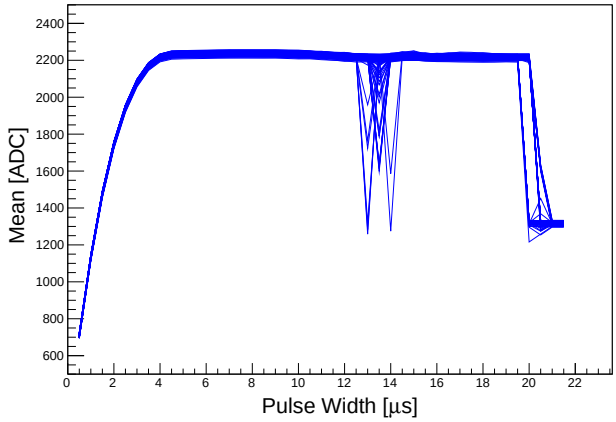


Figure 6.7: The timing diagram of the channel readout logic for a DAPB = 9 μs and PHRST = 8 μs. A test pulse is synchronised by the 1 MHz clock at t = 0 μs. The width of the pulse can be varied so that the falling edge of the pulse occurs at different times.

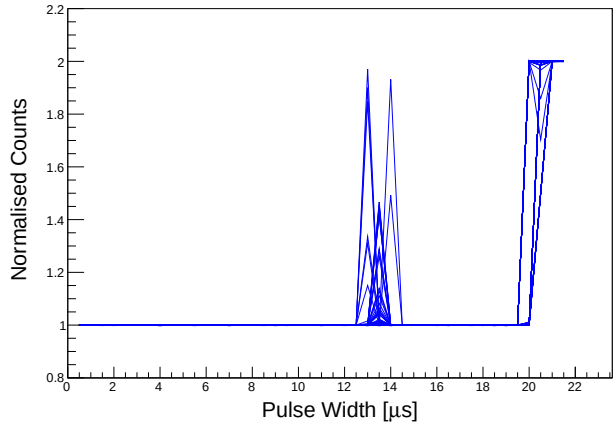
number of expected pulses.

This feature, where more pulses are recorded than are initially injected, can be explained by studying the structure of the timing logic for this measurement. The timing diagram shows that the falling edge of the preamplifier reset occurs at $t = 14$ μs. When $t > 24$ μs, all of the logic signals have been reset and the system is in a state where it is able to receive another pulse. More pulses are measured than injected when the falling edge of the test pulse coincides with the falling edge of the preamplifier reset or if the test pulse falling edge arrives after the peak-hold circuit has been reset. The data also reveals that anomalies are observed in the number of measured pulses for pulse widths with a falling edge that occur prior to the end of the PHRST (the PHRST finishes at t = 24 μs but pulses at t $\geq$ 21 μs are affected).

Another test was repeated for the electron mode configuration using the exact same setting as was used for the previous hole mode testing. The results of measuring the ADC and number of counts for each channel (data packets with same channel address) are shown in Figure 6.9. Just as was seen for the hole mode test, the rising edge of the sampled pulse peaks at t $\approx$ 4.5 μs. A fluctuation in the measured ADC and number of counts is observed at t = 13-13.5 μs due to the falling edge of the preamplifier reset. However the magnitude of the fluctuation is much smaller in comparison with the hole mode data as the number of measured counts



(a) Mean ADC.

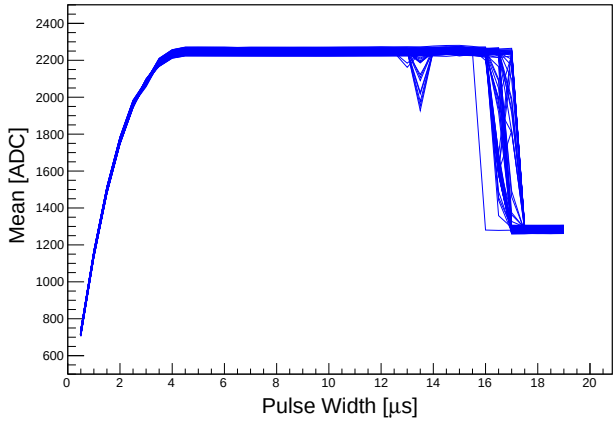


(b) Number of counts.

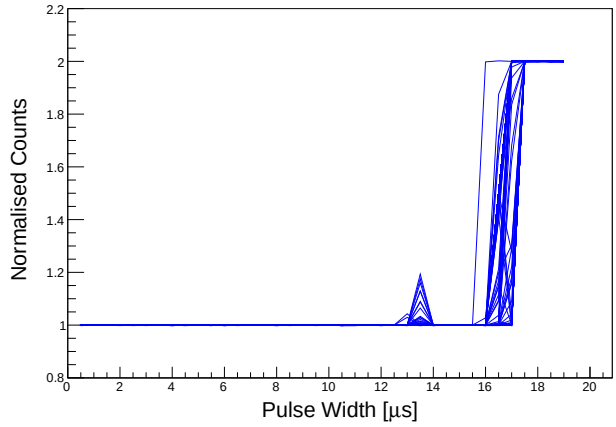
Figure 6.8: The width of the injected pulse was incremented from 0.5 μs to 21 μs in 0.5 μs steps. A total of 512 pulses were injected for each pulse width for hole mode using the following register settings: DAPB = 9 μs, sampling time = 11 μs and PHRST = 8 μs.

is approximately 1.2 times greater than the actual number of injected pulses. At t $\geq$ 17.5 μs all channels measure an ADC value that is approximately 60% of the peak amplitude ADC and all channels record twice the number of expected pulses due to pulse splitting.

The pulse splitting effect is observed for both modes for pulse widths where the falling edge of the pulse occurs before the end of the PHRST. This is contrary to what is expected. Pulse splitting is observed at slightly different pulse widths for the two modes (t $\geq$ 21 μs and t $\geq$ 17.5 μs for hole and electron mode respectively). The time difference between the pulse rising and the next clock signal can result in



(a) Mean ADC.



(b) Number of counts.

Figure 6.9: The mean ADC and number of recorded pulses for a range of pulse widths for electron mode using the following setting: DAPB = 9 μs, sampling time = 11 μs, PHRST = 8 μs.

a synchronisation time difference of up to ± 1 μs that is associated with each quoted time value. The difference in time at which splitting occurs for the two modes is given by Δt = 21 - 17.5 = 3.5 $\pm$ 1.4 μs).

6.3.3 Test Pulse Positioning

In Figure 6.10 a simulation of the ASIC, conducted by the ASIC designer, shows how a test pulse with a falling edge that occurs prior to the PHRST can result in triggering the energy comparator twice. When the test pulse is restored to the baseline there is an undershoot effect. This undershoot results in a signal which occurs after the falling edge of the test pulse which can trigger the energy comparator

Table 6.6: Different configurations of DAPB and PHRST values have been selected and the pulse width scanned from 0-25 μs in 0.5 μs increments. The minimum pulse width (Pulse Width Split) which results in more than one pulse being measured, for a single input pulse, is shown for each setting. The value of 3+DAPB+PHRST+4, signifies the time at which the PHRST signal finishes. The time at which the PHRST signal finishes is not the same as the pulse width at which pulse splitting begins to occur.

DAPB (μs)	PHRST (μs)	3+DAPB+PHRST+4 (μs)	Pulse Width Split (μs)
9	8	24	16
9	9	25	17
9	10	26	18
9	11	27	19
7	11	25	17
7	13	27	19
7	15	29	21

for a second time. Another simulation of the readout logic, shown in Figure 6.11, displays how the test pulse can be positioned to ensure the energy comparator fires once by ensuring the falling edge of the test pulse occurs before the reset signals. A simulation of the readout logic is shown in Figure 6.12 where the undershoot due to the falling edge of the test pulse is shaped. For this configuration, the peak-hold circuit only samples the pulse maximum and the energy comparator fires once.

The ASIC simulations provide a clear explanation as to how pulse splitting may occur depending on the position of the test pulse falling edge. When the test pulse is restored to the baseline, an undershoot effect can occur which can cause the readout of more than one signal. The values in Table 6.6 are the results of several measurements obtained via scanning the pulse width for different combinations of PHRST and DAPB. The measurements prove that the pulse width at which splitting occurs can be altered by changing the DAPB or PHRST settings. Increasing the value of PHRST and/or DAPB causes pulse splitting to occur at larger values of pulse width. This is confirmation that the two registers can be used to control the timing of the readout logic.

To ensure the reliable and accurate readout of injected test pulses, the readout logic and pulse width should always be configured such that the falling edge of the test pulse occurs before the reset signals occur. Only measurements carried out using this guideline are presented in the rest of this work.

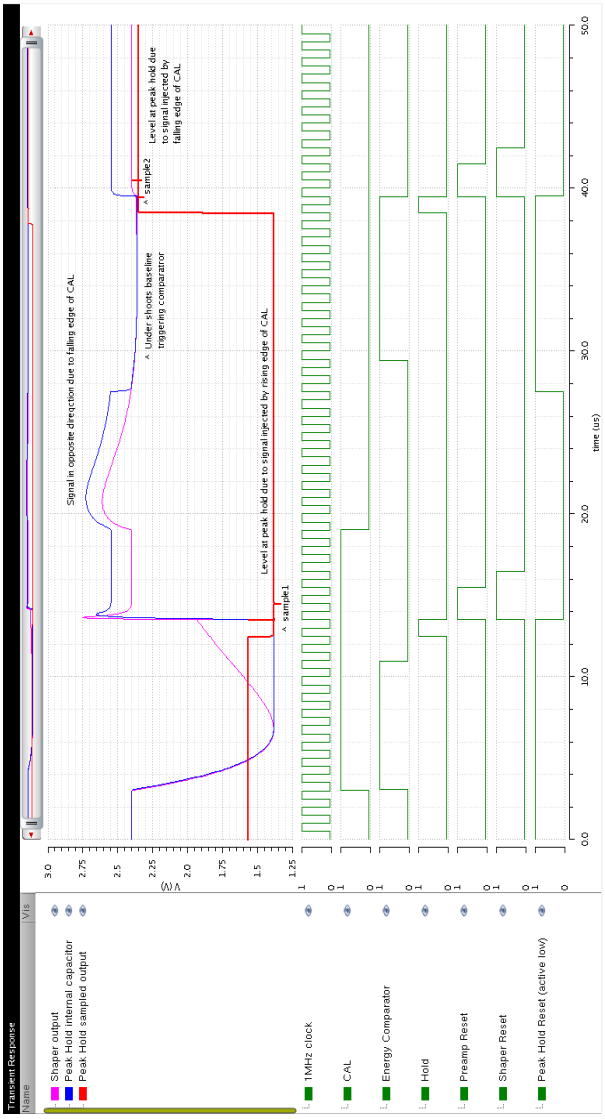


Figure 6.10: An ASIC simulation demonstrating how two pulses may be measured for one injected pulse. The falling edge of the test pulse (CAL) occurs after the shaper reset and during the peak-hold reset. When CAL is restored to the baseline, an overshoot occurs which is passed to the shaper and peak-hold circuit. As the overshoot is gradually restored to the baseline it produces an undershoot which is shaped and passed to the energy comparator. The undershoot is present after the peak-hold reset. The negative going shaper output due to the undershoot triggers the energy comparator which begins the readout of another pulse with another ADC value.

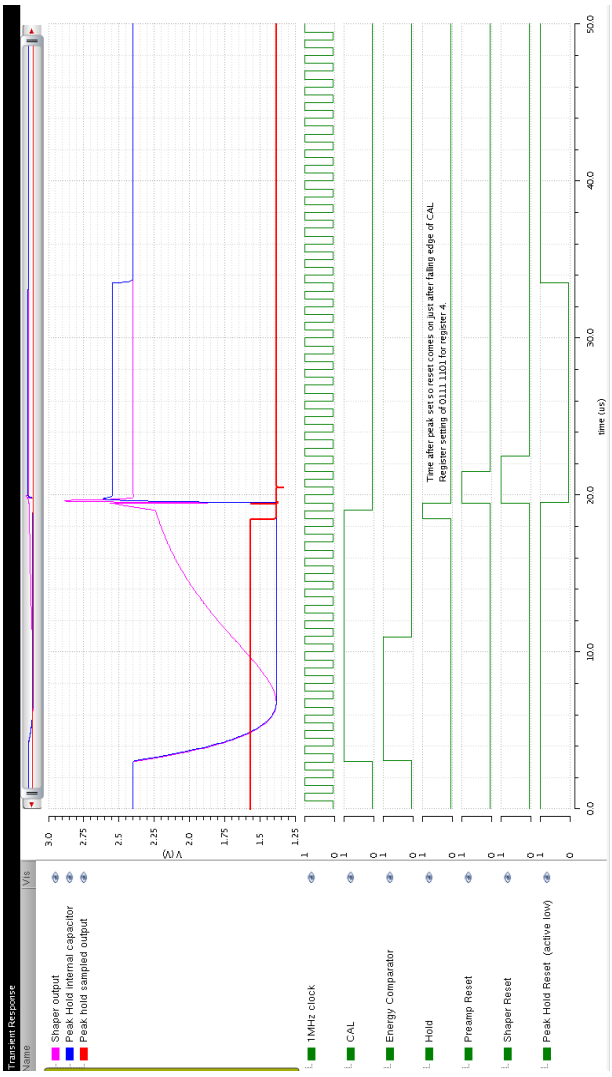


Figure 6.11: An ASIC simulation which demonstrates how the falling edge of the test pulse can be positioned to avoid the energy comparator triggering more than once for the same test pulse. The test pulse and DAPB setting are selected such that the test pulse (CAL) is restored to the baseline prior to the reset signals. This means the undershoot and overshoot, due to the falling edge of the test pulse, occurs before the shaper and preamplifier are reset.

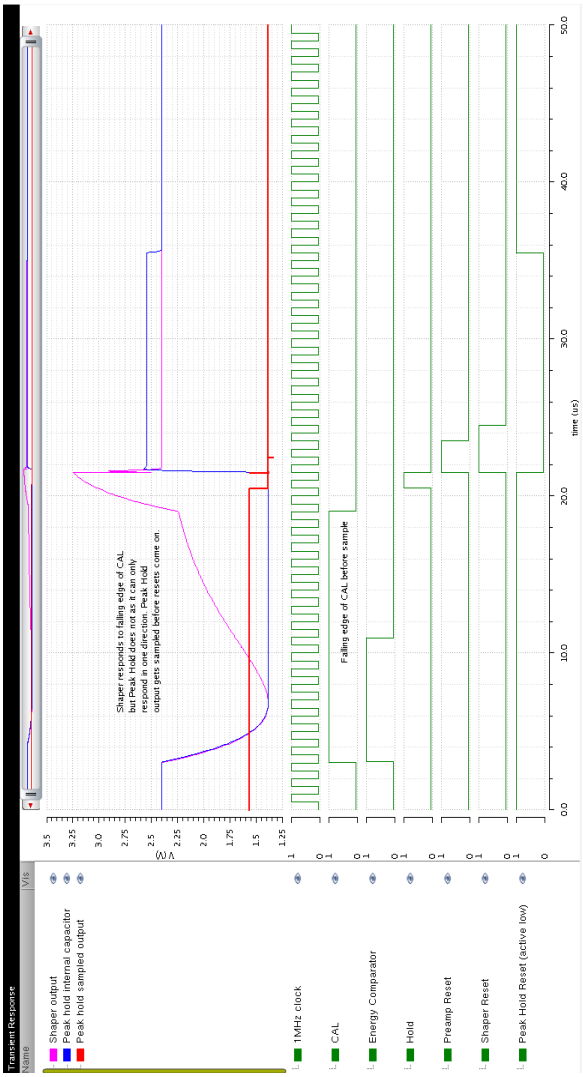


Figure 6.12: An ASIC simulation by the chip designer of the readout logic where the falling edge of the test pulse occurs before the reset and is shaped. The peak-hold circuit is only able to sample the pulse maximum and thus the undershoot presents no issues.

6.4 Four ASIC Readout

The previous measurements all show the response of a single ASIC (ASIC 1) where the channels of the three remaining ASICs in the chain (3, 5 and 9) were powered off during testing. Operation of the silicon tracker will require the readout of many ASICs so it is important to understand the variation in response from one ASIC to the next and crucially, to ensure that ASIC 1 (the focus of most of the testing) behaves like any other ASIC. This test requires all ASICs from a single chain to be read out.

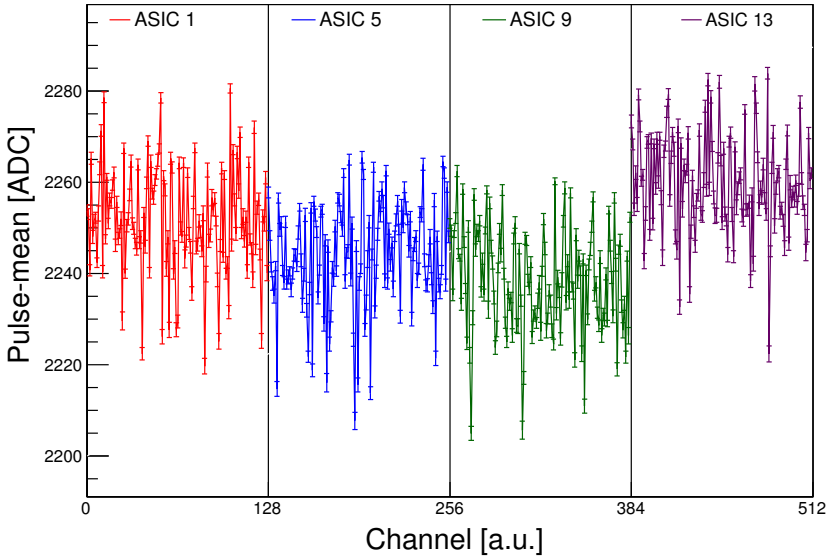
All four ASICs of the chain have been tested using the parameters outlined in Table 6.7 by firstly configuring all of the chips then powering off all chips other than the one to be tested. The remaining powered up ASIC receives pulses by grouping channels together (16 non-neighbouring channels are simultaneously pulsed). After all channels have been pulsed, the ASIC is powered off and the next ASIC in the chain is powered up before receiving pulses.

Table 6.7: Parameters used for testing the readout of multiple ASICs.

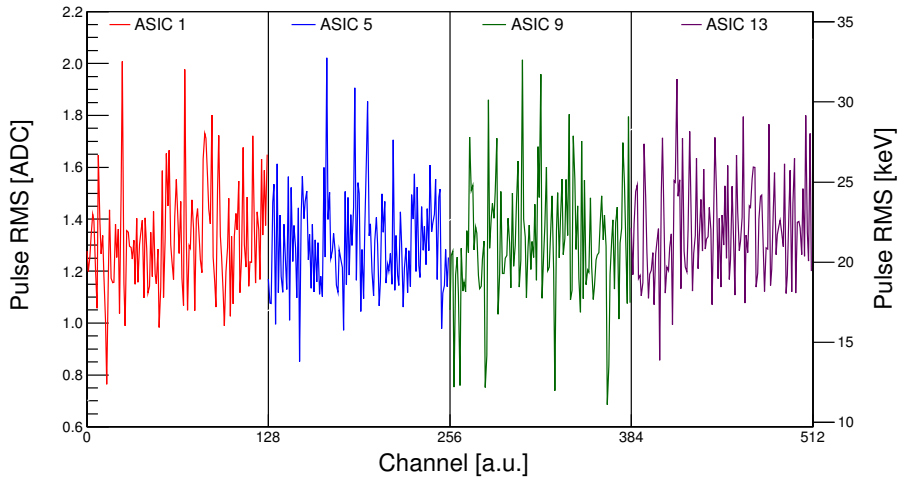
DAPB [μs]	τ_{peak}[μs]	Eth [DN]	V_{test} [DN] [MeV]	Width [μs]	Delay [μs]
11.0	4.0	138	[64] [32.6]	10.0	600

The mean and RMS ADC for each channel, obtained by injecting 512 pulses and reading out the data from all four ASICs of the chain for electron mode, are shown in Figure 6.13. All of the ASICs tested produce a similar response with no dead channels and uniform RMS ADC across the chip ranging between approximately 0.7 and 2.0 ADC, which is equivalent to 11-32 keV. The mean and RMS ADC values obtained for the hole mode measurement are presented in Figure 6.14.

This test has confirmed that ASIC 1 has a response which is similar to the other ASICs within the chain and that all ASICs of a single chain can be read out. All channels of ASIC 1 recorded a mean ADC within the range 2240-2300 ADC, for the same test pulse, therefore all channels have a similar front-end performance. The RMS noise was typically within the range 0.8-1.6 ADC for all ASIC for almost all channels. Slight variations in behaviour may be seen from ASIC to ASIC as different parts of the wafer, from which the ASICs are cut, may have slightly different properties. Hereafter only results of the testing carried out on ASIC 1 will be presented.

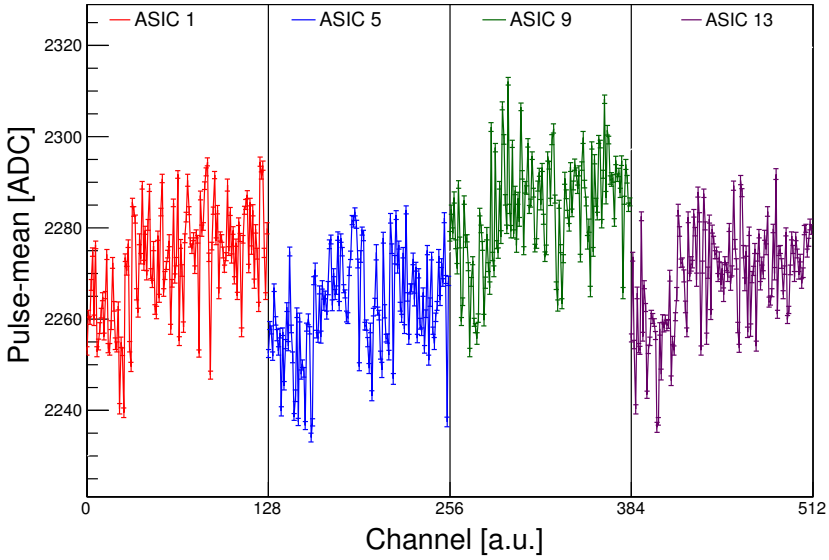


(a) Mean ADC.

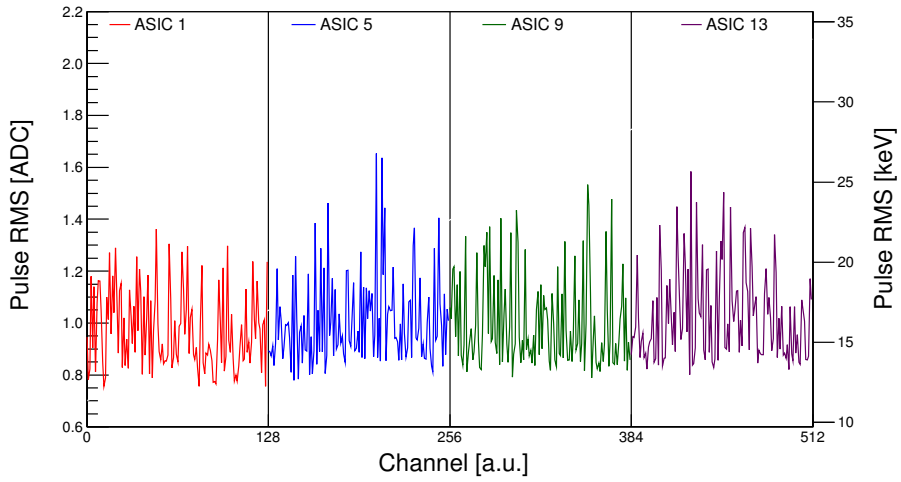


(b) RMS ADC.

Figure 6.13: Electron mode data collected for the readout of four ASICs constituting one chain.



(a) Mean ADC.



(b) RMS ADC.

Figure 6.14: Hole mode data collected for the readout of four ASICs constituting one chain.

6.5 Energy Threshold Trimming

One of the key programmable parameters of the ASIC is the reference voltage which is applied to the energy comparator, known as the energy threshold (Eth). A signal from the preamplifier is passed to the shaper, then a $\times 10$ gain amplifier ($SHA10$) before being passed to the energy comparator. The shaped signal is compared to the energy threshold voltage at the energy comparator. The smallest signal that can be detected will be determined by the noise at the energy comparator. For detecting the smallest signals (few hundred keV) the comparator's threshold voltage will be programmed to a level which is just above the noise. This test will focus on trimming the energy threshold so that the threshold conditions are uniform for all channels of an ASIC. The smallest possible energy threshold will be determined for each channel. The noise at the energy comparator will be quantified for each channel for three different peaking times.

6.5.1 Comparator Threshold Scanning

The energy threshold is a global parameter that is applied to all channels of the same chip. An additional trimming circuit is included that allows fine tuning of the baseline signal at the inverting input of the energy comparator, whereby the energy threshold can be trimmed on a channel by channel basis. The threshold is programmed by selecting a digital number (DN) from 0-255 (8-bit binary number), which equates to a voltage in the range 0.5 to 2.5 V. The selected voltage is then applied to the non-inverting input of the energy comparator which acts as a threshold voltage.

When no signal is present, the shaper output has a baseline voltage equivalent to the shaper's reference voltage. The shaper's baseline signal is passed to the $\times 10$ gain amplifier $SHA10$ which has an output with a baseline amplitude equal to the $\times 10$ gain amplifier reference voltage V_{SHA10}. Therefore, the baseline voltage at the energy comparator's inverting input is given by the $\times 10$ gain amplifier reference voltage, as shown in Figure 6.15. The default value of the $\times 10$ gain amplifier reference voltage is $V_{SHA10} = 1.5$ V for both electron and hole mode. The $\times 10$ gain amplifier reference voltage and energy comparator threshold voltage are programmed by registers such that they are the same for all channels of the same chip and range from 0.5 to 2.5 V.

Mismatches in the transistor sizes within the $\times 10$ gain amplifier and energy comparator can result in the actual $\times 10$ gain amplifier reference voltage and comparator

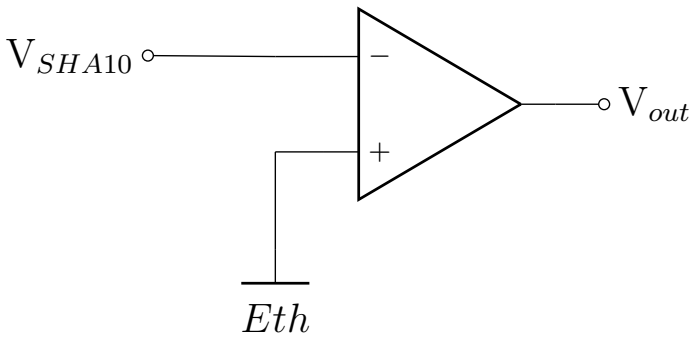


Figure 6.15: A circuit diagram of the comparator used to apply an energy threshold condition. The signal at the comparator's inverting input is equal to V_{SHA10} when no signal is present.

threshold voltage differing from their expected values for different channels of the same ASIC. Some channels may have slightly larger or smaller ×10 gain amplifier reference voltages whilst also having an energy threshold voltage that is slightly different to the expected value. The result is a misalignment of the baseline signal V_{SHA10} and the threshold voltage of the energy comparator Eth. The extent of the misalignment will differ from channel to channel and result in each channel having a different energy threshold condition. Figure 6.16 shows an exaggerated misalignment of the two signals V_{SHA10} and Eth and how this affects the energy threshold of individual channels.

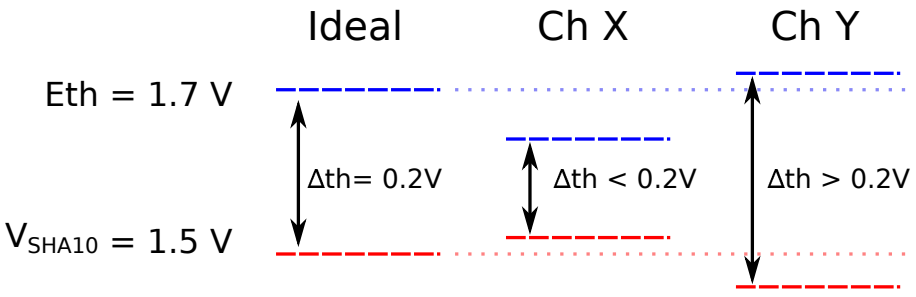


Figure 6.16: A schematic showing the ×10 gain amplifier reference voltage V_{SHA10} in red and the energy comparator's threshold voltage Eth in blue. The applied voltages for V_{SHA10} and Eth may differ slightly from the ideal values expected by the register settings. This may result in the effective threshold Δth being smaller for some channels (channel X) and larger for other channels (channel Y).

The discrepancy between the baseline of the signal at the energy comparator input and comparator threshold voltage can be rectified via a process known as threshold trimming. The trimming process is where a small offset voltage is added

to or subtracted from the $\times 10$ gain amplifier baseline signal V_{SHA10} on a channel by channel basis to correct for any misalignment.

A measurement was first performed where all register settings remained constant and only the energy comparator threshold voltage was varied. The comparator threshold voltage was scanned from the minimum (0.5 V or 0 DN) to the maximum (2.5 V or 255 DN). The energy threshold was thereby scanned across the V_{SHA10} baseline signal at the comparator's inverting input, which was programmed at its defualt value of $V_{SHA10} = 1.5$ V (128 DN). All measurements were carried out with no test pulse injection, only using the fluctuation of the baseline signal due to noise to generate hits. A hit occurs when $V_{SHA10} > Eth$ which results in the comparator output being a logical-high. The number of hits was measured for each threshold voltage setting for a time window of one second.

The effect of scanning the energy comparator threshold voltage is depicted in Figure 6.17. This schematic demonstrates how a small hit rate is observed for low and high thresholds and a maximum hit rate is observed when the values of Eth and V_{SHA10} are aligned. When the threshold voltage is much lower than the baseline voltage ($Eth < V_{SHA10}$), the comparator is in a saturated state and unable to reset unless the noise of the baseline momentarily falls below the threshold voltage. The number of measured hits is very low for small threshold voltages due to the inability of the comparator to be reset. As the threshold voltage increases it approaches the baseline voltage V_{SHA10} and the number of hits measured per second increases as the comparator is able to reset and then measure the next hit. When the threshold voltage is equal to the baseline ($Eth = V_{SHA10}$), the number of hits per second is a maximum because the baseline noise results in a signal which frequently crosses the threshold level. When the threshold voltage increases above the baseline level ($Eth > V_{SHA10}$) there are very few measured hits. For high thresholds, hits are only measured if the baseline momentarily exceeds the threshold level due to noise. The number of hits decreases as the threshold voltage increases further.

If a real pulse is passed from the shaper to the $\times 10$ gain amplifier, the output of the $\times 10$ gain amplifier is positive going for the electron mode case and negative going for the hole mode scenario. A polarity switch is included within the comparator that enables the comparator to operate in either hole or electron mode whilst using the same energy threshold register settings. This means that even though the electron mode and hole mode signals have different signal orientations, the polarity switch allows the threshold setting for both modes to be directly comparable.

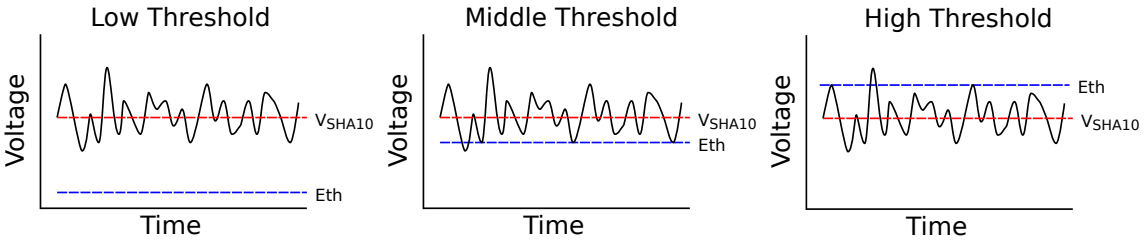


Figure 6.17: A schematic of scanning the energy comparator threshold voltage Eth across the baseline signal V_{SHA10} from the $\times 10$ gain amplifier. For low threshold settings, very few hits are measured as the comparator is in a saturated state and unable to reset. As the threshold is increased (towards middle threshold) the energy threshold occasionally exceeds the baseline, which enables the comparator to reset and record a hit. For a high threshold, hits are only recorded if the baseline noise exceeds the threshold.

6.5.2 Results Before Trimming

Only data within the range Eth = 119-138 DN (1.43-1.58 V) has been analysed. Outside of this range the comparator is either saturated (low threshold) or the baseline is much smaller than the value of Eth (high threshold) so that no hits are recorded. The result of keeping all registers fixed (V_{SHA10} = 1.5 V) and scanning the comparator threshold from the minimum to the maximum value is shown in Figure 6.18 for three different peaking times for electron mode. Figure 6.19 shows the same measurement for three peaking times in hole mode. Hits that occur for $Eth > 128$ DN are due to noise whereas hits at small values of Eth are observed as the comparator gradually becomes unsaturated.

A value of Eth = 128 DN should result in a comparator threshold voltage of 1.5 V which would mean that $V_{SHA10} = Eth$ for all channels. Therefore if there were no mismatches, the maximum number of hits should occur for every channel at $Eth = 128$ DN. The threshold scan data shows that for each channel, the alignment of Eth and V_{SHA10} occurs at different values of Eth. This means that the energy threshold conditions differ from one channel to the next.

6.5.3 Threshold Trimming

In order for every channel to have the same energy threshold conditions it is crucial that the input signal to the comparator is aligned with the comparator threshold voltage. The comparator threshold voltage and the gain amplifier reference voltage are both global settings that are applied to all channels of one ASIC. Every channel is equipped with a trim DAC (digital to analog converter) circuit at the output of

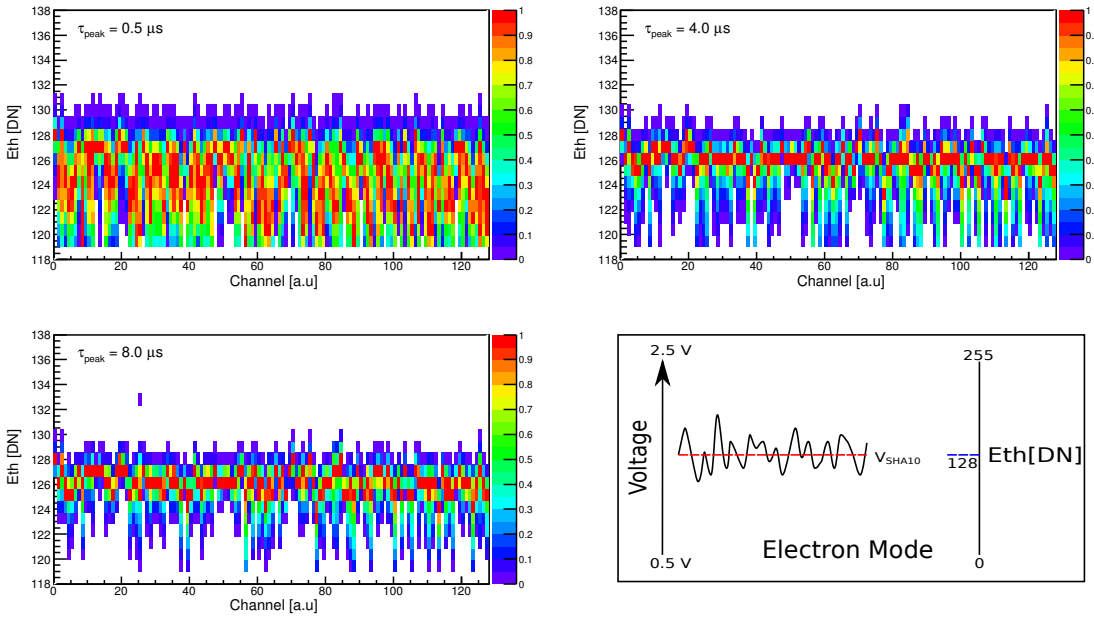


Figure 6.18: Scanning the energy comparator threshold voltage from 119-138 digital number (DN) and measuring the number of hits recorded during one second for each channel. The normalised number of hits per second is plotted for the same settings for three different peaking times in electron mode. A large value of Eth represents a large threshold voltage so that hits which occur for Eth >128 DN are due to noise.

the ×10 gain amplifier and before the comparator input. The trim circuit allows fine trimming of the DC baseline voltage for each channel at the comparator input. The baseline voltage at the comparator input is finely trimmed by adding or subtracting a small offset voltage to/from the baseline voltage V_{SHA10} to align it with the comparator threshold voltage. The trim DAC is programmed via an 8-bit number (0-255 DN). Values in the range 0-126 result in a negative offset and values 128-255 produce a positive offset value that is added to the baseline of the ×10 gain amplifier output. The offset value has a resolution of

$$1 \text{ offset DN} = 1.05 \text{ mV} \tag{6.4}$$

to enable a much finer trimming than would otherwise be capable using just the global registers. Herein, the value referred to as offset ranges from -127 to +127 DN where negative values represent trim DAC register settings of 0-126 and positive values represent register settings of 128-255.

After the initial energy threshold scan, the next step in the trimming process is to determine the offset value required to align V_{SHA10} with Eth for each individual

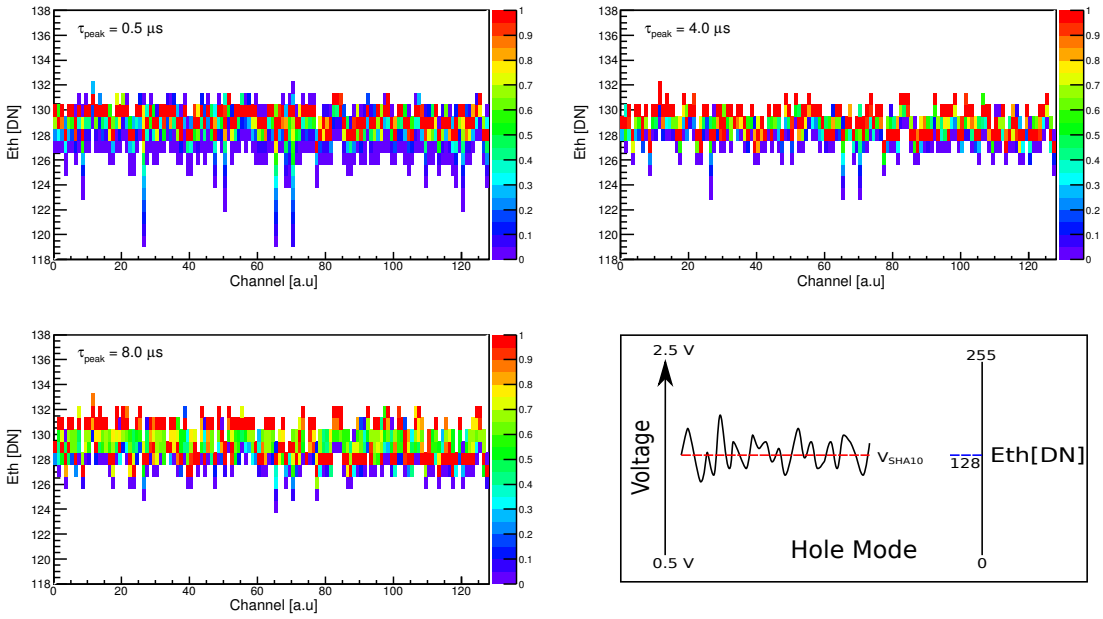


Figure 6.19: Scanning the energy comparator threshold voltage from 119-138 digital number (DN) and measuring the number of hits recorded during one second for each channel. The normalised number of hits per second is plotted for the same settings for three different peaking times in hole mode. A large value of Eth represents a large threshold voltage so that hits which occur for Eth >128 DN are due to noise.

channel. This is achieved by keeping V_{SHA10} and Eth fixed whilst scanning the value of the trim offset from the maximum to the minimum for a single channel at a time. A value of $Eth = 128$ DN (1.5 V) was selected for the comparator threshold voltage for this test. A different value for the comparator threshold voltage can be selected depending on which energy threshold is required, and the trimming process must be repeated if a different threshold voltage is selected. Scanning the offset value, and hence the baseline input voltage ($V_{SHA10} \pm$ offset) to the comparator, will result in the comparator input voltage crossing the comparator threshold voltage at some offset value. When the number of hits recorded is a maximum, then the two signals are aligned and the offset value represents the value required to align the two signals for the channel being tested. Figure 6.20 shows the number of hits measured for each offset value by selecting an energy threshold of $Eth = 128$ DN and scanning the offset value across the full range for electron mode. The corresponding measurement obtained for the hole mode configuration is shown in Figure 6.21.

The data from the offset scans in Figure 6.20 and Figure 6.21 allows the offset value with the largest number of hits (black line) to be determined for each chan-

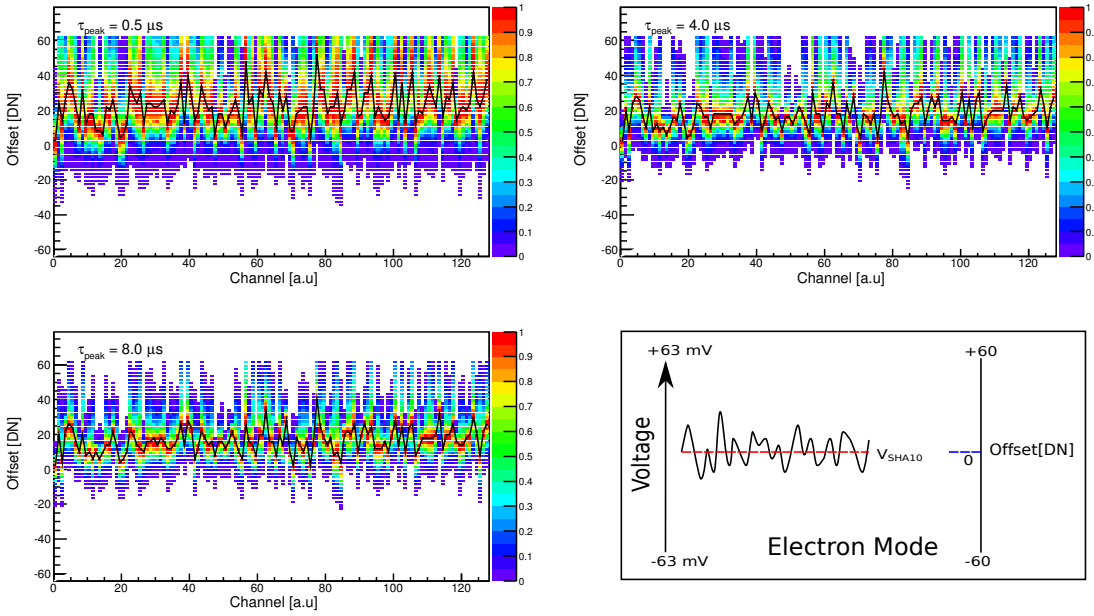


Figure 6.20: The normalised number of hits per second is shown for each channel where the trim DAC offset was scanned from -60 to 60 digital number (DN). The black line represents the offset value for each channel corresponding to the maximum number of hits. Results shown are for electron mode (positive going comparator input signal). A positive offset adds a small voltage to V_{SHA10} which raises V_{SHA10} above Eth so that saturation effects are observed for positive offset values and hits due to noise arise for negative offset values.

nel. A configuration file is then created, which stores the channel number and the associated offset value. The file can then be used to set the offset value for each individual channel that will align the baseline voltage at the comparators inverting input with a comparator threshold voltage of $Eth = 128$ DN.

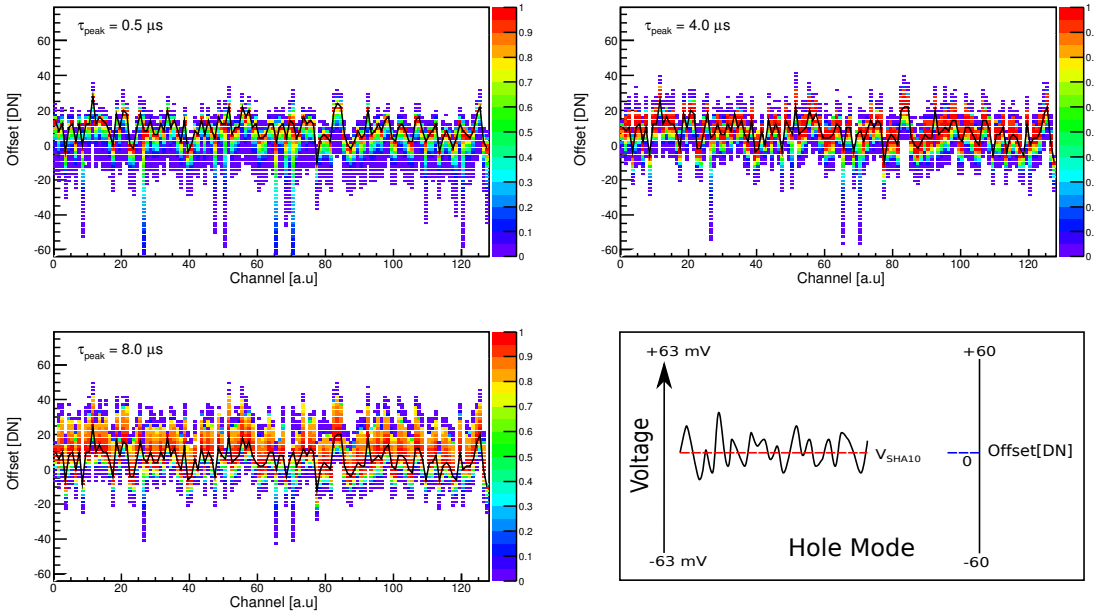


Figure 6.21: The normalised number of hits per second is shown for each channel where the trim DAC offset was scanned from -60 to 60 digital number (DN). The black line represents the offset value for each channel corresponding to the maximum number of hits. Results shown are for hole mode (negative going comparator input signal). A positive offset adds a small voltage to V_{SHA10} which raises V_{SHA10} above Eth so that saturation effects are observed for negative offset values and hits due to noise arise for positive offset values.

6.5.4 Results

The process of keeping all registers constant and scanning the energy comparator threshold voltage can be repeated, but now also applying the unique offset value to each channel. The inclusion of the offset should result in a uniform alignment of the comparator input signal and the comparator threshold voltage across all of the channels. The maximum number of hits for every channel is now expected to occur for a threshold of $Eth = 128$ DN. Figure 6.22 and Figure 6.23 show the result of repeating the process seen in section 6.5.2 but now including the offset values. The data shown is trimmed for an energy threshold of 128 digital number and the normalised number of measured hits is shown for every channel.

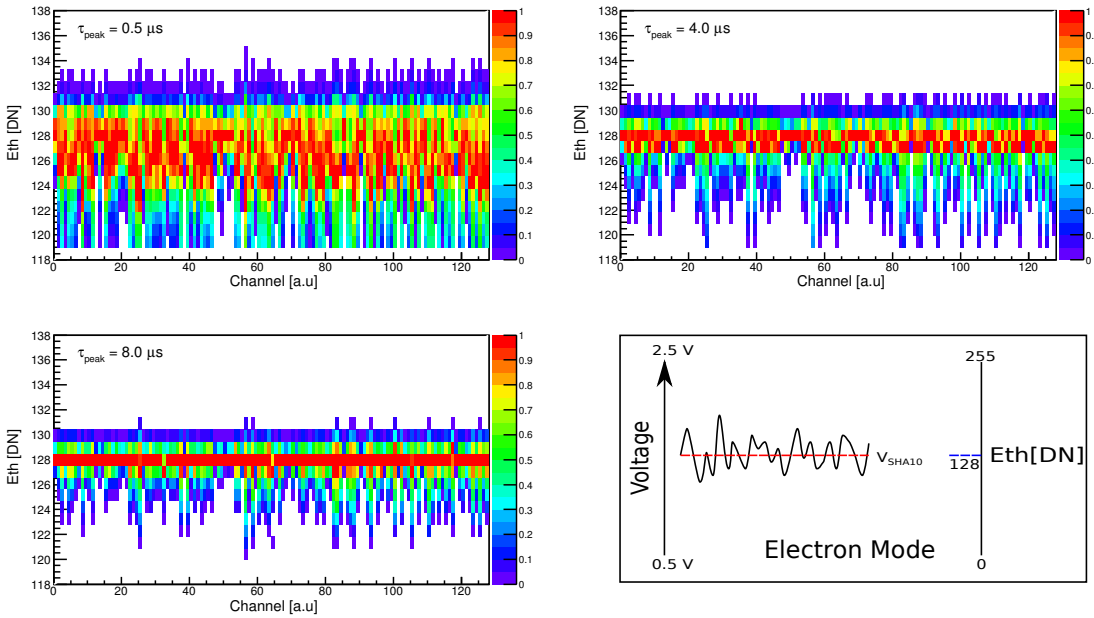


Figure 6.22: After trimming. Scanning the energy comparator threshold voltage from 119-138 digital number (DN) and measuring the number of hits recorded during one second for each channel. The normalised number of hits per second is plotted for the same settings for three different peaking times in electron mode. A larger value of Eth represents a larger threshold voltage.

A change in energy threshold of $\Delta Eth = 1$ DN is equivalent to a voltage change of 7.8 mV at the energy comparator. This equates to a 0.78 mV signal at the input of the $\times 10$ gain amplifier and hence a 0.81 mV ($\frac{0.78}{0.96} = 0.81$) signal at the preamplifier output when accounting for the shaper gain $A_{sha} = 0.96$. Using equation 5.2 a

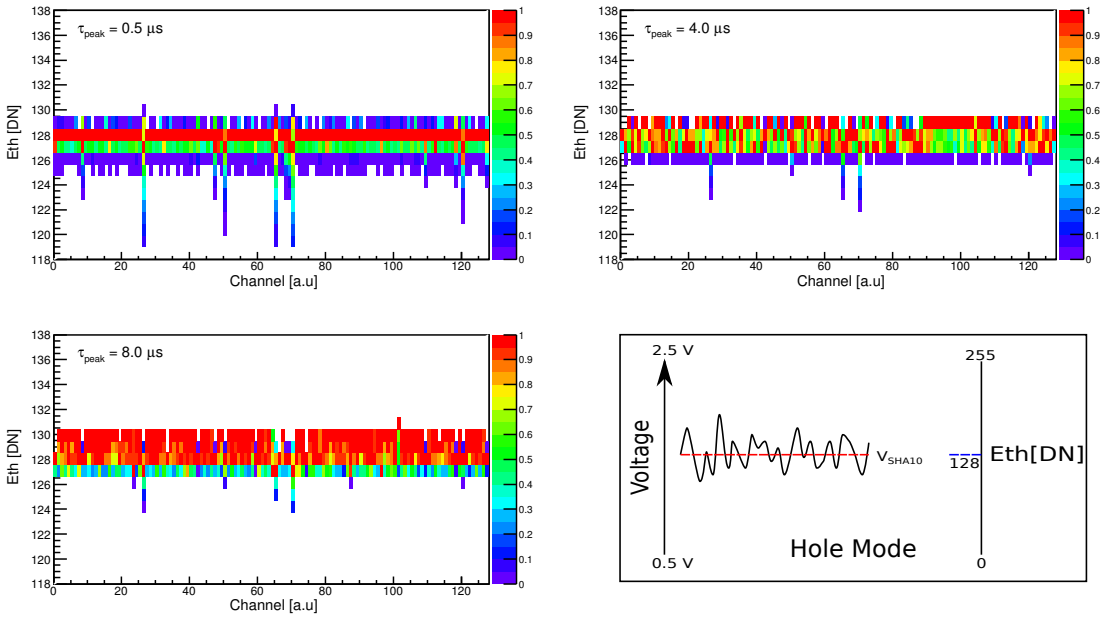


Figure 6.23: After trimming. Scanning the energy comparator threshold voltage from 119-138 digital number (DN) and measuring the number of hits recorded during one second for each channel. The normalised number of hits per second is plotted for the same settings for three different peaking times in hole mode. A larger value of *Eth* represents a larger threshold voltage.

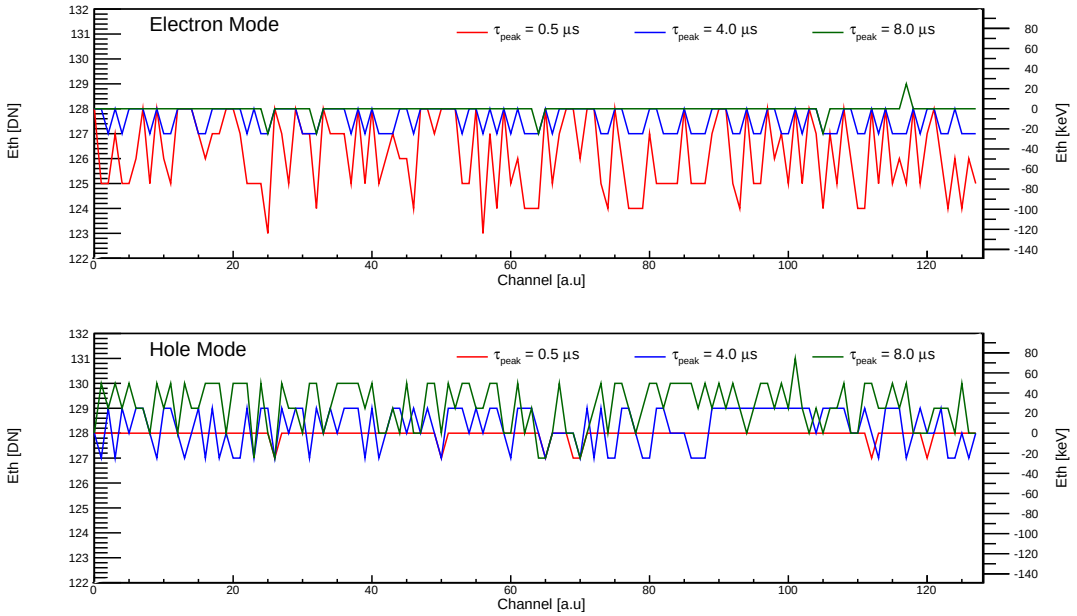


Figure 6.24: The energy threshold at which the maximum number of hits occurred is shown for three peaking times for both modes after trimming for $Eth = 128$ DN.

voltage of 0.81 mV at the preamplifier output is achieved by an injected charge of

$$Q_i = 1.41 \times 10^{-12} \times \frac{0.78}{0.96} \times 10^{-3} = 1.146 \times 10^{-15} \text{ C} . \tag{6.5}$$

According to equation 5.9 this quantity of charge is equal to 25.8 keV so that the energy threshold setting can be expressed in units of keV as

$$\Delta Eth = 1 \text{ DN} = 25.8 \text{ keV} . \tag{6.6}$$

If the energy threshold is trimmed for 128 DN then the setting 129 DN represents a signal level of approximately 25 keV. Figure 6.24 shows the energy threshold value for which the maximum number of hits was measured for each channel. For electron mode, the best alignment of the two signals is achieved for $\tau_{peak} = 8$ μs where all but five channels have recorded the maximum number of hits at $Eth = 128$ DN. For hole mode, the largest number of aligned channels occurred when $\tau_{peak} = 0.5$ μs as all but six channels recorded the maximum number of hits at $Eth = 128$ DN.

As the energy threshold is incremented upwards from 128 DN, the recorded hits are due to noise causing fluctuations of the V_{SHA10} and Eth signals. A critical aspect of the energy threshold trimming is measuring the number of channels that are still triggered for $Eth > 128$ DN and how large must the threshold be to prevent hits occurring due to noise. If a large threshold is required, then very small signals will be undetectable as the threshold will exceed the small signal amplitude. The percentage of channels that fired for each comparator threshold setting after tuning to $Eth = 128$ DN is shown in Figure 6.25 for both modes. The corresponding results are displayed in Table 6.8.

For the hole mode setting, all of the channels fired when the comparator threshold was set to 128 DN. For a comparator threshold of 130 DN, 2,0 and 84% of the channels fired for peaking times of 0.5, 4.0 and 8.0 μs, respectively. For a comparator threshold voltage of 131 DN, no channels fired for the 0.5 and 4.0 μs peaking times and just one channel fired for the 8.0 μs peaking time. A comparator threshold setting of 131 DN represents a threshold level that is about 75 keV above the baseline of the comparator input signal. Therefore the maximum baseline noise seen for the hole mode configuration is between 50 keV and 75 keV for 99% of channels. The lowest noise was measured for a peaking time of 4.0 μs where 100% of the channels had a noise less than 50 keV.

For the electron mode setting 100% of the channels fired for a comparator thresh-

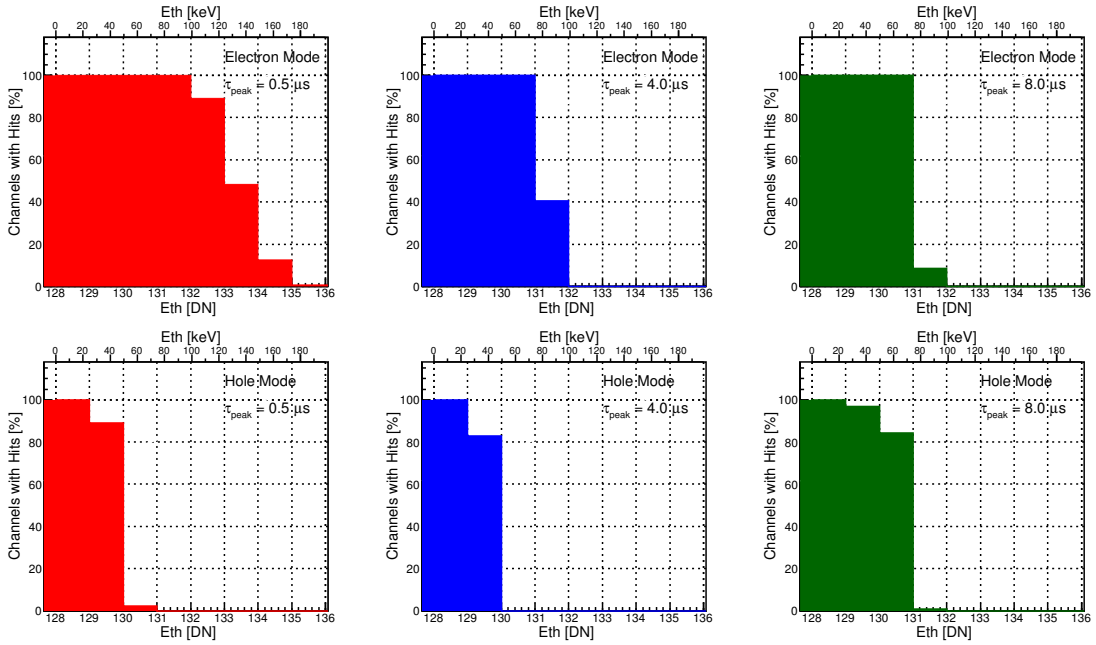


Figure 6.25: The percentage of channels that fired for each threshold setting after trimming the energy comparator.

old voltage of 128 DN. For a threshold voltage of 130 digital number, all channels fired for all three peaking times that were measured. This indicates that 100% of the channels have an electronic baseline noise of at least 50 keV. For the peaking times of 4.0 and 8.0 μs, a comparator threshold of 132 DN yielded no firing channels, which indicates a noise level which is less than 105 keV for all channels. The trimming obtained for the 0.5 μs peaking time suffers from much more noise than the other measurements with 13% of channels having a noise level between 155 keV and 180 keV. The smallest noise level was obtained for a peaking time of 8.0 μs where only 9% of channels had a noise greater than 75 keV and all channels had a noise of less than 100 keV.

The smallest energy threshold that can be set is limited to approximately 100 keV by the noise. The largest threshold that can be set is determined by the maximum threshold voltage that can be applied to the comparator. A register setting of $Eth = 255$ DN corresponds to a voltage of 2.5 V. The default reference voltage of the $\times$10 gain amplifier ($V_{SHA10} = 128$ DN) will always be adhered to for the experimental configuration, resulting in a baseline voltage of 1.5 V. Therefore the largest achievable threshold condition is 1 V above the $\times$10 gain amplifier baseline. A 1 V signal at the energy comparator approximately equates to a 0.1 V signal at the preamplifier output (ignoring shaper gain effects). Using equation 5.2, the charge

Table 6.8: Summary of energy comparator threshold testing data after trimming for an energy threshold of 128 DN.

		Electron Mode			Hole Mode		
		Peaking Time [μs]					
		0.5	4.0	8.0	0.5	4.0	8.0
Threshold [DN]	Threshold [keV]	Hit Channels [%]					
127	-25	100	100	100	100	100	100
128	0	100	100	100	100	100	100
129	25	100	100	100	89	83	97
130	50	100	100	100	2	0	84
131	75	100	41	9	0	0	1
132	105	89	0	0	0	0	0
133	130	48	0	0	0	0	0
134	155	13	0	0	0	0	0
135	180	1	0	0	0	0	0

at the preamplifier input is $Q_i = 0.141$ pC which is equivalent to 3.2 MeV according to equation 5.9. The largest energy threshold that can be applied to each channel of the ASIC is approximately 3.2 MeV, assuming a default reference voltage of the $\times 10$ gain amplifier. If the reference voltage of the $\times 10$ gain amplifier is decreased ($0.5\text{ V} < V_{SHA10} < 1.5\text{ V}$), a larger threshold can be achieved up to ≈ 6 MeV for a positive going signal.

6.6 Pulse Amplitude and Energy Threshold

The measured signal amplitude should be independent of the energy threshold, so that measurements taken with different threshold settings can be compared. The operation whereby the peak-hold circuit stores the maximum amplitude and its output is sampled should be unaltered by changes to the energy comparator threshold voltage. See Appendix A.1 for an analysis of the pulse amplitude measured for different energy threshold conditions.

6.7 Timestamp Threshold Trimming

Every recorded hit has an associated timestamp, which is preferably obtained using the logical-high output of the time comparator. It is possible for a timestamp to be obtained without the time comparator but all testing in this section will focus on timestamps that are generated by the time comparator. A timestamp is generated when the time comparator output fires, due to a signal exceeding the threshold, resulting in a 15-bit timestamp being sampled from the timestamp clock.

Each hit consists of 48-bits in total (section 5.7). A hit with a hit-bit value of 0 has a timestamp that is generated when the time comparator does not fire (energy comparator fired), whereas a hit-bit value of 1 signifies that the timestamp for the hit was generated via the firing time comparator (both time and energy comparators fired). All measurements for this testing have hits with a hit-bit value of 1. The threshold settings of the time comparator will be trimmed so that the threshold conditions are the same for every channel. After trimming, the noise at the time comparator will be measured so that the smallest signal for which a timestamp can be generated (via the time comparator) can be determined.

6.7.1 Time Comparator Properties

The fundamental principles by which the time comparator behaves and how it is programmed are largely the same as for the energy comparator which is discussed in section 6.5. Unlike the energy comparator, the time comparator receives fast signals from the preamplifier via a $\times 10$ gain amplifier with reference voltage V_{PRE10} (energy comparator receives slow signals from the shaper via a $\times 10$ gain amplifier with reference voltage V_{SHA10}). The time comparator is used to compare an unshaped signal from the preamplifier with a specified threshold voltage Tth.

For a positive going signal (signal that increases above baseline) the comparator will fire if the signal is greater than the threshold voltage. For a negative going signal (signal that decreases below baseline) the comparator will fire if the signal is below the threshold voltage. For electron mode, the time comparator receives negative going signals and for hole mode the signals are positive going. This condition is the opposite polarity to that observed for the energy comparator setup where the CR-RC shaper adds another signal inversion stage before the signal is passed to the comparator.

For the energy comparator, increasing the value of Eth represented a larger energy threshold voltage. The opposite is true for the time comparator where larger

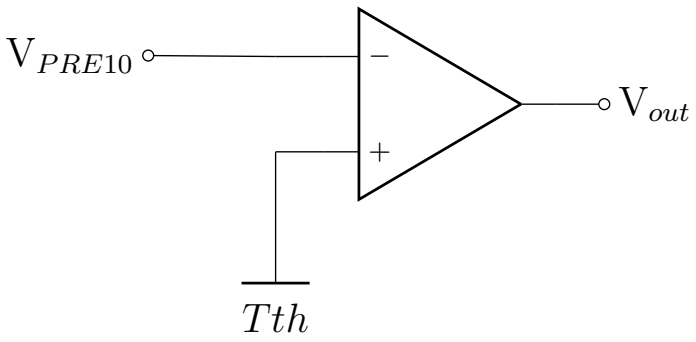


Figure 6.26: A circuit diagram of the comparator used to apply a timestamp threshold condition. The signal at the comparator's inverting input is equal to the ×10 gain amplifier reference voltage V_{PRE10} when no signal is present.

values of Tth represent smaller threshold voltages. For the energy comparator the threshold Eth = 0-255 DN corresponds to a threshold voltage ranging from 0.5-2.5 V. For the time comparator the threshold Tth = 0-255 DN results in a threshold voltage of 2.5-0.5 V.

The signal that is passed directly from the preamplifier to the ×10 gain amplifier and then to the time comparator is expected to have more noise than the shaped signal that is passed to the energy comparator. It is expected that the time comparator will thereby require a higher threshold setting than the energy comparator. The threshold Tth applied to the time comparator is a global parameter, which may differ slightly from channel to channel. To ensure that the threshold conditions for the time comparator are the same for every channel it is necessary to align the baseline signal from the ×10 gain amplifier (V_{PRE10}) with the threshold Tth for every channel using principles similar to those for the energy comparator in section 6.5.

6.7.2 Comparator Trimming

It is not possible to trim the time comparator threshold unless the energy comparator has already been trimmed. This is because the readout of a hit can only occur if the energy comparator is fired. Therefore, testing of the time comparator must be carried out using the previously obtained energy threshold trim settings for each channel.

For the time comparator trimming, the energy threshold Eth and baseline V_{SHA10} are aligned such that the energy comparator threshold is positioned so as to generate the maximum number of hits for each channel. For the time comparator trimming,

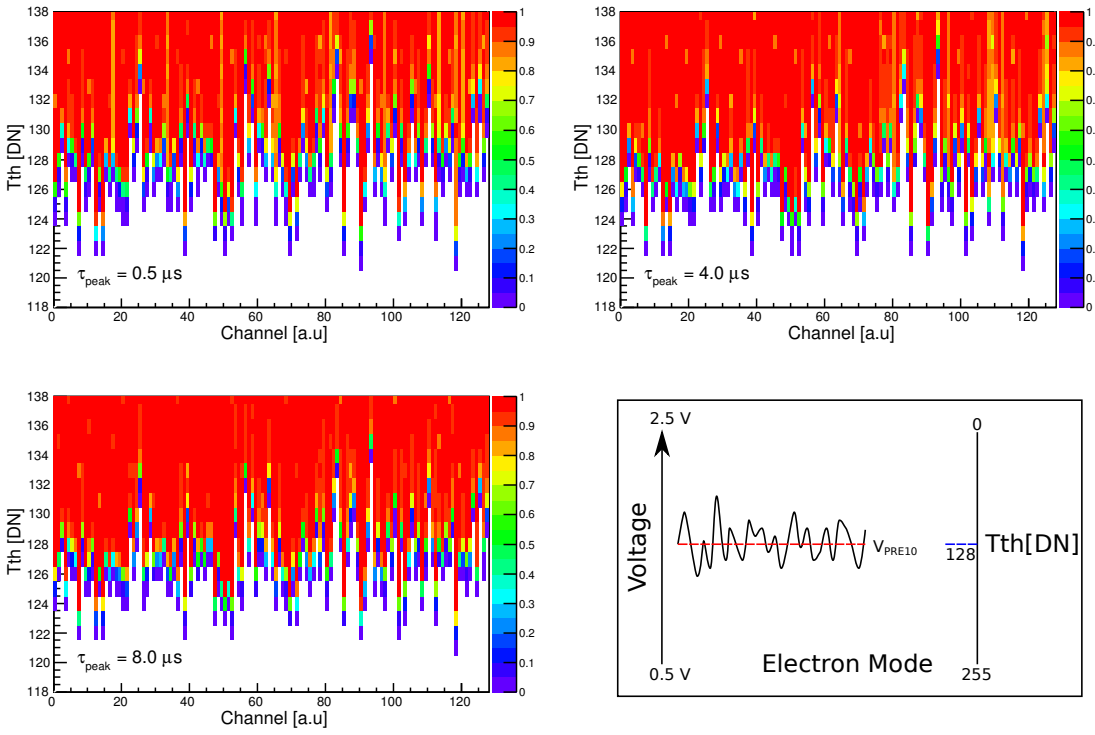


Figure 6.27: A plot of the normalised number of hits measured per second for each channel for three different peaking times in electron mode. A large value of Tth represents a small threshold voltage resulting in many hits.

all registers were fixed (V_{SHA10} = 1.5 V ± offset, Eth = 1.5 V and V_{PRE10} = 1.5 V) and the threshold voltage was scanned from Tth = 118-140 DN (1.59-1.42 V). This means that the energy threshold is positioned to achieve the maximum number of hits per second and only the time comparator threshold is varied. The change in the number of hits measured is therefore only dependent on the time comparator threshold. The results of the time comparator threshold scan (before time comparator trimming) are shown for both electron mode and hole mode in Figure 6.27 and Figure 6.28, respectively.

When the maximum number of hits is observed, this signifies that the threshold voltage is smaller than the baseline voltage V_{PRE10}. The maximum number of hits is observed for large values of Tth (small thresholds), and smaller values of Tth ($<$ 120 DN) result in no hits for all channels because the threshold is larger than the baseline signal. As the time comparator threshold voltage increases (towards smaller DN), the threshold gradually becomes greater than the V_{PRE10} baseline signal. This results in fewer hits with hit-bit equal to 1 and more hits with hit-bit equal to 0

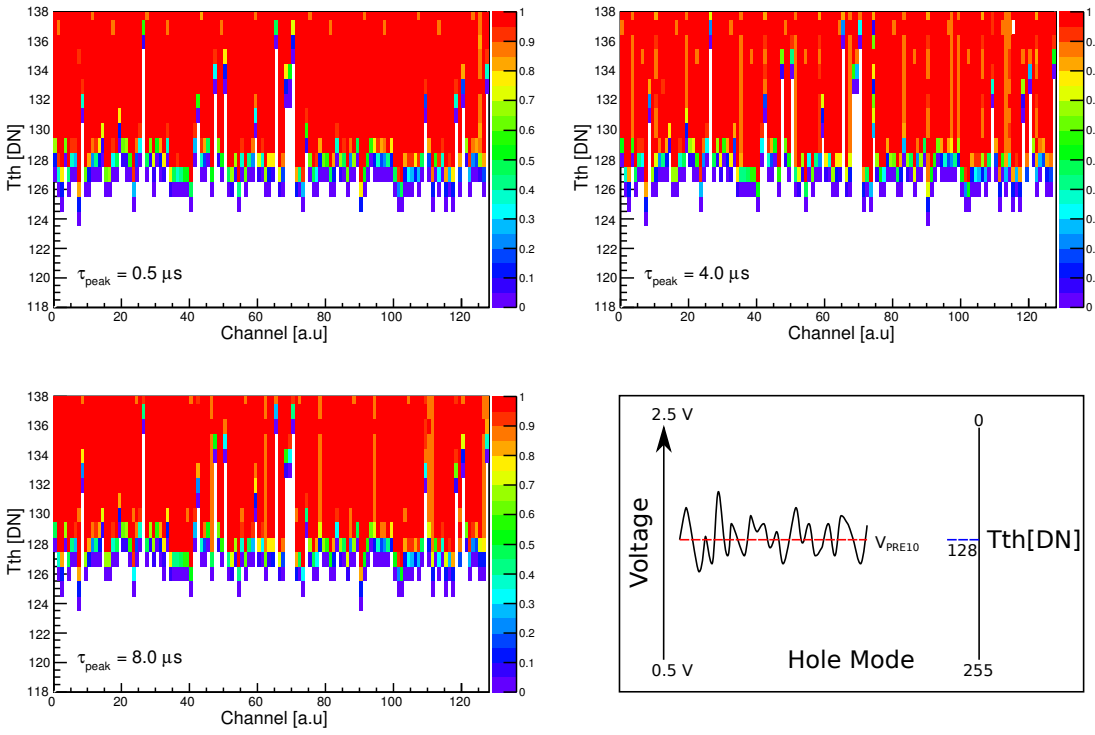


Figure 6.28: A plot of the normalised number of hits measured per second for each channel for three different peaking times in hole mode. A large value of Tth represents a small threshold voltage resulting in many hits.

for smaller DN values. When $Tth > 138$ DN, the number of hits per second with hit-bit equal to 1 reaches a maximum. The threshold setting Tth at which a channel transitions from mainly hits with hit-bit = 1 to hit-bit = 0 occurs at different values of Tth for different channels. This difference from channel to channel occurs due to the misalignment between the $\times 10$ gain amplifier reference voltage V_{PRE10} and the threshold voltage Tth for each channel. The time comparator threshold scans show that the threshold conditions are different for each channel. It is expected that changing the peaking time should have very little effect on the observed time comparator behaviour as the time comparator does not receive shaped signals. Small differences may appear due to different shaping time-constants because of the different energy comparator trimming at different time-constants.

Trimming Offset Scan

Fine trimming of the DC baseline voltage, at the input of the time comparator for each channel, is possible using the trim DAC (digital to analog converter) at the

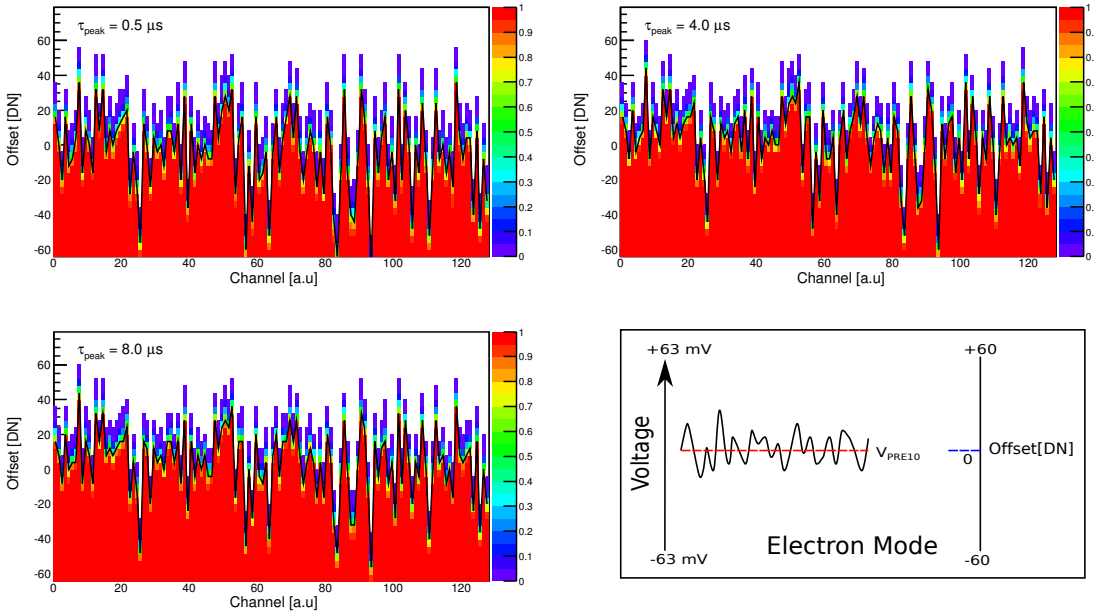


Figure 6.29: The trim DAC offset was scanned from -60 to 60 digital number (DN) for a fixed threshold $Tth = 128$ DN for electron mode (negative going signal). The black line represents the DAC offset value at which the number of hits was half of the maximum. A positive offset adds a small voltage to V_{PRE10} which raises V_{PRE10} above Tth resulting in no hits at large positive offset values.

output of the $\times 10$ gain amplifier $PRE10$ and before the time comparator input. The trim DAC is programmed via an 8-bit number (0-255 DN), resulting in a negative or positive offset value that is added to or subtracted from the baseline of the $\times 10$ gain amplifier output. The value of the offset is the same as was previously defined for the energy comparator in section 6.5.3 (1 DN = 1.05 mV).

The result of keeping the values of V_{PRE10} and Tth fixed at 128 DN (1.5 V) and scanning the offset setting for each channel is shown in Figure 6.29 for electron mode and Figure 6.30 for hole mode. Only offset values corresponding to an offset of $\pm$ 60 DN are shown. For electron mode, the input signal to the time comparator is negative going and a negative offset decreases the voltage V_{PRE10} which results in more hits. For hole mode, the time comparator input signal is positive going and a positive offset increases the voltage V_{PRE10} which results in more hits.

To accurately align the two signals it is crucial to determine the offset value at which the number of measured hits is half of the maximum. The back line in Figure 6.29 and Figure 6.30 indicates the offset value for each channel that resulted in the number of hits being closest to half of the maximum number of hits. The procedure

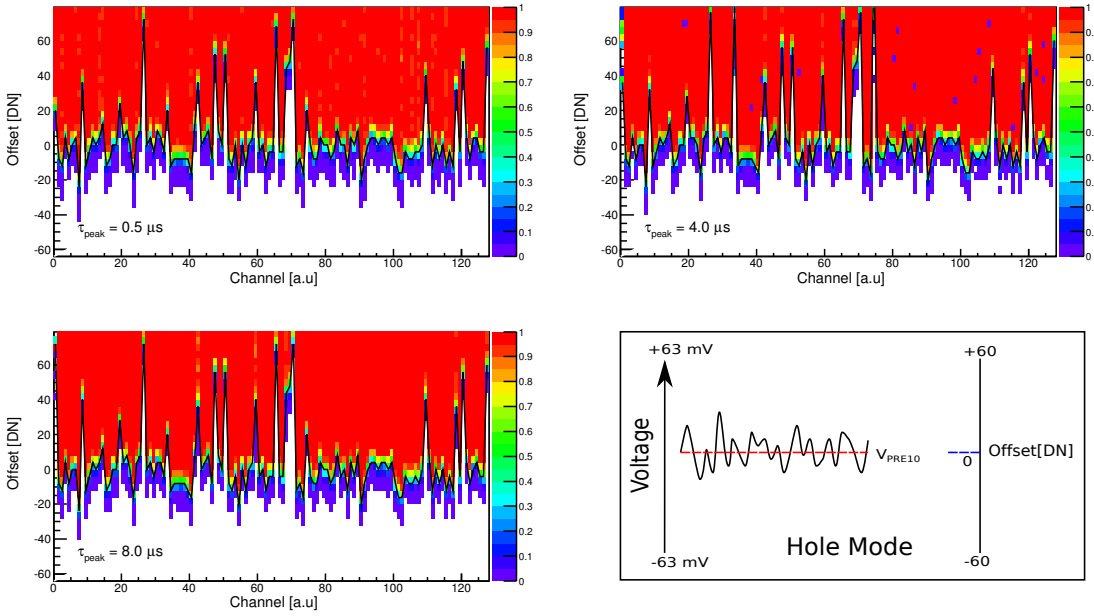


Figure 6.30: The trim DAC offset was scanned from -60 to 60 digital number (DN), for a fixed threshold $Tth = 128$ for hole mode (positive going signal). The black line represents the DAC offset value at which the number of hits was half of the maximum. A positive offset adds a small voltage to V_{PRE10} which raises V_{PRE10} above Tth resulting in many hits at large positive offset values.

used to determine the offset value for a single channel is shown in Figure 6.31 where the offset corresponding the middle of the s-curve was stored for each channel.

6.7.3 Results

The stored offset values can be used to produce a configuration file that should align the baseline voltage V_{PRE10} and the threshold voltage Tth for each channel. Just as before, a scan of the threshold from Tth = 0-255 DN was repeated whilst keeping all registers constant (V_{SHA10} = 1.5 V ± offset, Eth = 1.5 V and V_{PRE10} = 1.5 V) but also applying the unique trim offset value to V_{PRE10} for each channel. The results of such a measurement using the trim DAC offset values is shown in Figure 6.32 and Figure 6.33 for both modes.

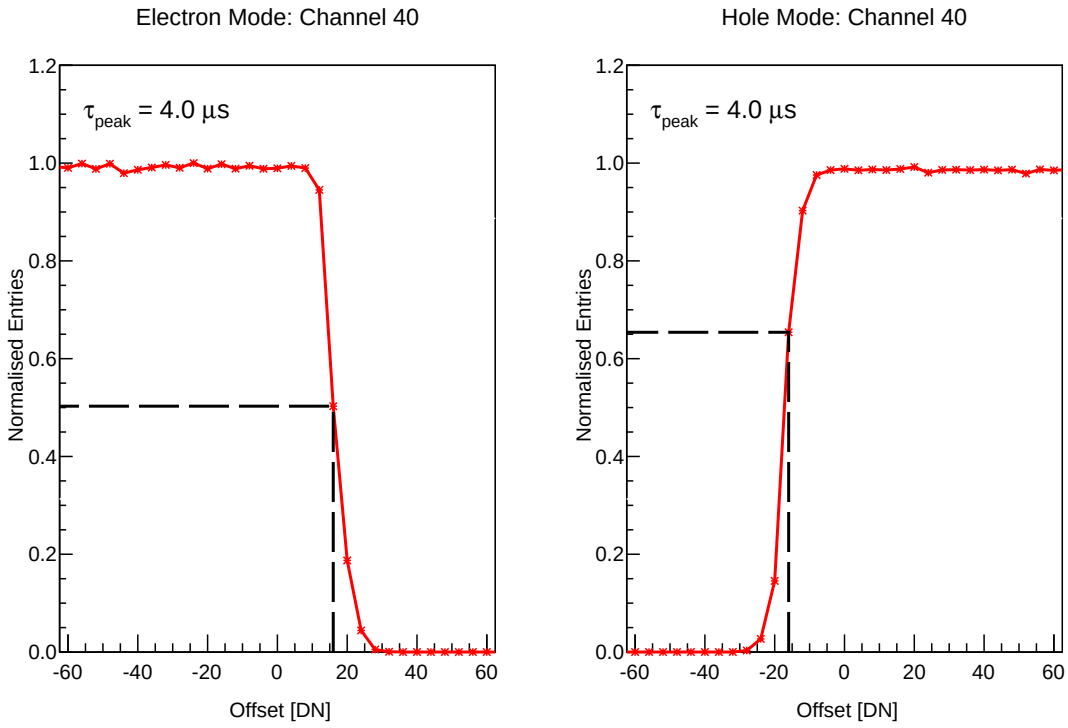


Figure 6.31: An example of offset trimming for channel 40 for electron and hole mode. The offset value at which the number of entries is closest to half of the maximum is stored for each channel. The black line indicates the selected offset value and the associated normalised number of entires. For electron mode the signal at the comparator's inverting input is negative going, whereas the signal is positive going for hole mode.

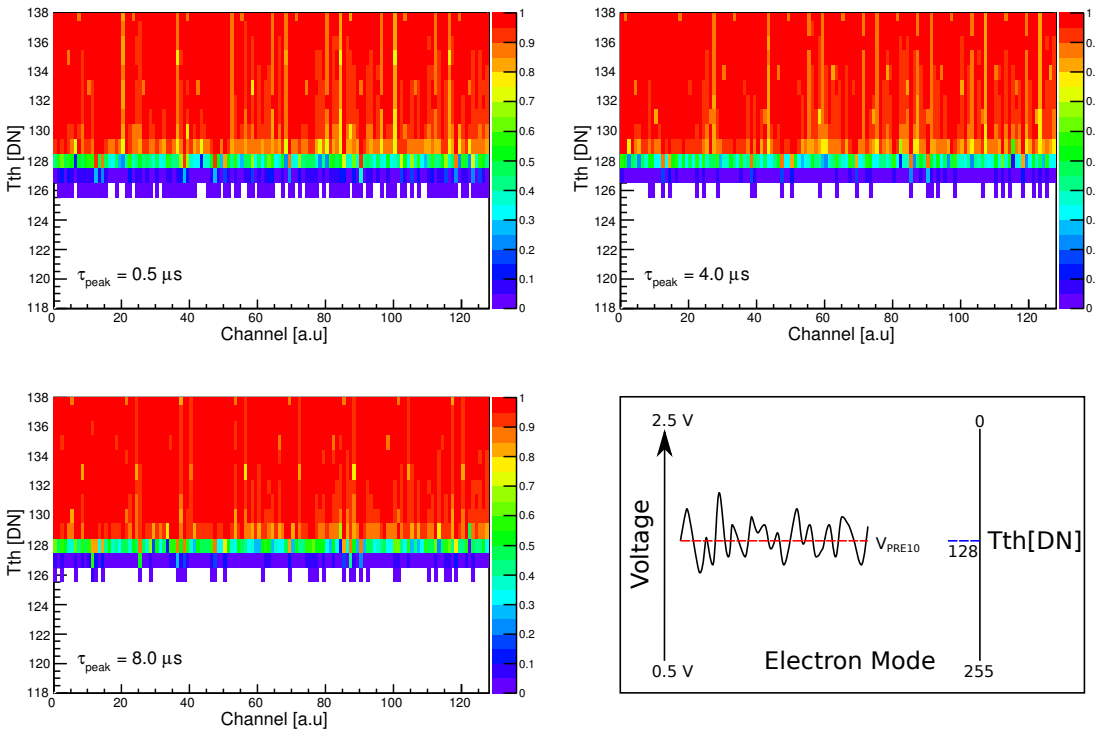


Figure 6.32: A plot of the normalised number of hits measured per second for each channel for three different peaking times in electron mode after trimming. A large value of Tth represents a small threshold voltage resulting in many hits.

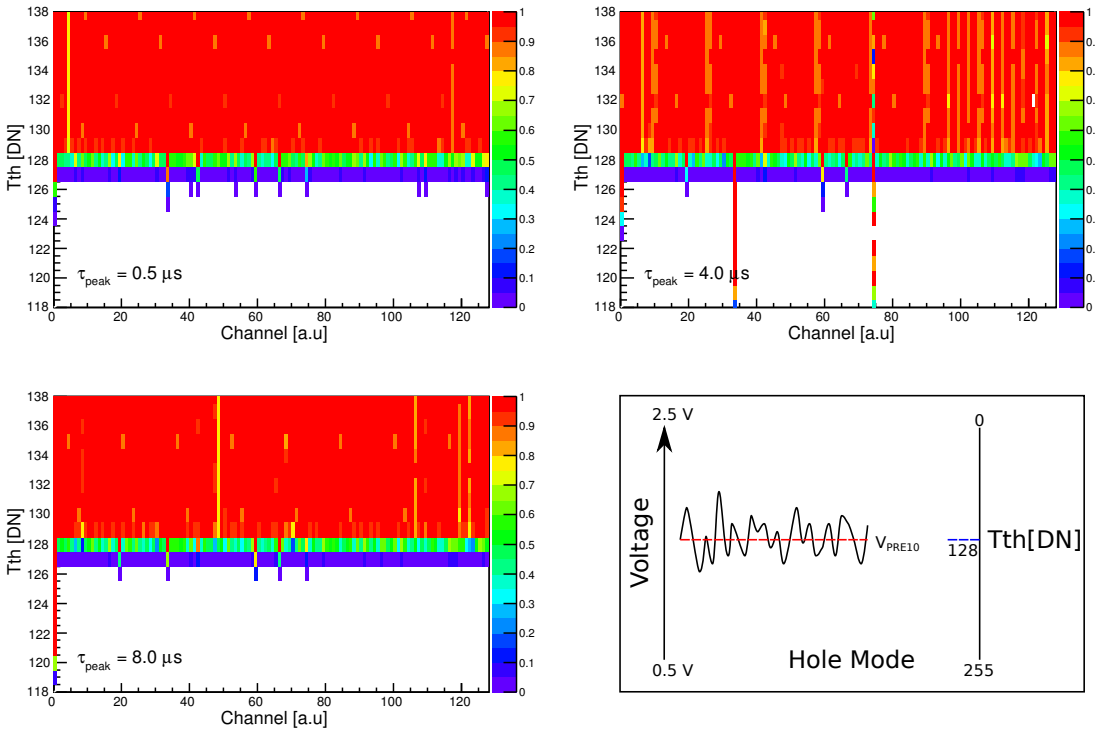


Figure 6.33: A plot of the normalised number of hits measured per second for each channel for three different peaking times in hole mode after trimming. A large value of Tth represents a small threshold voltage resulting in many hits.

After trimming the time comparator threshold, it is clear that both modes perform well with the vast majority of channels having been aligned as the number of hits is approximately half of the maximum when $Tth = 128$ DN. A value of $Tth = 1$ DN corresponds to a 24.8 keV signal at the preamplifier input (small but negligible difference compared to energy comparator as no shaper contribution to timestamp signal). Therefore any hits recorded at $Tth = 127$ or 126 DN correspond to noise levels of approximately 25 and 50 keV.

The number of channels that recorded a hit at each threshold is shown in Table 6.9. For electron mode, there are no channels with a noise level exceeding 75 keV. The 0.5 μs peaking time exhibits a slightly larger noise than the 4.0 and 8.0 μs peaking times, which is probably due to poorer energy comparator trimming for the 0.5 μs peaking time data set. For $\tau_{peak} = 4.0$ and 8.0 μs, the majority of channels have a maximum noise level between 25 keV and 50 keV. For hole mode, channel 0 was not trimmed correctly for all peaking times and two other channels failed to be trimmed for a peaking time of 4.0 μs. Ignoring the untrimmed channels, the

three peaking times show a similar noise level with all but two channels recording a maximum noise level less than 75 keV for all peaking times. The 4.0 and 8.0 μs peaking times appear to result in marginal reduction in noise compared to the 0.5 μs data.

The comparator required for timestamping purposes has been trimmed for three peaking times for both modes and a timestamp threshold setting of $Tth = 125$ DN (75 keV) should result in only one or two channels firing due to high noise levels or mistrimming.

Table 6.9: Summary of timestamp comparator threshold trimming results after trimming for a threshold of 128 DN. The number of channels that recorded hits is shown for each threshold setting in units of keV and digital number (DN).

		Electron Mode			Hole Mode		
		Peaking Time [μs]					
		0.5	4.0	8.0	0.5	4.0	8.0
Threshold [DN]	Threshold [keV]	Num. Hit Channels					
128	0	100	100	100	100	100	100
127	25	100	100	100	100	100	100
126	50	92	28	33	11	6	6
125	75	0	0	0	2	4	1

6.8 Shaping Time-Constant

The shaping time-constant is a programmable parameter that determines the time at which the shaper output pulse peaks and has important consequences for sampling the pulse height as well as noise filtering. Sampling a pulse before the peak will result in measurement of the rising edge. It is important that the sampling time is programmed such that a pulse is always sampled after the peak to ensure the maximum pulse height is sampled.

The shaping time-constant can be varied from 0.5 to 8.0 μs in increments of half a microsecond by selecting a digital number from 0-15 (4-bit binary number), which controls a set of switches to adjust the differentiator and integrator capacitances. The shaper response has been tested for different time-constants to verify that the true peaking time is the same as the programmed shaping time-constant. Further testing has been conducted to investigate the dependency of the noise on the programmed shaping time-constant. It is expected that sampling after the peaking time should return the same ADC value for the pulse height due to the peak-hold circuit. An analysis of ADC values obtained by sampling only after the peak is also presented.

6.8.1 Measurement Technique

The shaping time-constant is programmed via the first 4-bits of register four, the remaining 4-bits of the register are used to programme the DAPB which allows the pulse to be sampled at different times. There are two techniques by which the response of the shaper, to a fast rising edge from the preamplifier can be tested. The first technique (DAPB scan), where the full profile of the shaped pulse is sampled, is outlined in Figure 6.34. This allows the pulse amplitude to be measured at one microsecond intervals, starting two clock cycles after the shaper output begins to rise. The time τ_{peak} at which the peak amplitude is measured, can be compared with the programmed shaping time-constant. The DAPB scan measurement can be achieved by setting a fixed value for the shaping time-constant and altering the value of the sampling point (DAPB + 2 μs) so as to sample the pulse before, during and after the peak. The peak-hold circuit of the ASIC will always store the maximum pulse amplitude meaning the decay tail (after the peak) of the shaper output pulse cannot be viewed. The rising edge (before the peak) of the pulse can be profiled using this technique to determine the peaking-time to the nearest microsecond.

Figure 6.35 shows another possible technique (pulse width scan) for measuring

Table 6.10: The range of parameters used for testing the shaping time-constant using the DAPB scan technique.

DAPB [μs]	τ_{peak}[μs]	PHRST [μs]	Eth [DN]	V_{test} [DN] [MeV]	Width [μs]	Delay [μs]
0.0 - 15.0	0.5 - 8.0	15.0	160	[64] [32.57]	DAPB + 2	600

Table 6.11: The range of parameters used for testing the shaping time-constant using the pulse width scan technique.

DAPB [μs]	τ_{peak}[μs]	PHRST [μs]	Eth [DN]	V_{test} [DN] [MeV]	Width [μs]	Delay [μs]
15.0	0.5 - 8.0	15.0	160	[64] [32.57]	0.5-10.0	600

the peaking time of a shaped pulse by varying the pulse width and keeping all other registers fixed. The pulse width scan method allows the DAPB to be set to the maximum and only the pulse width to be changed. Injecting a test pulse that is shorter in duration than the shaping time-constant will ensure that the rising edge is sampled. When the width of the test pulse is greater than or equal to the shaping time-constant then the peak amplitude will be observed. The range of settings used for the DAPB scan measurement are outlined in Table 6.10 and the settings used for the pulse width scan are shown in Table 6.11.

The shaping time-constant has been tested using both the techniques outlined above, DAPB scan and pulse width scan. For the DAPB scan, the full range of possible shaping time-constants has been tested for all possible sampling points where the DAPB has been scanned from the minimum value (DAPB = 0 μs) to the maximum (DAPB = 15 μs) in increments of 1 μs (15 data sets taken for each shaping time-constant). The time at which the shaped pulse is sampled is given by DAPB + 2 μs which allows the pulse to be sampled between the range 2-17 μs after the pulse is synchronised on the rising clock edge. For every data set, the falling edge of the test pulse occurred after the expected peaking time and before the preamplifier reset signal so that the measurement is unaffected by termination of the test pulse (section 6.3.3 explains where to position the test pulse falling edge). For the pulse width scan, the pulse width has been scanned from 0.5 μs to 10 μs, in increments of 0.5 μs, for every programmable shaping time-constant. For the pulse width scan, the DAPB setting was set to the maximum value of 15 μs for all measurements. For both techniques, the shaper response has been tested for a single ASIC for both electron mode and hole mode in which all channels received 512 test pulses.

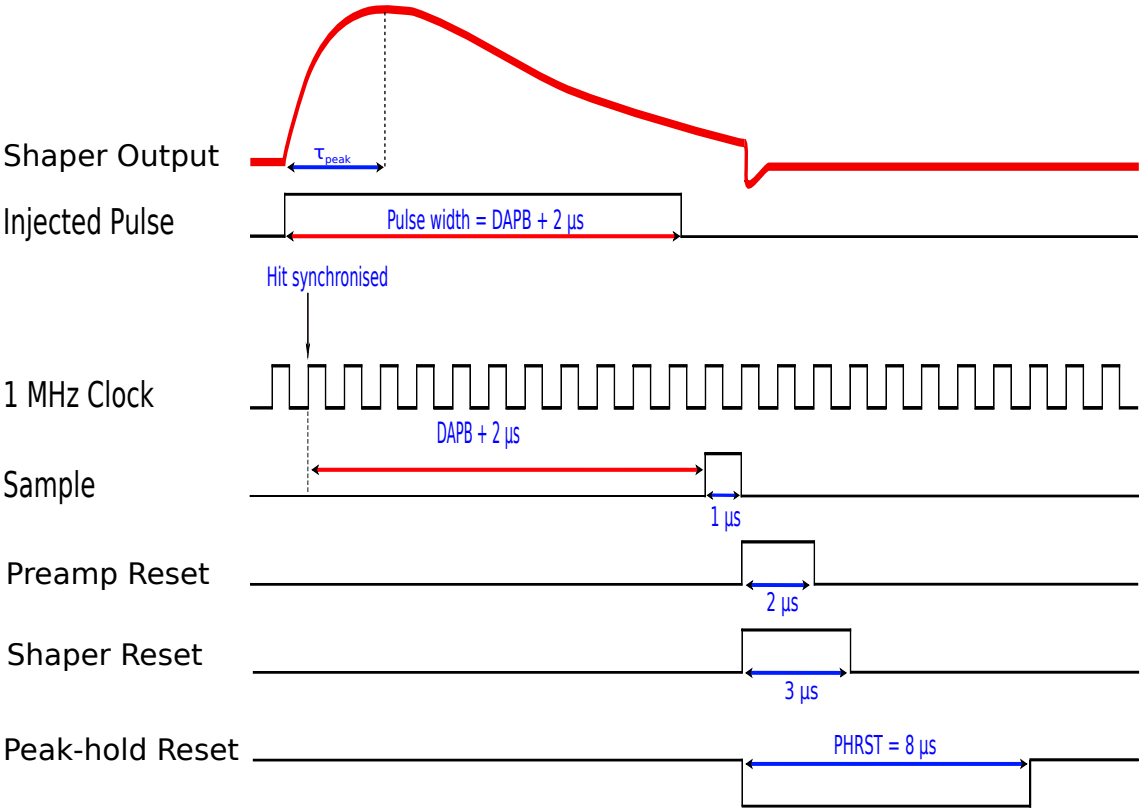


Figure 6.34: A schematic of the ASIC timing logic showing how the peaking time τ_{peak} of a signal at the shaper output is observed. An approximation of the profile of the shaper output signal is included for representative purposes. The lines in red indicate parameters of the readout timing that can be programmed. A fixed shaping time-constant is selected and the DAPB setting (sampling point = DAPB + 2 μs) is scanned from the minimum (0 μs) to the maximum (15 μs). This allows the signal to be sampled at different points, so that the rising edge is observed for $t < \tau_{peak}$. The width of the injected test pulse is selected such that it is larger than the shaping time-constant and the falling edge occurs before the preamplifier reset.

6.8.2 Results

Figure 6.36 shows the result of using both techniques to examine the shaper output pulse for a shaping time-constant of 5 μs for all 128 channels of an ASIC in electron mode. At each sampling time and pulse width, the mean ADC has been calculated for all channels and is plotted as a blue line. The average of all channels (red line) has then been calculated via the following expression

$$\overline{x} = \frac{\sum_{i=0}^{N} x_i}{N} \ , \tag{6.7}$$

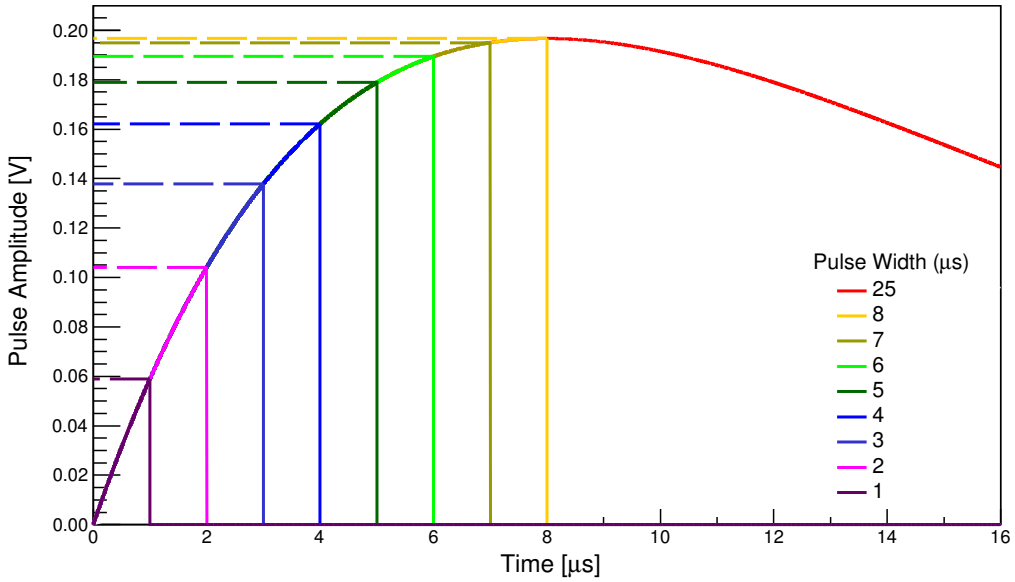


Figure 6.35: Scanning the width of the injected test pulse allows the rising edge of the shaped pulse to be observed when using pulse widths smaller than the programmed shaping time-constant. The theoretical pulse amplitude is shown for a range of pulse widths for an ideal shaper response with a shaping time-constant of 8 μs. The dashed lines show the peak amplitude corresponding to each pulse width. The peak amplitude is observed when the pulse width is equal to the peaking time.

where $\overline{x}$ is the mean ADC of all the channels at a given DAPB value or pulse width, N is the number of channels per ASIC and x_i is the mean ADC of channel i for a given pulse width or DAPB value. The ADC value obtained from averaging all 128 channels is plotted for each sampling time and pulse width value as a red line. The error bars of 3σ are calculated according to

$$\sigma = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(x_i - \overline{x})^2} \ , \tag{6.8}$$

where the symbols have the same meaning as the previous equation. Figure 6.36 demonstrates that all 128 channels of the ASIC have a measured mean ADC value that is within 3σ of the average value of all 128 channels when using either the DAPB scan or pulse width scan technique.

The measured mean ADC increases with sampling time until the peak occurs after which the mean ADC value remains constant due to the peak-hold circuit. The rising edge of the pulse is clearly seen between 2 μs and 5 μs for the DAPB scan

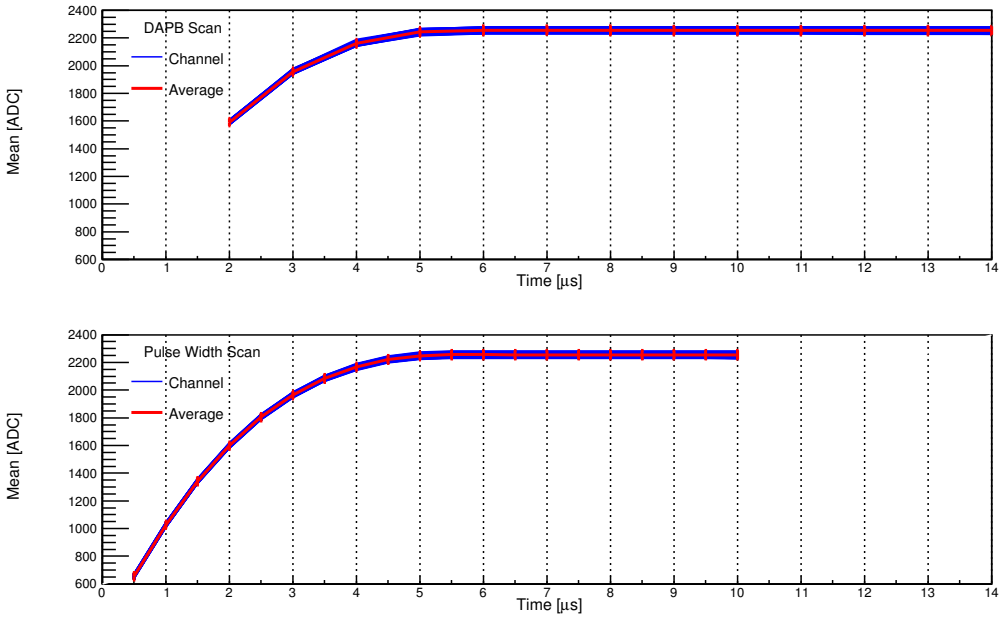


Figure 6.36: A plot showing the measured mean ADC of all 128 channels in blue for a shaping time-constant of 5 μs for two different measurement techniques. The average of all 128 channels is shown in red with 3σ error bars.

and between 0.5 μs and 5 μs for the pulse width scan. By scanning the pulse width it is possible to achieve a better time resolution than using the DAPB scan and it allows measurements of the pulse amplitude to be carried out for $t < 2\mu$s. The 1 MHz clock of the channel control logic limits the sampling point resolution to 1 μs for the DAPB scan. Unlike the pulse width scan, the DAPB scan actually requires changing of the DAPB register values and as such directly tests the register four settings. Therefore both techniques have their merits and it is useful to cross check the results of both measurements.

Figure 6.37 shows a detailed plot of the pulse profile focussing closely on the region in which the peak amplitude occurs. Inspecting the region around the peak it is clear that the time at which the pulse peaks is actually larger than the programmed shaping time-constant. It is expected that the peak would occur at t = 5 μs but the data shows the peak amplitude at 6 μs for the DAPB scan and at 5.5 μs for the pulse width scan. The two measurements yield a similar profile and agree that the pulse has a peaking time between 5 and 6 μs. The

As it is not possible to view the profile of the pulse's decay tail, an ideal calculation for the shaper response has been included for comparison. The full profile of the ideal shaper output has been calculated for every programmable shaping time-

constant, using the capacitance and resitance values specified for the R^{3}B ASIC with equation 5.15. Figure 6.38 displays the averaged data for both measurement techniques (3σ error bars) accompanied by the theoretical pulse profile that peaks at t = 5 μs where all data has been normalised. The two measurements show a strong agreement with each other for all measured data points and closely follow the profile of the ideal shaper. For a shaping time of 5 μs the measured pulse amplitude at t = 5 μs is more than 99% of the amplitude measured for t $\geq$ 5.5 μs as shown in Figure 6.39.

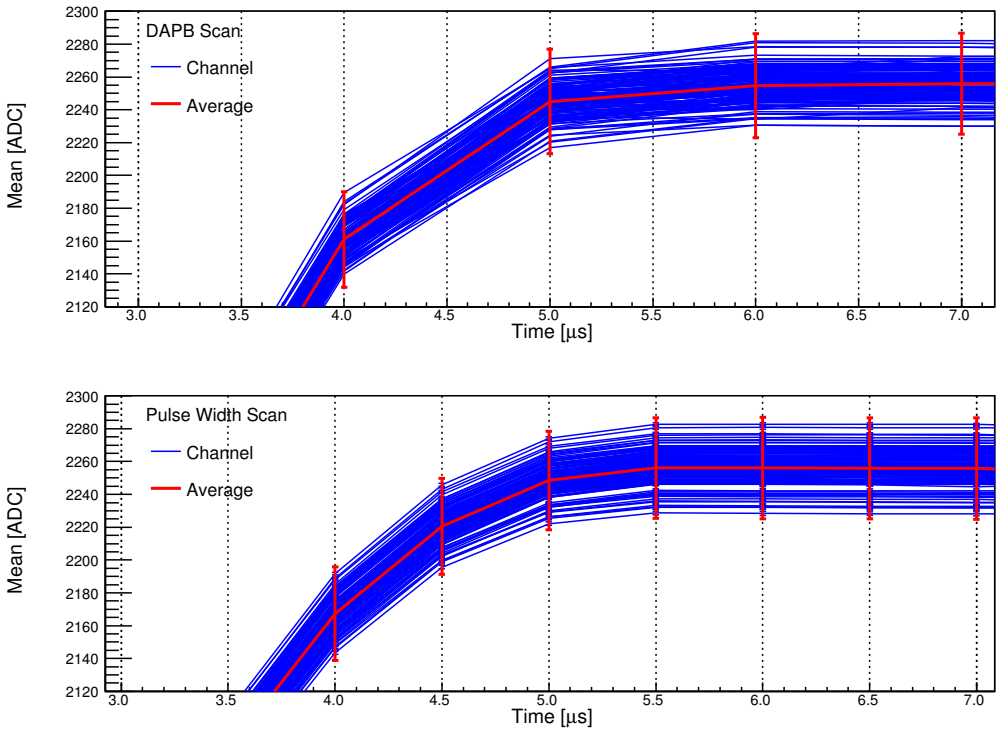


Figure 6.37: A plot for a shaping time of 5 μs showing the pulse profile around the peak amplitude. The data for each channel is shown in blue and the average of all 128 channels is shown in red with 3σ error bars.

The DAPB scan and pulse width scan have been used to test all possible shaping time-constants for both electron and hole mode. The results for each integer time-constant are shown in Appendix A.2. The results show, most clearly for smaller shaping times (1-4 μs), that the true peaking time typically occurs later than the programmed shaping time-constant (data in green and blue rises later than ideal calculation in red). The data points from the pulse width scan, which are every 0.5 μs, shows that the pulse always peaks within 0.5 μs after the programmed shaping time-constant. As was observed for the 5 μs shaping time in electron mode, all data

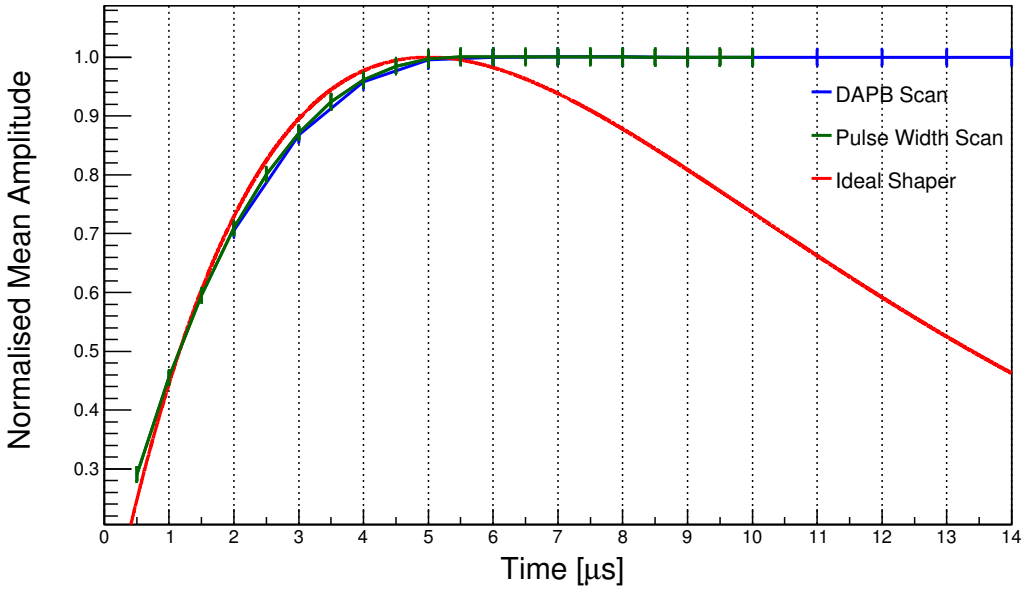


Figure 6.38: A plot for a shaping time of 5 μs showing the normalised pulse amplitude versus time for the two measurements as well as an ideal pulse profile.

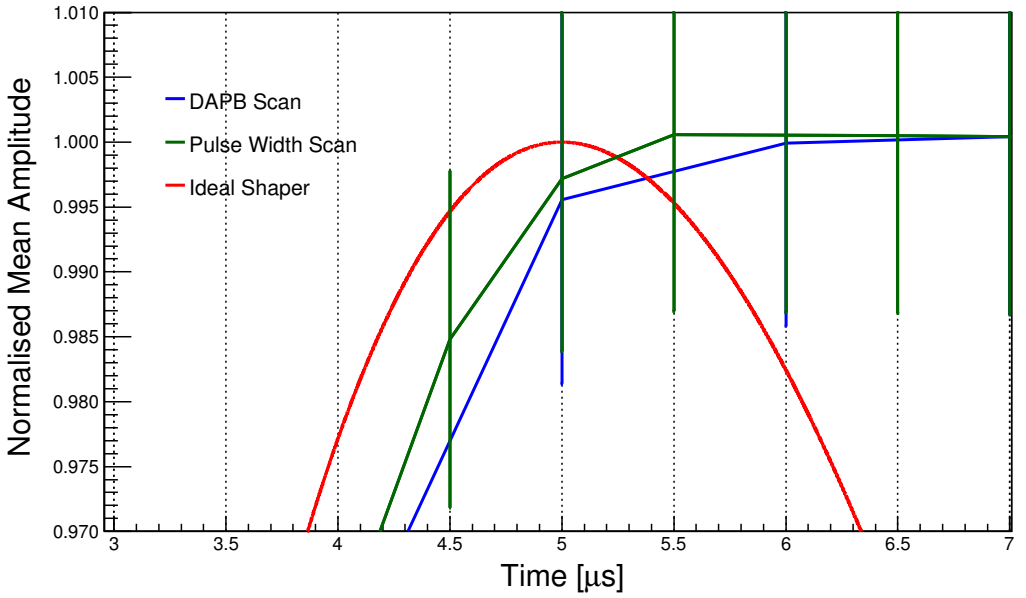


Figure 6.39: For a shaping time of 5 μs, the pulse profile reveals the peaking time occurs at 5.5 μs and 6 μs for the pulse width and DAPB scan measurements, respectively. The pulse height measured at t = 5 μs is about 99.5% of the true maximum pulse amplitude.

sets show that the pulse amplitude measured at the expected peaking time (i.e. t = 3 μs for shaping time-constant of 3 μs) is about 99% or more of the maximum amplitude obtained by sampling after the pulse has peaked.

6.8.3 Shaper Capacitance Tolerances

As discussed in section 5.5.1, the values of the differentiator and integrator time-constants influence the time at which the shaper output pulse reaches its maximum amplitude. The ASIC specifications outline the values of the capacitors and resistors which make up the shaper network. For a programmed shaping time-constant of 8 μs all of the switches of the CR-RC network are closed such that the differentiator and integrator capacitances are given by C_{diff} = 20.80 pF and C_{int} = 8.00 pF (see Figure 5.16 circuit diagram of R^3B shaper). The ratio C_{diff}/C_{int} influences the amplification of the signal and the time-constants are given by $\tau_{diff} = R_{diff}C_{diff}$ and $\tau_{int} = R_{int}C_{int}$. Altering the values of the capacitances thus changes the time-constants and can alter the time at which the signal peaks. The ASIC specifications quote the shaper capacitances to have a tolerance of 15%. Figure 6.40 shows the expected peaking time for C_{diff} = 20.80 pF and C_{int} = 8.00 pF as well as the upper and lower limits due to varying capacitances.

The quoted tolerance of the capacitances indicates a peaking time of 8 $\pm$ 1.2 μs. The measured data reveals that the true values of the capacitances is well within this 15% tolerance limit as the observed peaking time differs by less than 0.5 μs from the programmed value. To ensure that the maximum pulse amplitude is always sampled, it is advisable to sample at least 1 μs after the expected peaking time. For example, when using a programmed shaping time-constant of 4 μs the DAPB should be set to sample at t $\geq$ 5 μs to guarantee that sampling occurs after the peak.

6.9 Sampling Time and Peaking Time

Sampling after the peak ensures that the peak-hold capacitor stores the maximum amplitude. It is expected that the functionality of the peak-hold circuit should be unaffected by the time at which the pulse is sampled. The same ADC value should be returned regardless of whether the sampling time was just after the peaking time or at the maximum value of 17 μs from when the rising edge of the pulse was synchronised.

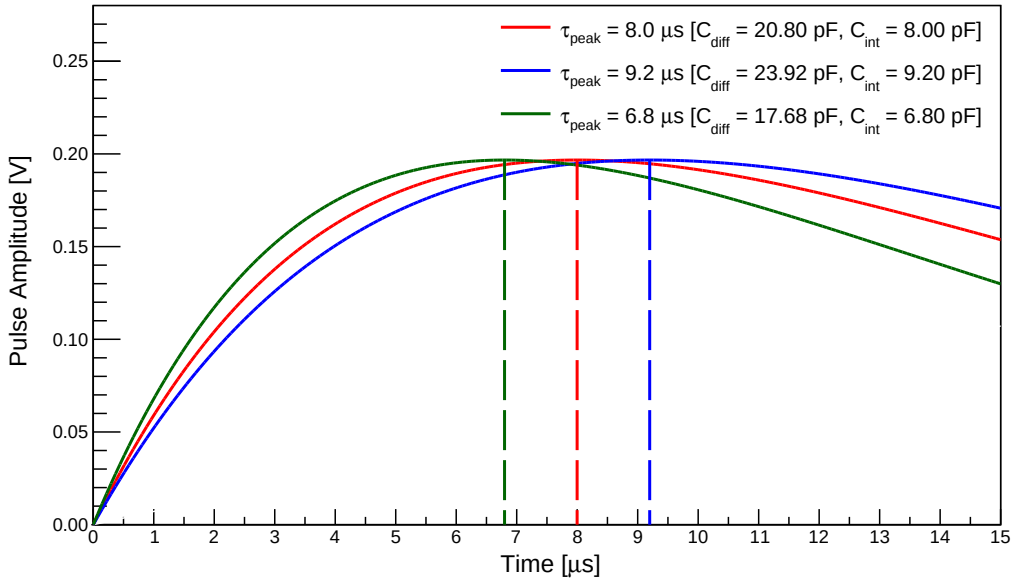


Figure 6.40: Three ideal shaper responses showing variation in peaking time for a 15% increase or decrease in shaper capacitance relative to the specified capacitances. The shaper output signal has been calculated using exact differentiator and integrator capacitances for an 8 μs shaping time-constant (red). The upper (blue) and lower (green) peaking time limits according to the quoted tolerances are plotted. The calculations were performed using a square wave of amplitude 0.206 V at the shaper input (0.1 V test input at preamplifier results in 0.206 V square wave at shaper input).

6.9.1 Measurement Technique

The variation in measured pulse amplitude has been tested, by only sampling after the peaking time. All programmable shaping time-constants have been tested. It is important to understand the variation in measured amplitude and noise with respect to the sampling time. Increasing the sampling time means the preamplifier, shaper and peak-hold circuit resets occur later, which results in a longer dead time for a channel. The sampling time will determine the time at which the signal from the peak-hold circuit is passed to the analogue multiplexer and thus influences how long the peak-hold capacitor remains charged. The peak-hold capacitor is always reset prior to the arrival of the next pulse. The following tests have been conducted using the register settings outlined in Table 6.12.

Table 6.12: The ASIC parameters used to sample the shaper output after the peaking time.

DAPB [μs]	τ_{peak}[μs]	PHRST [μs]	Eth [DN]	V_{test} [DN] [MeV]	Width [μs]	Delay [μs]
(τ_{peak}+1) - 15.0	0.5 - 8.0	15.0	160	[64] [32.573]	τ_{peak} + 0.5	600

The ASIC response for different sampling times has been tested by injecting a fixed number of test pulses into each channel and varying the sampling time whilst fixing the shaping-time constant. A total of 512 test pulses were injected into each channel for every sampling time for every shaping time-constant. All shaping time-constants have been tested by sampling from 1 μs after the expected peaking time to the maximum of DAPB+2 = 17 μs. The mean ADC of the injected pulse amplitude, obtained by sampling only after the peaking time, has been determined for every shaping time-constant for every possible sampling time.

6.9.2 Amplitude vs Sampling Time Results

The mean ADC vs sampling time data for six different shaping time-constants is shown in Figure 6.41 for electron mode. The mean ADC of the 512 test pulses is plotted at each sampling time for all 128 channels. The data confirms that there is very little alteration in the measured mean ADC due to changing the sampling time. The variation in ADC is shown to be of the order 2-3 ADC counts for the electron mode data. The equivalent data for the hole mode setting is shown in Figure 6.42. For the hole mode setting, there is a more noticeable change in the ASIC's response due to changes in the sampling time. The hole mode data shows that some time-constants yield a mean ADC value that gradually increases with increasing sampling time. For example, the shaping time-constant of 7 μs has been tested for both modes by using sampling times ranging from 8-17 μs. A 7 μs time-constant exhibits a measured mean ADC that gradually increases at larger sampling times for the hole mode setting whilst the measured ADC remains relatively unchanged for the same measurement in electron mode.

To gain a clearer understanding, the average channel behaviour has been calculated for all shaping time-constants at every sampling time. The result of calculating the mean ADC for the average of all channels is plotted in Figure 6.43a and Figure 6.43b for the two modes. The difference in performance between the two modes is now shown more clearly. On average, the electron mode data shows a fluctutation in the mean ADC of $\pm$ 2-3 ADC, which is consistent with the reproducibility tests

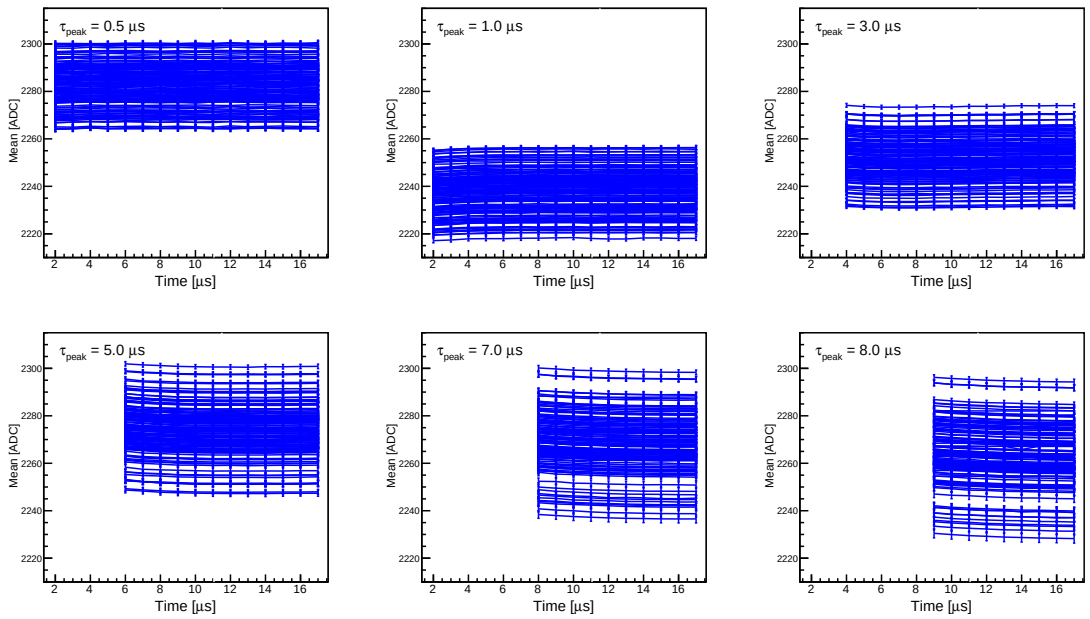


Figure 6.41: The mean ADC is plotted against sampling time for each channel for six different shaping time-constants. Only sampling times that occur after the peaking time are shown. One channel is one blue line. Data is for electron mode.

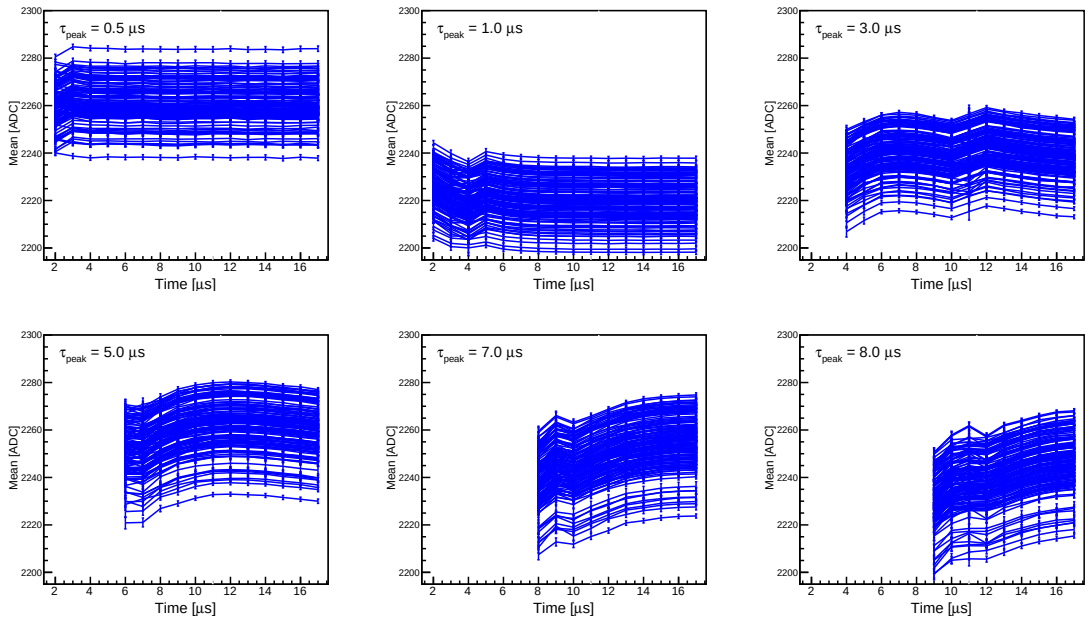
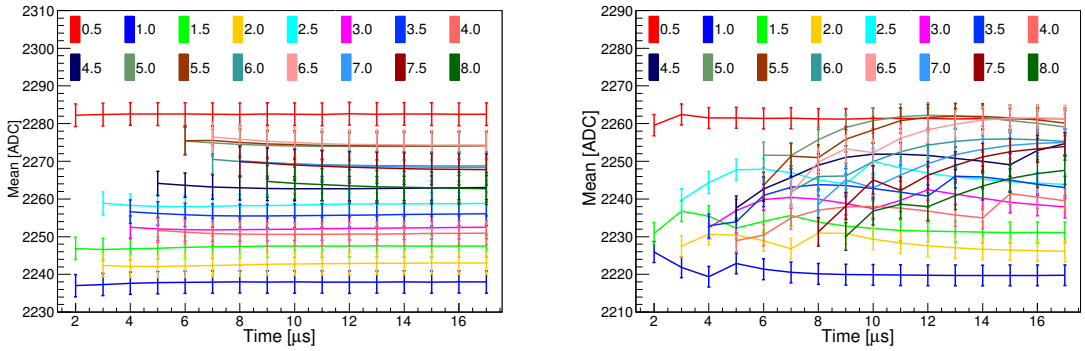


Figure 6.42: The mean ADC is plotted against sampling time for each channel for six different shaping time-constants. Only sampling times that occur after the peaking time are shown. One channel is one blue line. Data is for hole mode.



(a) Electron mode.

(b) Hole mode.

Figure 6.43: The mean ADC for each of the 128 channels has been used to calculate the average channel behaviour for every possible shaping time-constant. The average channel ADC is plotted versus sampling time for each shaping time-constant. The errors shown are $\sigma/3$, so that error bars can be distinguished for different data sets.

in section 6.2. The hole mode shows a maximum difference of $\approx$ 20 ADC with the maximum ADC usually observed for large sampling times of 10-17 μs.

A data set taken for a fixed shaping time-constant with a specified sampling time can be directly compared with another data set using the same shaping time-constant with a different sampling time when using electron mode. For example, an electron mode data set using τ_{peak}= 5 μs and DAPB = 10 μs can be directly compared with another data set using τ_{peak}= 5 μs and DAPB = 15 μs. The same statement cannot be made for the hole mode setting.

6.9.3 Noise vs Sampling Time Results

The calculated RMS ADC of the pulse amplitudes measured for each channel is shown for different sampling times for electron mode in Figure 6.44 and hole mode in Figure 6.45. The RMS ADC is shown for every channel as a blue line. For electron mode, the RMS ADC remains broadly unchanged due to changes in sampling time. The hole mode data shows that for some shaping time-constants the deviation is larger when sampling just after the peaking time and gradually decreases towards a minimum value at the largest sampling times.

The noise level for an average channel has been calculated for both modes and is shown in Figure 6.46a and Figure 6.46b. The noise level does not change with sampling time for electron mode but for hole mode a small reduction in the noise is observed for larger sampling times for some shaping time-constants. The largest

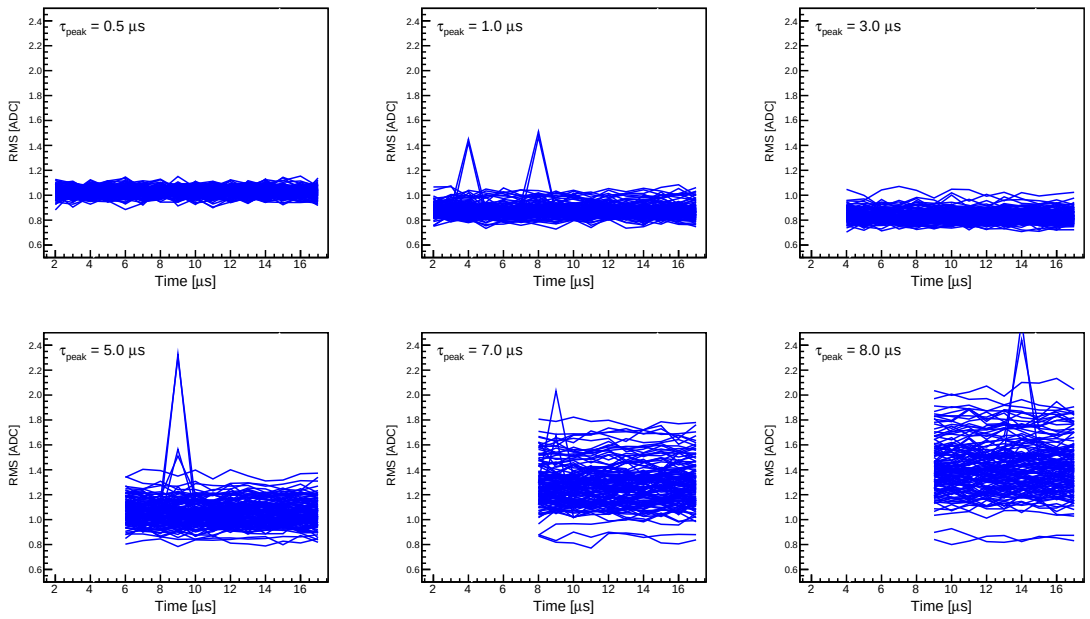


Figure 6.44: The RMS of the measured amplitudes of 512 pulses is shown for the different shaping time-constants and sampling times in electron mode for each individual channel.

noise levels are seen for the hole mode setting for integer values of shaping time-constant when the sampling time is set so that the pulse is sampled just after the peaking time. The half-integer shaping time-constants show an average channel noise that is consistent with the values measured for electron mode.

6.9.4 Noise vs Shaping Time-constant

In section 5.5.1, the concepts of pulse shaping were introduced as well as the dependency of noise on the selected shaping time-constants. The electron mode data presented in Figure 6.46a clearly demonstrates that the noise level varies for different shaping time-constants. The data in Figure 6.46b exhibits a similar relationship however some integer shaping time-constants appear to suffer from greater noise when sampling just after the peaking time. The largest noise is observed for both modes for a shaping time-constant of 8.0 μs.

Taking the data in Figure 6.46, it is clear that the maximum sampling time of 17 μs results in lower values of RMS noise for the hole mode configurations, whereas the RMS noise in electron mode appears to be unaffected by changes in sampling time. The result of plotting the RMS ADC for a sampling time of 17 μs against shaping time-constant for electron and hole mode is shown in Figure 6.47. This

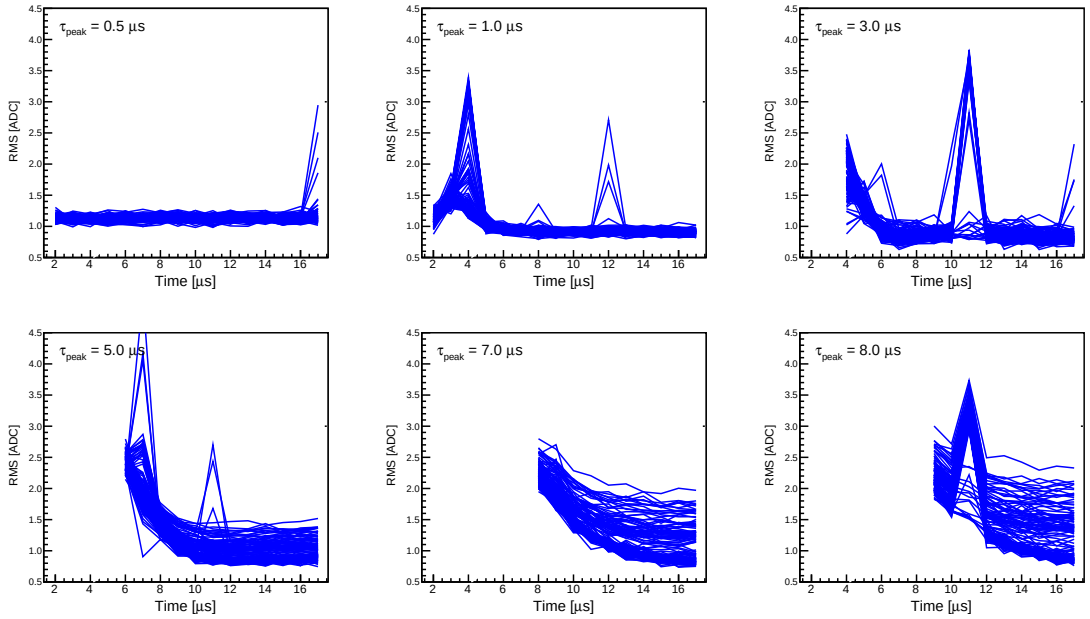
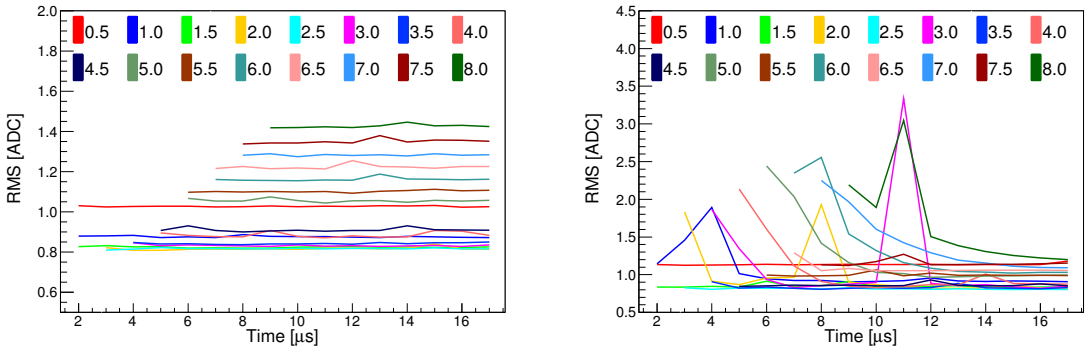


Figure 6.45: The RMS ADC of the measured amplitudes of 512 pulses is shown for the different shaping time-constants and sampling times in hole mode for each individual channel.



(a) Electron mode.

(b) Hole mode.

Figure 6.46: The RMS ADC of an average channel is plotted versus sampling time for each shaping time-constant.

represents the average channel noise when using the maximum sampling time. For both electron and hole mode, the minimum RMS noise is observed for shaping time-constants in the range 1.5-3.0 μs and a larger noise is observed at 0.5 and 8.0 μs. The minimum average channel noise in electron mode was measured to be 0.81 ADC for a shaping time-constant of 2.0 μs. For hole mode, the minimum average channel noise was 0.80 ADC for a shaping time-constant of 2.5 μs. The largest RMS noise value

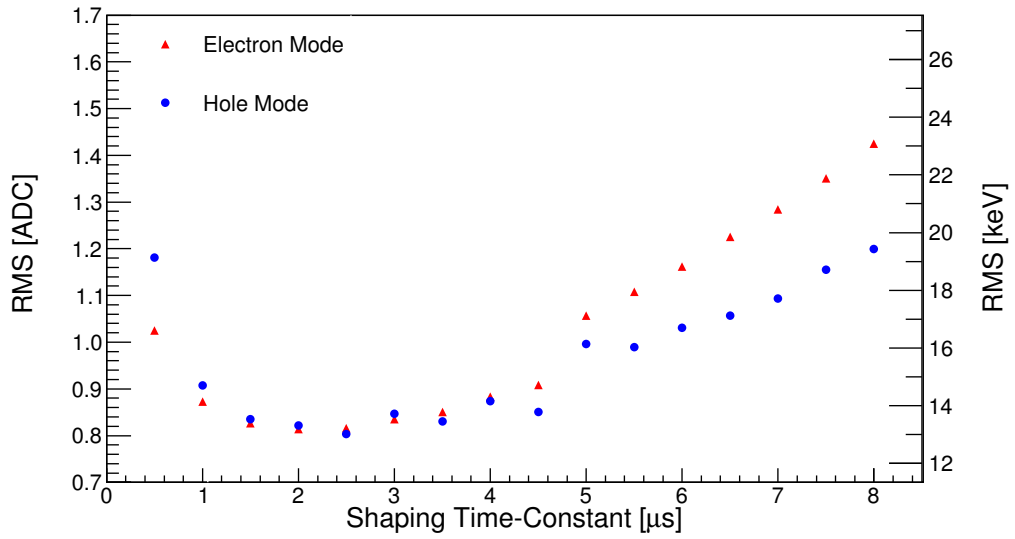


Figure 6.47: The average RMS noise of all channels is plotted for every shaping time-constant for both modes. All data shown is for a test pulse amplitude of V_{test} = 32.6 MeV (middle of dynamic range) when using the maximum sampling time of 17 μs.

of $\approx$ 1.4 ADC was observed for an 8.0 μs shaping time-constant. It is expected that a minimum in the measured noise should occur for a given shaping time-constant, as the series noise is proportional to $1/\sqrt{\tau}$ and parallel noise is proportional to $\sqrt{\tau}$. This results in large series noise contributions at small shaping time-constants and large parallel noise contributions at large shaping time-constants.

Using the relationship between ADC and keV (equation 5.25) the minimum RMS noise for a channel can be shown to be

$$0.8 \text{ ADC} = 0.8 \times 16.2 = 13.0 \text{ keV} \ . \tag{6.9}$$

Therefore the measured RMS noise for the bare ASIC is slightly smaller than the ADC resolution (16.2 keV). When connected to a strip of the detector the associated load at the preamplifier input, due to the strip capacitance, will increase the RMS noise so that it approaches the ADC resolution. The smallest noise that has been measured is greater than the 8.0 keV quoted in the ASIC specifications. The smallest value for the measured equivalent noise charge may also be expressed in units of electrons at the preamplifier input as

$$\frac{0.8 \times 16.2 \times 1000}{3.6} = 3600 \text{ electrons (RMS)}, \tag{6.10}$$

Table 6.13: The amplitude and delay of the test pulse was varied for fixed ASIC settings. Different shaping-time constants were tested.

DAPB [μs]	τ_{peak}[μs]	Eth [DN]	V_{test} [DN] [MeV]	Width [μs]	Delay [μs]
15.0	0.5-8.0	160	[1, 20, 48, 96] [0.5, 10.2, 24.4, 48.9]	10	200,400,600

where values of $\varepsilon_{pair} = 3.6$ eV for silicon and 16.2 keV for the theoretical ADC bin width have been used to convert the value in equation 6.9 to electrons.

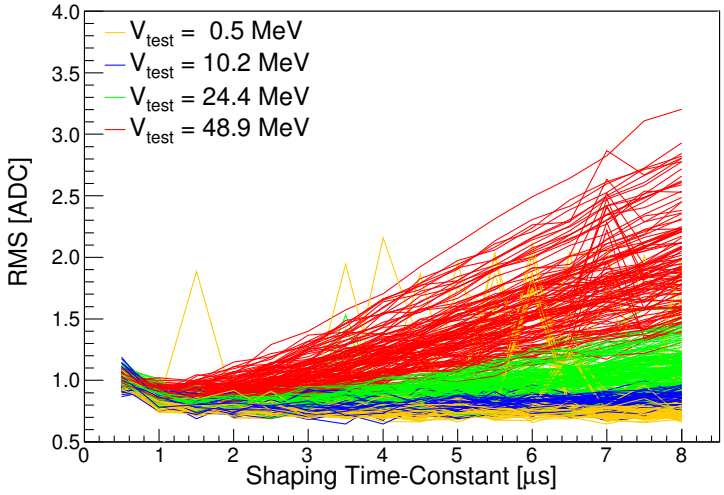
6.10 Pulse Amplitude and Rate Effects

The dependency of the RMS noise level on the amplitude of the injected pulse and the time between successive pulses (delay) must be understood. The effect of pulse amplitude and rate on the observed noise level has been quantified for four pulse amplitudes (0.5, 10.2, 24.4 and 48.9 MeV) and three pulse rates (200, 400 and 600 μs) using the settings outlined in Table 6.13. This range of amplitudes ensures the ASIC has been tested up to the maximum quoted dynamic range and the range of pulse delay settings also ensures the quoted maximum readout rate (5 kHz) has been tested. The sampling time was fixed for all tests by using a constant value so that DAPB has no influence on the results. A value for the sampling time of DAPB = 15 μs was decided upon as it has been proven that this produces the best performance for both modes. A total of 512 test pulses were injected into each channel for each of the four pulse amplitudes using the full range of shaping time-constants.

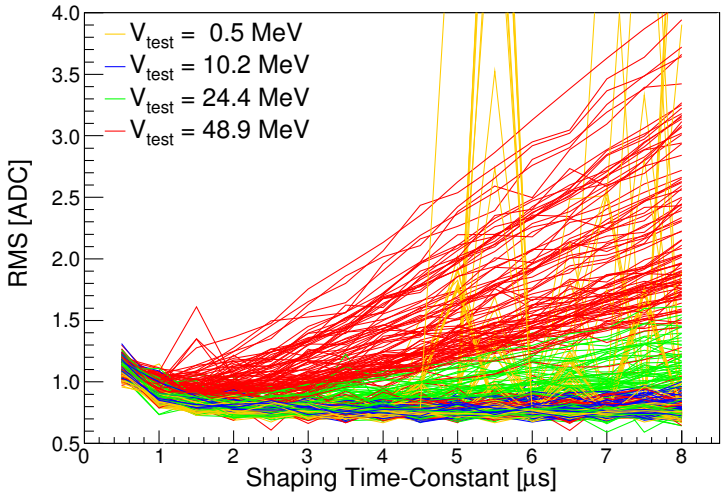
6.10.1 Pulse Amplitude and Noise

Four different test pulse amplitudes have been tested using a pulse delay of 600 μs. The distribution of measured ADC values has been analysed for different test pulse amplitudes and the RMS ADC is calculated for every channel. The RMS ADC obtained for the different pulse amplitudes (using fixed ASIC settings) is shown in Figure 6.48. Increasing the test pulse amplitude results in greater RMS noise, with more noise seen for the largest shaping time-constants. For shaping time-constants of 0.5 and 1.0 μs, the pulse amplitude has little or no effect on the measured RMS noise. As the shaping time-constant increases above 1.0 μs, the effect of pulse amplitude on the RMS noise becomes ever more noticeable. The maximum RMS noise is observed for the largest pulse amplitude and largest shaping time-constant. Conversely, the minimum RMS noise is observed for the smallest pulse amplitude

for shaping time-constants in the range 1-3 μs.



(a) Electron mode.

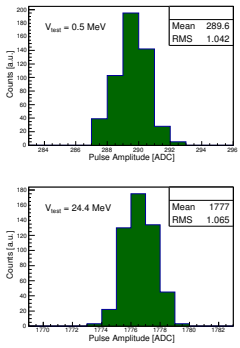


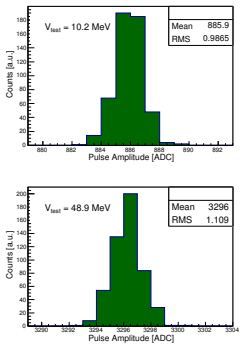
(b) Hole mode.

Figure 6.48: The RMS ADC is plotted against shaping time-constant for a range of pulse amplitudes covering the full dynamic range. The RMS noise is highest for large pulse amplitudes.

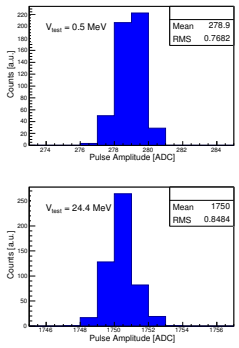
To further understand the relationship between RMS noise and pulse amplitude, it is necessary to study the measured ADC distribution for the different test pulse amplitudes. Figure 6.49 shows the distribution of the pulse amplitudes that were measured for all 512 pulses that were injected into channel 1. The amplitude distributions are shown for four pulse amplitudes using three different shaping time-constants where the mean and RMS of each distribution is shown.

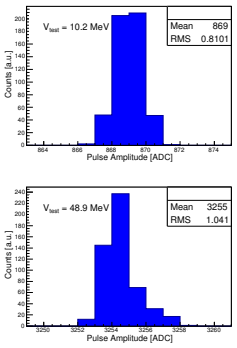
For a test pulse amplitude V_{test} = 48.9 MeV, the measured ADC distribution becomes more non-Gaussian for larger shaping time-constants. The data for V_{test} = 48.9 MeV in Figure 6.49c (τ_{peak}= 8.0 μs), shows a non-Gaussian distribution with a significant number of measured pulses having ADC values that are greater than the mean of the distribution. The excessive number of pulses with an ADC greater than the mean leads to an increased value of the RMS for the distribution which is also clearly seen for V_{test} = 48.9 MeV in Figure 6.49b (τ_{peak}= 4.0 μs). This tailing effect is less apparent for V_{test} = 48.9 MeV in Figure 6.49a (τ_{peak}= 0.5 μs). The ADC distribution observed for V_{test} = 24.4 MeV in Figure 6.49c (τ_{peak}= 8.0 μs) also exhibits a tailing effect but the same behaviour is not seen for other shaping time-constants for the same pulse amplitude.



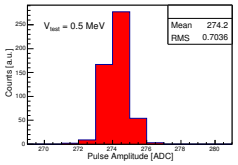


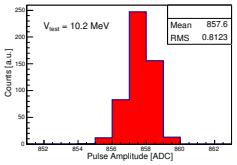
(a) Shaping time-constant = 0.5 μs.

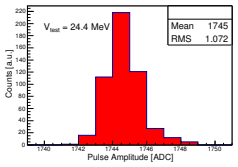


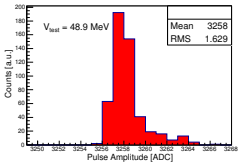


(b) Shaping time-constant = 4.0 μs.









(c) Shaping time-constant = 8.0 μs.

Figure 6.49: The ADC distribution of 512 injected pulses with four different amplitudes is shown in (a), (b) and (c) for channel 1. Three different shaping time-constants are shown for comparison. For shaping time constants of 4.0 μs (b) and 8.0 μs (c) the RMS noise increases for larger pulse amplitudes due to a non-Gaussian distribution of amplitudes. Electron mode data.

The RMS ADC values from Figure 6.49 are summarised in Table 6.14. For a shaping time-constant of 0.5 μs, the RMS noise is similar for all test pulse ampli-

Table 6.14: The calculated RMS ADC value is shown for each test pulse amplitude for three shaping time-constants.

	V_{test} [MeV]			
	0.5	10.2	24.4	48.9
Shaping Time-Constant [μs]	RMS [ADC]			
0.5	1.04	0.99	1.07	1.11
4.0	0.77	0.81	0.85	1.04
8.0	0.70	0.81	1.07	1.63

tudes. For a shaping time-constant of 8.0 μs, the RMS noise is smallest for small pulse amplitudes and increases for larger pulse amplitudes. The smallest RMS noise is observed for small test pulse amplitudes with shaping time-constants in the range 2-8 μs.

Comments

The data shown in Figure 6.49 is all for the same channel. Any variation in the measured ADC distributions can therefore not be attributed to differences in preamplifier or shaper gain, as all data is gathered using the same front-end components. It was previously shown in section 6.9.4, for a fixed pulse amplitude, that a shaping time-constant of 8.0 μs results in a larger RMS noise than a smaller shaping time-constant. However, a larger pulse amplitude can significantly increase the RMS noise also.

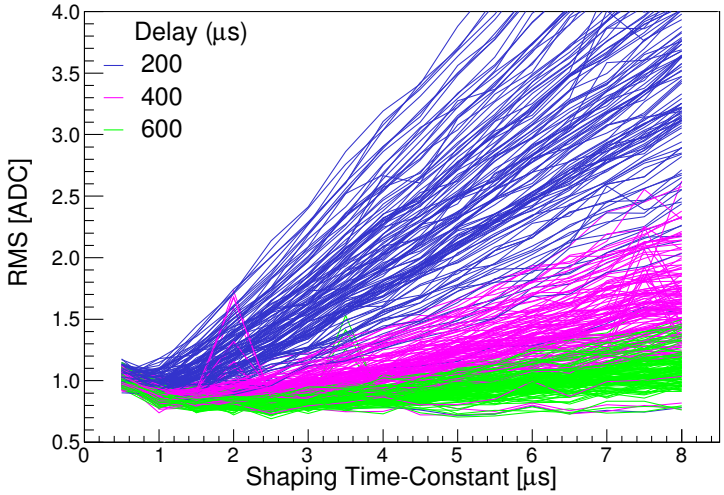
A possible explanation for this pulse amplitude dependency may be due to the undershoot that occurs when the test pulse finishes and is restored to the baseline. When the test pulse is restored to the baseline, at the falling edge of the pulse, there may be a temporary undershoot where the signal briefly falls below the baseline. The amplitude of the undershoot may be greater for larger test pulse amplitudes. If a second pulse is injected whilst the undershoot is still present in the system, the amplitude of the second pulse will be slightly smaller than the first pulse as the reference baseline is now smaller. A scenario such as this could result in an ADC distribution where many pulses have an ADC that is slightly smaller than expected and a few pulses may have been minimally affected resulting in slightly larger ADC values. This may explain why the ADC distribution has a tail for the largest pulse amplitudes.

6.10.2 Pulse Rate and Noise

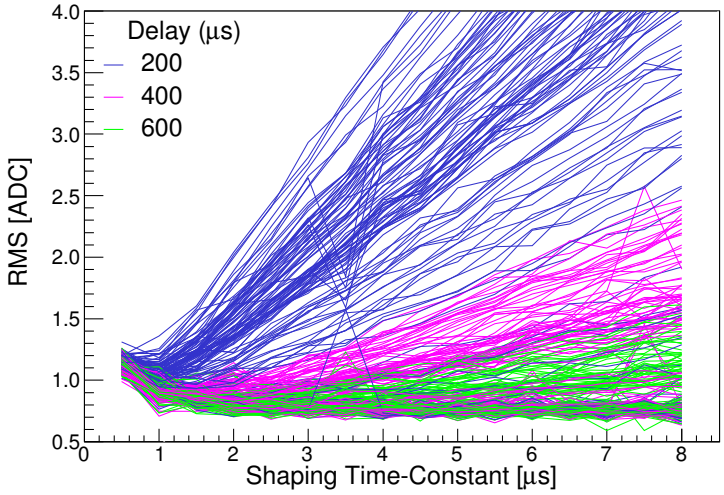
The ASIC's performance has been tested using different test pulse rates with a fixed pulse amplitude $V_{test} = 24.4$ MeV for different shaping time-constants. Test pulses were injected at delay intervals of 200, 400 and 600 μs. The measured ADC values have been analysed for the different pulse rates. The RMS of the ADC distribution of each channel has been calculated for each delay setting for all shaping time-constants.

The RMS noise for electron mode and hole mode is plotted for each shaping time-constant for three pulse delay settings in Figure 6.50. The test pulses that were injected using the longest delay of 600 μs result in the smallest RMS noise. The shortest pulse delay of 200 μs generated RMS ADC values greater than 4 ADC for the largest shaping time-constants. This is a similar behaviour to what was seen previously in section 6.10.1 where a dependency between noise and pulse amplitude was observed. Whereas it was previously determined that increasing pulse amplitude resulted in larger RMS noise, it can also be said that a faster pulse rate increases the RMS noise. The configuration with the longest delay and smallest pulse amplitude thus gives the least amount of noise.

The measured ADC distribution for a single channel (channel 1) is shown in Figure 6.51 for the three pulse delay settings used. It is clear that decreasing the pulse delay from 600 μs to 200 μs produces an ADC distribution that is broader with a smaller value for the mean ADC. By changing the delay from 600 μs to 200 μs the mean ADC is altered by approximately 3 ADC. This phenomena may arise due to the undershoot which occurs when the test pulse is restored to the baseline. For the fastest pulse rates, the undershoot may still be present when the next pulse is injected which will effectively decrease the amplitude of the next injected pulse. Therefore, slightly smaller ADC values may be measured for very fast pulse rates up to 5 kHz. In Figure 6.51 this phenomena can clearly be seen with the effect being only slightly noticeable for a pulse delay of 400 μs.



(a) Electron mode.



(b) Hole mode.

Figure 6.50: The RMS ADC is plotted against shaping time-constant for three pulse rates up to the maximum of 5kHz (200 μs delay). The RMS noise is largest for the shortest delay.

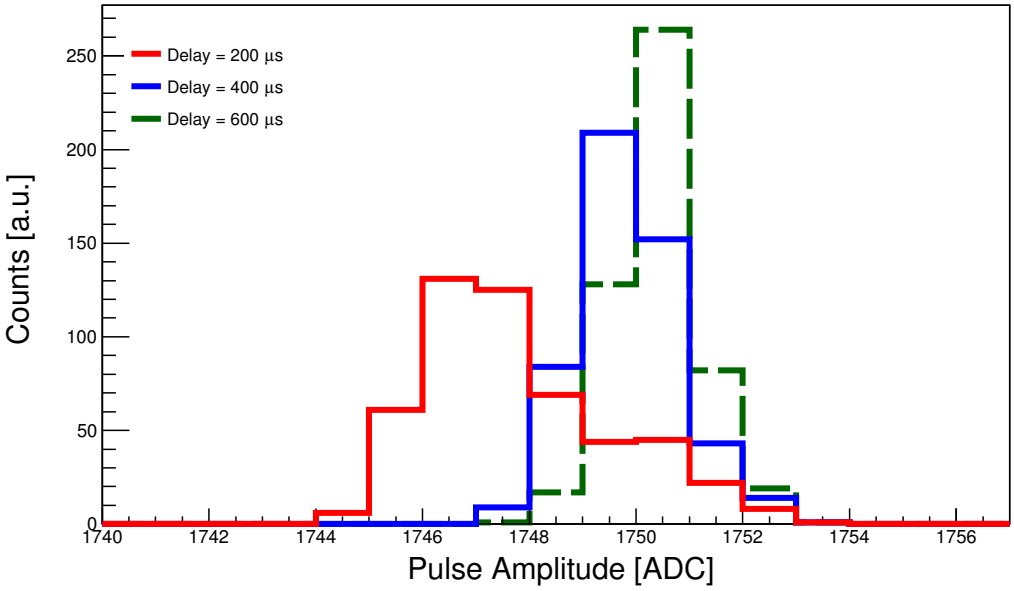


Figure 6.51: Plot for V_{test} = 24.430 MeV (DN = 48), electron mode channel 1 showing the effect of pulse delay for a constant peaking time of 4.0 μs.

6.11 Front-End Linearity Testing

An important property of the ASIC functionality is the ability of the front-end to convert an analogue voltage signal to a digital number which represents the signal amplitude. A larger quantity of charge at the preamplifier input will result in a larger amplitude signal at the ADC input. The linearity of the ASIC is a property which can be tested by varying the amplitude of the injected test pulse and studying how the measured ADC value changes. A test has been performed where the test pulse amplitude was swept across the entire energy range and the difference between the resulting output and an ideal ADC output has been calculated.

6.11.1 Dynamic Range

Increasing the amplitude of the test pulse V_{test} results in a larger quantity of charge at the input to the preamplifier. A larger test pulse will thereby produce a preamplifier output signal with a larger amplitude. This results in a larger signal at the shaper output and subsequently a larger voltage is sampled by the peak-hold circuitry that is then converted to a larger digital number courtesy of the 12-bit ADC. The linearity of both electron and hole mode has been examined. The test pulse amplitude was incremented from the smallest test pulse amplitude 7.8 mV (509 keV) until the ADC became saturated.

The specifications quote the full dynamic range of the ADC as 2 V. A 2 V signal at the ADC input should ideally result in an ADC output code of 4095. The testing was implemented by injecting 512 test pulses into each channel using the settings outlined in Table 6.15. Figure 6.52 displays the relationship between test pulse amplitude and the measured ADC for all 128 channels of an ASIC for electron and hole mode. A similar behaviour is seen for all channels with the intercept (ADC value at $V_{test} = 0$ DN) appearing to be roughly 300 ADC for all channels for both modes. Figure 6.53 shows the saturation of the ADC occurring for both modes at test pulse amplitudes of approximately 63.62 MeV (125 DN). In electron mode a test input of 63.62 MeV ($VCal = 125$ DN) resulted in saturation of the ADC for all channels. For hole mode, a $VCal$ value of 125 DN resulted in saturation of the ADC for all except three channels.

Table 6.15: ASIC and test pulse settings used for front-end linearity testing.

DAPB [μs]	τ_{peak} [μs]	Eth [DN]	ΔV [DN] [MeV]	Width [μs]	Delay [μs]
15.0	0.5, 4.0, 8.0	154	[1-130] [0.5-66.2]	10	600

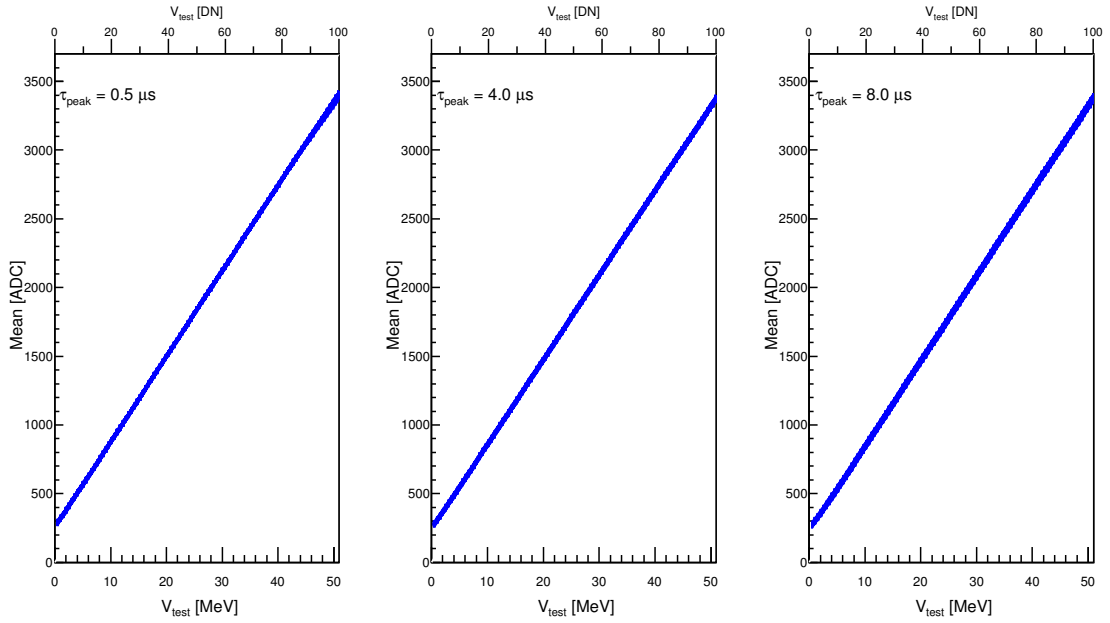
A test pulse amplitude greater than $V_{test} = 125 \times 7.8$ mV = 0.975 V at the test capacitor results in saturating the ADC of all channels in both electron mode and hole mode. A test pulse of $V_{test} = 0.975$ V can be represented as $E_{test} = 63.62$ MeV, according to equation 5.9. The specifications quote a dynamic range for the ASIC of 0-50 MeV, which is comfortably within the measured dynamic range of about 0-63 MeV.

ADC Dynamic Range

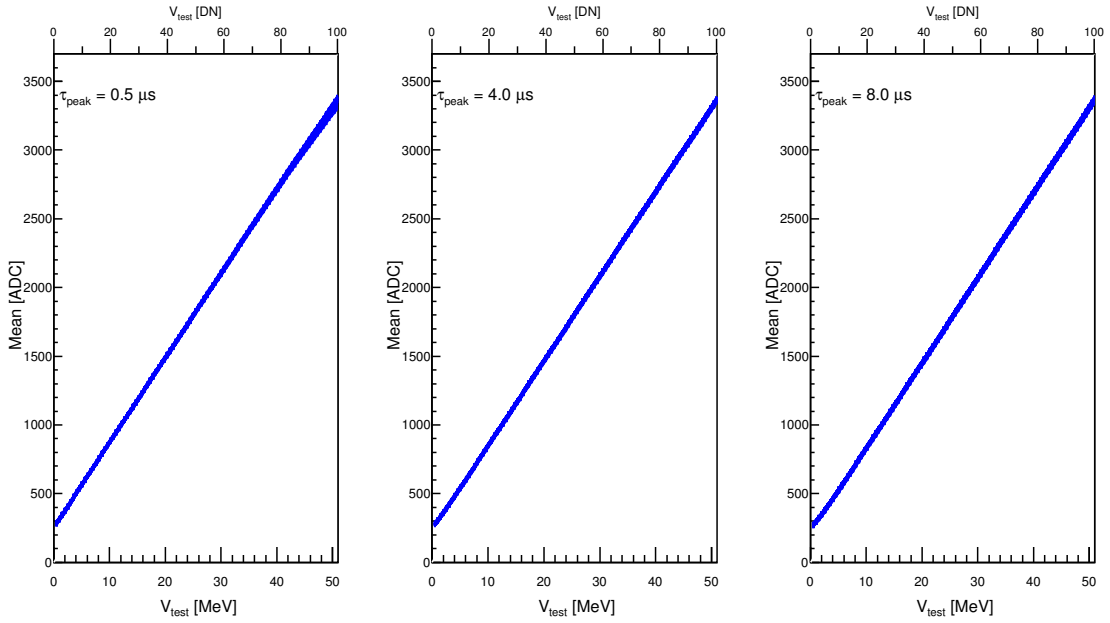
It was previously calculated that the preamplifier gain for an injected test pulse is $A = 2.057$. The signal from the preamplifier is passed to the ADC via the shaper (gain = 0.956) and peak-hold circuit (gain = 1). The default shaper reference voltage of 0.105 V means that all signals from the shaper have a minimum baseline level of 0.105 V. Therefore, for a test input of amplitude $V_{test} = 0.975$ V the expected amplitude of the shaper output is

$$V_{out} = (2.057 \times 0.956 \times 0.975) + 0.105 = 2.022 \text{ V} . \tag{6.11}$$

The theoretically calculated voltage at the shaper output, which is passed to the ADC, is shown in Table 6.16 for the test pulse amplitudes at which the ADC was observed to reach saturation for channels in both modes. A signal of amplitude 124 DN and 125 DN would be expected to cause saturation of an ADC with a 2 V dynamic range. The test pulse amplitude at which saturation occurs is consistent with the calculations for an ideal preamplifier and shaper in Chapter 5 and prove that the ADC has a dynamic range of 0-2 V.

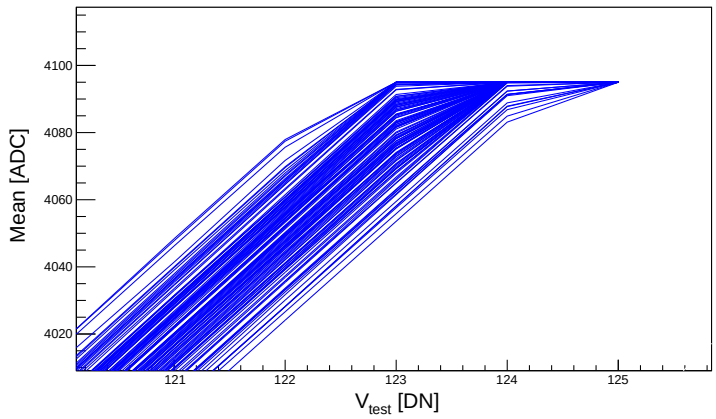


(a) Electron mode.

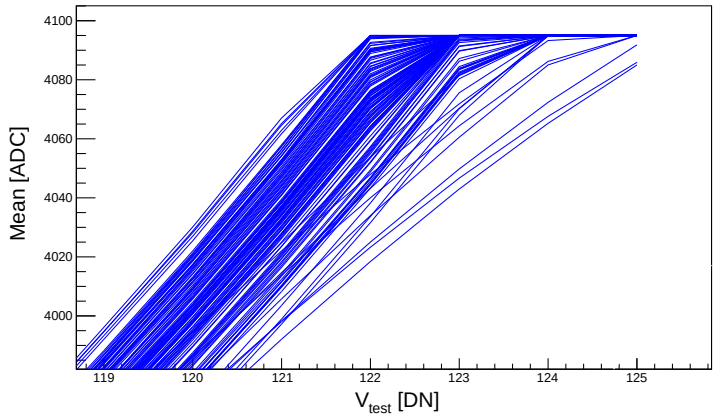


(b) Hole mode.

Figure 6.52: A front-end linearity test where the amplitude of the input pulse and the corresponding mean ADC of the 512 pulses are plotted for each channel up to 50 MeV. The test pulse amplitude is shown in units of MeV and DN (digital number). The test pulse amplitude in Volts is obtained by multiplying the value V_{test} [DN] by 7.8 mV.



(a) Electron mode.



(b) Hole mode.

Figure 6.53: Saturation of the ADC at large test pulse amplitudes for a shaping time-constant of 4.0 μs. A test pulse of V_{test} = 125 DN saturates all but three channels for both modes.

Table 6.16: The test pulse amplitude in digital number (DN) and Volts is shown with the associated shaper ouput voltage V_{out} which is passed to the ADC.

V_{test} [DN]	V_{test} [V]	V_{out} [V]
122	0.952	1.976
123	0.959	1.992
124	0.967	2.007
125	0.975	2.022

6.11.2 Linearity Fitting Analysis

To fully understand how the measured ADC changes with signal amplitude it is beneficial to compare the data for each channel with a straight line fit, which is representative of an ideal response. A linear fit has been performed for the data of each channel for three peaking times for both modes to reveal small changes within the measured ADC across the full dynamic range quoted in the specifications. By calculating a straight line fit for each channel, the average slope and intercept of each channel has been determined which will be used for further analysis. The ASIC specifications quote a dynamic range of 50 MeV and therefore the following analysis will primarily consider data within the range 0-50 MeV (V_{test} = 1-98 DN).

Shown in Figure 6.54 is the data for a single channel (channel 0) along with the performed chi-squared minimisation fit (data is fitted up to V_{test} = 120 DN for this example only). The values for the intercept and slope, obtained from the straight line fit for channel 0, are displayed in Table 6.17 for fitting within the range V_{test} = 1-120 DN and V_{test} = 1-98 DN for comparison. The result of fitting within the two ranges results in a small change in the measured intercept and slope of a single channel.

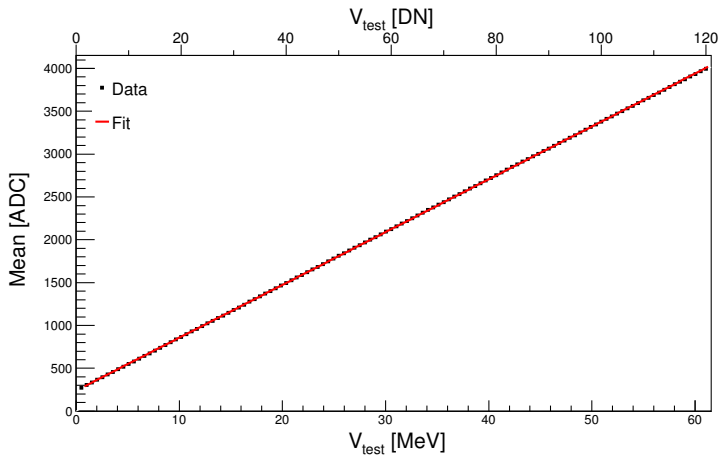


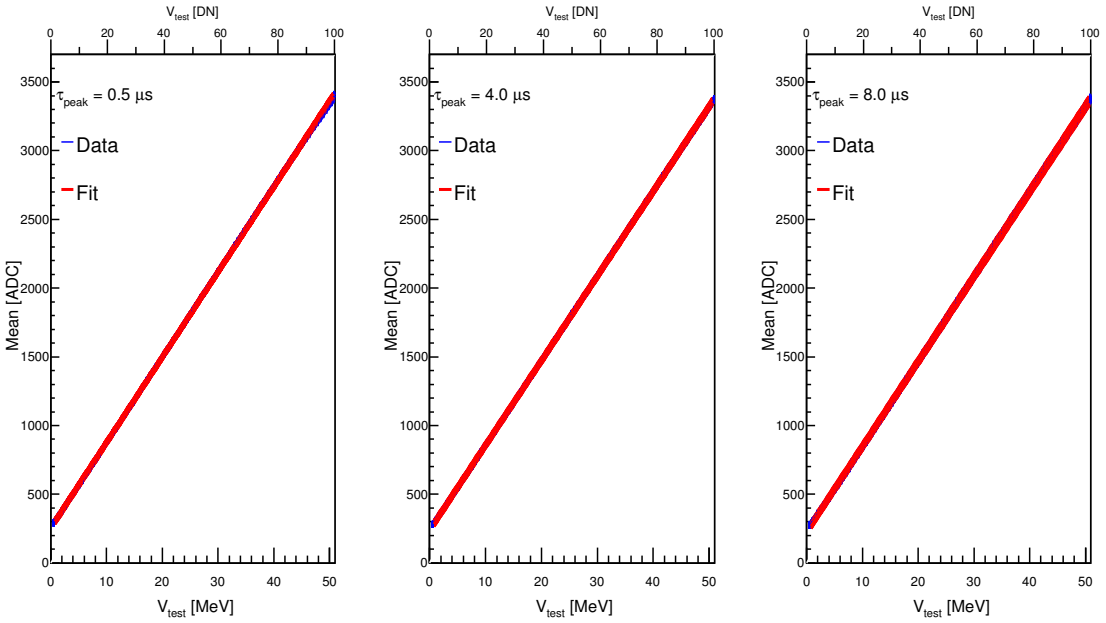
Figure 6.54: A fit of the linearity for channel 0 in electron mode for a peaking time of 4 μs. The plotted data (black) and the associated fit (red) range from 509 keV to 61.074 MeV (V_{test} = 1 DN to V_{test} = 120 DN).

A straight line fit has been applied to the data from all individual channels for both modes (fitting from V_{test} = 1-100 DN only) and the results are displayed in Figure 6.55. The ADC intercept and slope value of the fit for each channel has been histogrammed for each peaking time in order to make a comparison between the different settings. In Figure 6.56 the intercept values have been histogrammed for

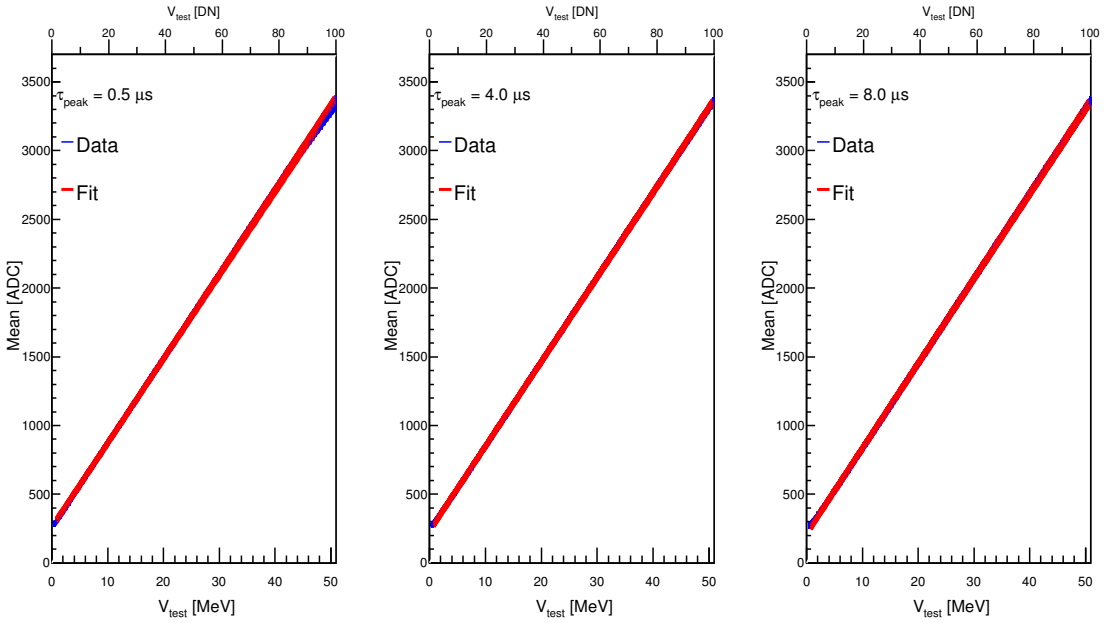
electron mode and the equivalent plots for hole mode are shown in Figure 6.57. The slope values have been histogrammed for electron mode in Figure 6.58 and for hole mode in Figure 6.59. The histograms have then been analysed to calculate mean and RMS ADC values of the intercept and slope values from the distributions of the 128 channels. The mean and RMS ADC values are summarised in Table 6.18 and Table 6.19 and will be used for further analysis of the slope and intercept.

Table 6.17: Slope and intercept value for linearity fit of channel 0 for electron mode with a peaking time of 4 μs.

Channel	Slope [ADC/keV]	Intercept [ADC]
(V_{test} = 1-120)	0.06166	240.181
(V_{test} = 1-98)	0.0617858	237.797



(a) Electron mode.



(b) Hole mode.

Figure 6.55: A linear fit has been calculated for all channels for all modes to determine the slope and intercept of each channel. The measured data is shown as a blue line for each channel and the straight line fit for each channel is the red line.

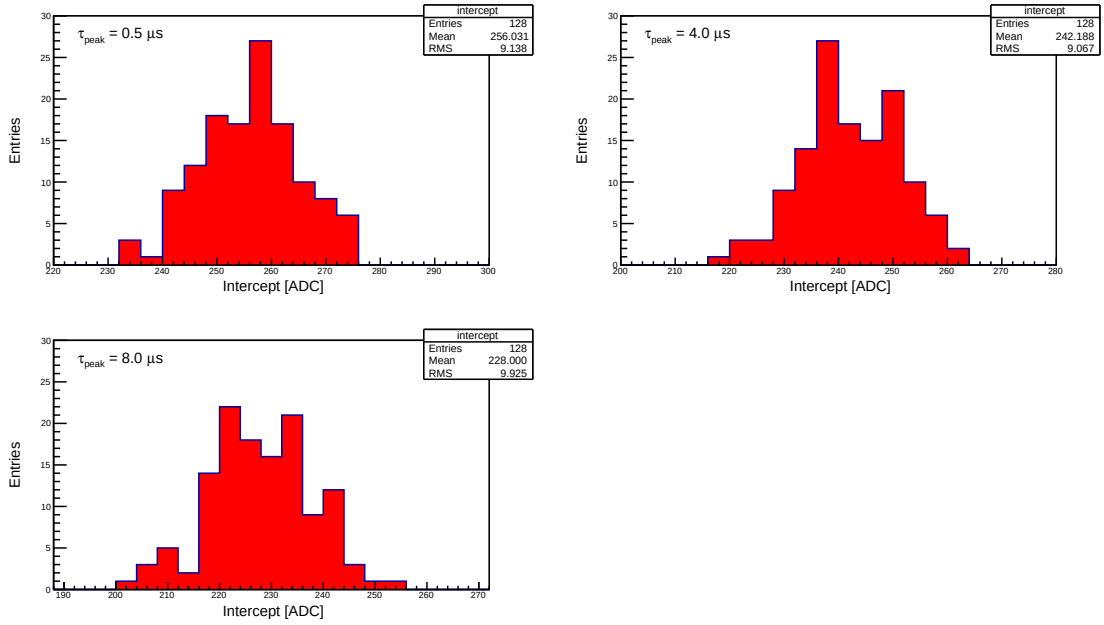


Figure 6.56: Intercept values are histogrammed for straight line fits for all channels in electron mode.

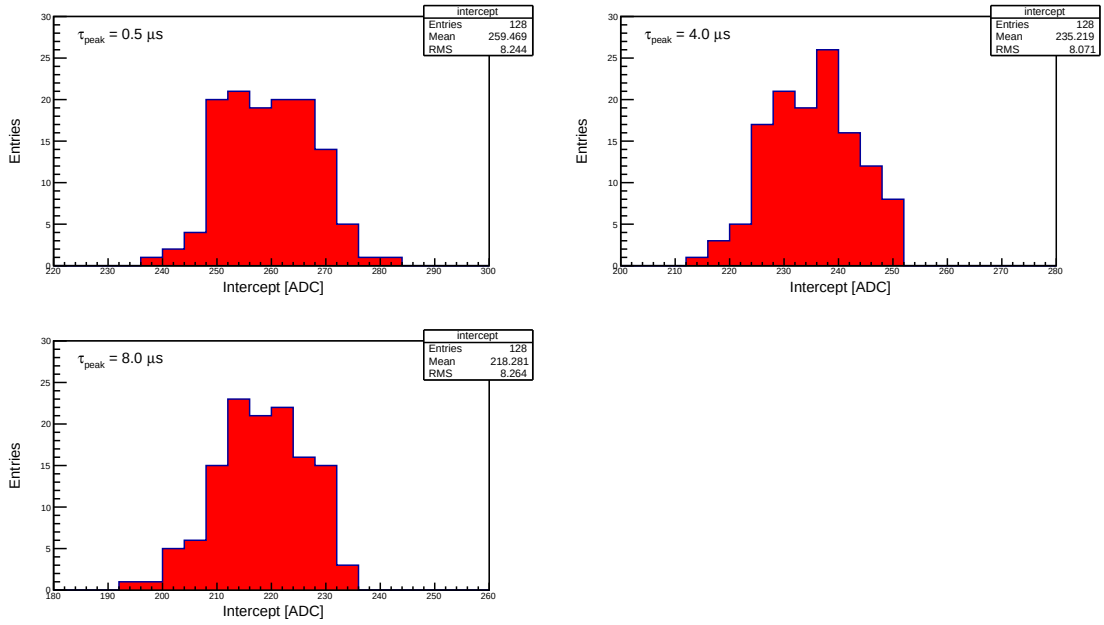


Figure 6.57: Intercept values are histogrammed for straight line fits for all channels in hole mode.

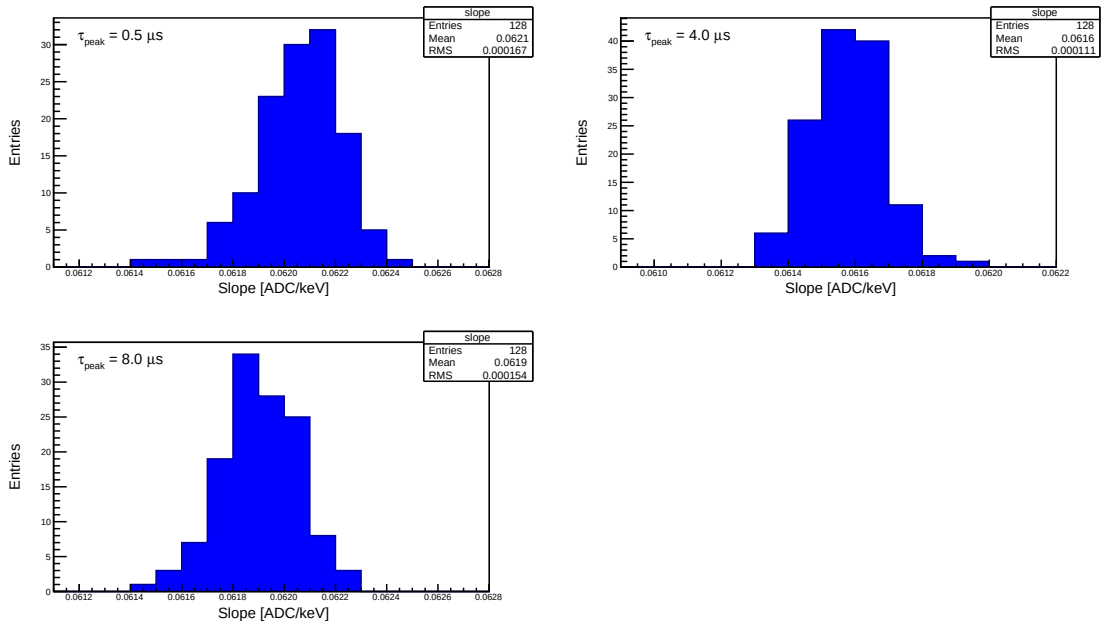


Figure 6.58: Slope values are histogrammed for straight line fits for all channels in electron mode.

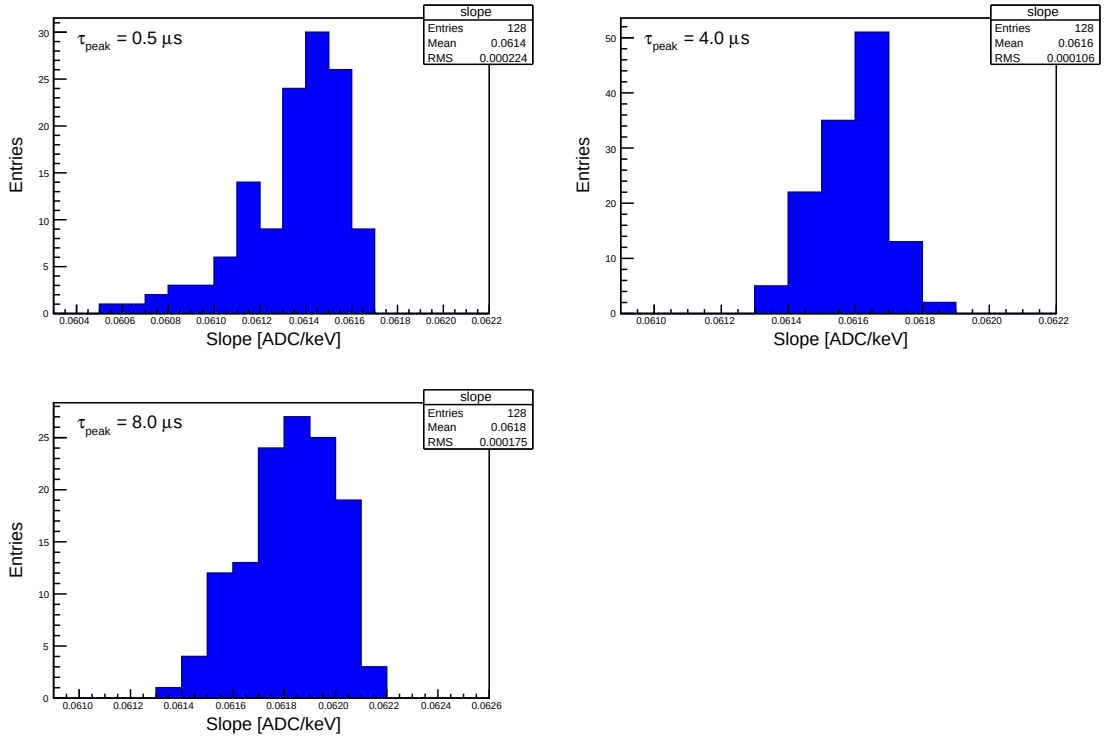


Figure 6.59: Slope values are histogrammed for straight line fits for all channels in hole mode.

Table 6.18: The mean and RMS ADC values for the linearity straight line fit of all channels for $\tau_{peak} = 0.5, 4.0$ and 8.0 μs for electron mode within the range 0-50 MeV.

$\tau_{peak}[\mu s]$	Slope [ADC/keV]		Intercept [ADC]	
	Mean	RMS	Mean	RMS
0.5	0.0621	0.000167	256.031	9.138
4.0	0.0616	0.000111	242.188	9.067
8.0	0.0619	0.000154	228.000	9.925

Table 6.19: The mean and RMS ADC values for the linearity straight line fit of all channels for $\tau_{peak} = 0.5, 4.0$ and 8.0 μs for hole mode within the range 0-50 MeV.

$\tau_{peak}(\mu s)$	Slope [ADC/keV]		Intercept [ADC]	
	Mean	RMS	Mean	RMS
0.5	0.0614	0.000224	259.469	8.244
4.0	0.0616	0.000106	235.219	8.071
8.0	0.0618	0.000175	218.281	8.264

Slope Analysis

For a peaking time of $\tau_{peak} = 4.0$ μs, for both modes, the mean value for the slope of all 128 channels was calculated to be 0.0616 $\pm$ 0.0001 ADC/keV. This slope value is an average of all channels that represents the average gain of each channel across the dynamic range. The average width of each ADC bin is thus given by the reciprocal of the slope, and hence is measured to be 16.23 $\pm$ 0.03 keV/ADC for both modes for a shaping time-constant of 4.0 μs.

The theoretical ADC bin width was previously determined in section 5.5.4 by calculating the voltage amplitude at the ADC input for all possible test pulses and converting the analogue voltage to an ADC value. By plotting the ADC value against the test pulse amplitude in keV it was possible to construct a plot whereby the slope (front-end gain) was determined. For a 12-bit ADC it was shown in equation 5.25, assuming ideal equations, that 0.488 mV pulse at the ADC input corresponds to 1 ADC which is equivalent to a 16.20 keV signal at the preamplifier input. The ideal slope value was calculated to be 0.0617 ADC/keV. This calculation accounted for the shaper gain being $A_{sha} = 0.96$ when using the exact capacitance values quoted in the ASIC specification.

The average slope values for each peaking time and the resultant average ADC bin width values are shown in Table 6.20. The average slope and thus bin width has

Table 6.20: The mean slope values and corresponding measured bin widths in keV for each peaking time.

τ_{peak} = 0.5 μs	Slope [ADC/keV]		Bin Width [keV/ADC]	
	Mean	RMS	Mean	RMS
Electron	0.0621	0.000167	16.10	0.04
Hole	0.0614	0.000224	16.29	0.06
τ_{peak} = 4.0 μs	Slope [ADC/keV]		Bin Width [keV/ADC]	
	Mean	RMS	Mean	RMS
Electron	0.0616	0.000111	16.23	0.03
Hole	0.0616	0.000106	16.23	0.03
τ_{peak} = 8.0 μs	Slope [ADC/keV]		Bin Width [keV/ADC]	
	Mean	RMS	Mean	RMS
Electron	0.0619	0.000154	16.16	0.04
Hole	0.0618	0.000175	16.18	0.05

been measured for both modes for three shaping time-constants and the smallest bin width measured is 16.10 ± 0.04 keV/ADC and the largest bin width is 16.29 ± 0.06 keV/ADC. The theoretically calculated ADC bin width falls within this range and shows very good agreement with all front-end gain values that have been measured.

The results show that small differences in the measured values for the slope were obtained for the three different peaking times that were tested. The variation in gain due to changes in shaping time-constant is small and can be attributed to variation in shaper capacitances resulting in slightly different shaper gain for different time-constants. It was shown previously (see section 5.5.4) that a ±15% tolerance on the shaper capacitances can result in a maximum and minimum gain of 0.09642 and 0.0389 ADC/keV, respectively. The true values of the shaper capacitances are well within this 15% tolerance limit and the ideal calculations performed throughout Chapter 5 show very strong agreement with the measured data.

Intercept Analysis

The ADC value at which the straight line fit for a channel intersects the y-axis (V_{test} = 0 DN) is an important property of the ASIC. The value of the intercept obtained from the linearity fit represents the ADC offset which determines the smallest possible ADC value that can be achieved. The ADC offset should be dependent upon the shaper reference voltage only. It is expected that the value of the offset should be the same for any programmed shaping time-constant as long as the shaper reference voltage remains constant. When no signal is present, the shaper output will retain

a fixed baseline voltage, which is equal to the shaper reference voltage and thus any signal at the ADC input must be at least greater in amplitude than the shaper reference voltage.

For the electron mode configuration, all shaper output signals are referenced to a 2.5 V reference baseline (0.5 V baseline for hole mode). In electron mode, the input signal to the preamplifier is negative going, thus producing a positive going preamplifier output signal and a negative going shaper output signal (decreases relative to 2.5 V baseline). For hole mode the shaper output signal is positive going (increases relative to 0.5 V baseline). For electron mode the default shaper reference voltage is $V_{SHA} = 2.406$ V and for hole mode the reference voltage is $V_{SHA} = 0.594$ V. For both modes, the shaper reference voltage results in a shaper output voltage that differs from the reference baseline level by $V_{rel} = 0.094$ V when no signal is present at the shaper input. Therefore, when a signal is received at the shaper input, the shaper output value decreases from its baseline of 2.406 V towards 0.5 V for electron mode. Conversely for the hole mode setup the shaper output is positive going and thus the shaper output value increases from its baseline of 0.594 V towards 2.5 V due to a signal.

Using the relationship between ADC output code and the ADC input voltage (shown previously as 1 ADC $= 2/2^{12}$ V for a 12-bit ADC with 2 V dynamic range), the measured intercept ADC can be easily converted to an equivalent voltage. The relative default shaper reference voltage ($V_{rel} = 0.094$ V) should theoretically result in an intercept value of

$$\mathrm{ADC}_{Intercept} = \frac{V_{rel}}{\frac{2}{2^{12}}} = \frac{0.094}{\frac{2}{2^{12}}} = 193 \text{ ADC} \tag{6.12}$$

for both electron and hole mode. The measured intercept values for the peaking times 0.5, 4.0 and 8.0 μs are shown in Table 6.21 for the default shaper reference voltage of 2.406 V (electron mode) and 0.594 V (hole mode). The measured value for the ADC intercept (average of 128 channels) has been used to calculate a value for the shaper reference voltage relative to the 0.5 and 2.5 V levels. The value of the intercept in Volts $V_{Intercept}$ signifies the difference between the shaper reference voltage and the 0.5 or 2.5 V level. The shaper reference voltage V_{SHA} is related to the measured ADC intercept by

$$V_{SHA} = 2.5 - V_{Intercept} = 2.5 - \left(\mathrm{ADC}_{Intercept} \times \frac{2}{2^{12}}\right), \tag{6.13}$$

for electron mode, and

$$V_{SHA} = 0.5 + V_{Intercept} = 0.5 + \left(\text{ADC}_{Intercept} \times \frac{2}{2^{12}} \right) , \tag{6.14}$$

for hole mode.

Table 6.21: The mean and RMS value for the measured intercept ADC for all 128 channels is shown for $\tau_{peak} = 0.5$, 4.0 and 8.0 μs for both modes. The ADC value is converted to Volts and the shaper reference voltage V_{SHA} is equal to the difference between the intercept and the reference level (2.5 V for electron mode and 0.5 V for hole mode).

$\tau_{peak}(\mu s)$	Intercept [ADC]		Intercept [V]		V_{SHA} (V)	
Electron Mode	Mean	RMS	Mean	RMS	Mean	RMS
0.5	256	9	0.125	0.004	2.375	0.004
4.0	242	9	0.118	0.004	2.382	0.004
8.0	228	10	0.111	0.005	2.389	0.004
$\tau_{peak}(\mu s)$	Intercept [ADC]		Intercept [V]		V_{SHA} (V)	
Hole Mode	Mean	RMS	Mean	RMS	Mean	RMS
0.5	259	8	0.127	0.004	0.627	0.004
4.0	235	8	0.115	0.004	0.615	0.004
8.0	218	8	0.107	0.004	0.607	0.004

For the three different shaping time-constants, the value of the ADC intercept shows some difference but theoretically the ADC intercept should be the same for all shaping time-constants. The maximum ADC intercept measured was 259 ADC and the minimum value was 218 ADC. When considering the shaper reference voltage is programmed with an 8-bit resolution and the 12-bit ADC resolution is 0.49 mV/bin, some variation in measured ADC is expected due to the difference in granularity. For all six measurements, the value that has been deduced for the shaper reference voltage is approximately 2.4 V and 0.6 V for electron and hole mode, respectively when rounding to one decimal place. The measured reference voltages therefore agree with the values quoted in the ASIC specifications that specify the bias voltage to a precision of one decimal place.

Shaper Reference Voltage

A further test has been carried out in electron mode to understand how the ADC intercept changes with V_{SHA}. Three different values for the shaper reference voltage have been tested using the same programmed shaping time-constant (8.0 μs). Altering the shaper reference voltage should increase or decrease the baseline signal at the shaper output and consequently increase or decrease the measured ADC intercept.

The result of injecting test pulses with amplitudes covering the full dynamic range of 0-50 MeV and fitting with a straight line is shown in Figure 6.60 for three different shaper reference voltages. The change in ADC intercept due to changes in V_{SHA} is clear and the intercept value for every channel is histogrammed in Figure 6.61 for the different reference voltages. The mean and RMS ADC values obtained from the three histograms have been converted to Volts in Table 6.22, where the theoretically expected value for V_{rel} is included for comparison. For the three measurements, the expected value V_{rel} is always slightly smaller than the actual measured intercept value but a clear relationship is observed. The values in the table show that the measured ADC intercept changes linearly with V_{SHA} and the ADC intercept value can be directly related to the difference between the shaper reference voltage and the 2.5 V reference level V_{rel} in electron mode.

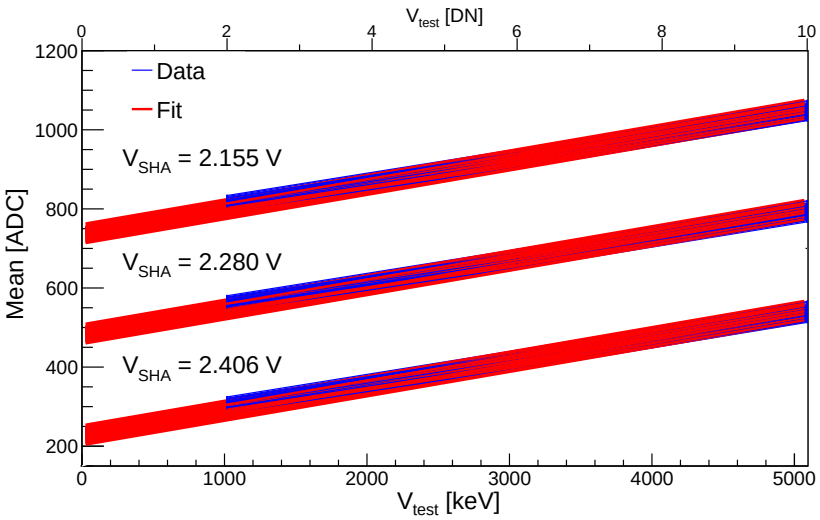


Figure 6.60: Changing the shaper reference voltage for an 8 μs shaping time-constant in electron mode results in a different ADC intercept. The data for each channel has been fitted for the range 0-50 MeV and is represented by the red line.

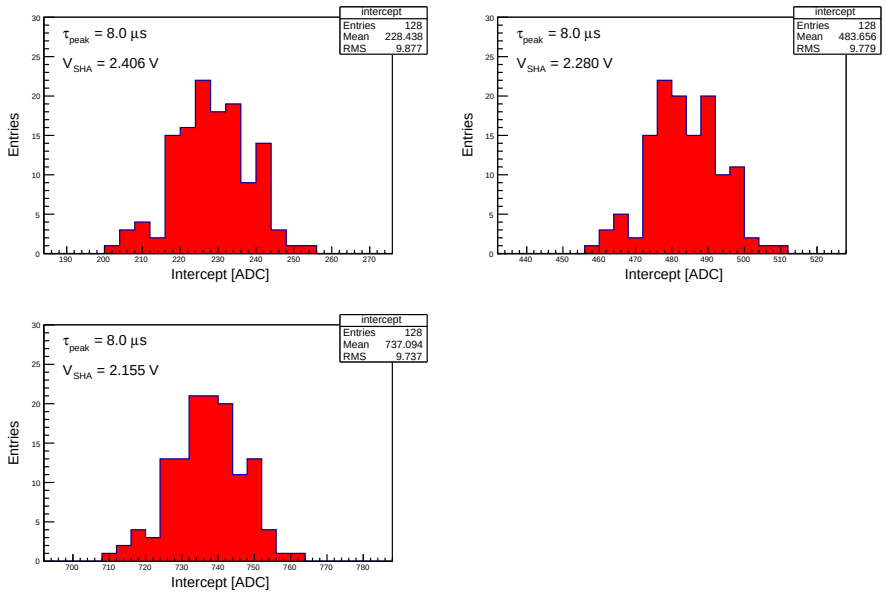


Figure 6.61: The ADC intercept is shown for all 128 channels of an ASIC for three different shaper reference voltages in electron mode for a shaping-time constant of 8 μs.

Table 6.22: The mean and RMS values for the ADC intercept of all 128 channels are shown in units of Volts (Intercept[V]) for three shaper reference voltages. The difference between the programmed shaper reference voltage and the 2.5 V level is represented by V_{rel}[V].

Shaper Reference [V]	Intercept [ADC]		Intercept [V]		V_{rel}[V]	
	Mean	RMS	Mean	RMS	Mean	RMS
2.406 V	228.438	9.877	0.111	0.005	0.094	0.0001
2.280 V	483.656	9.779	0.236	0.005	0.220	0.0001
2.155 V	737.094	9.737	0.360	0.005	0.345	0.0001

It is expected that the shaper reference voltage should only influence the baseline of the shaper output. Therefore it is expected that changing the shaper reference voltage should not influence the gain in anyway and as such the slope should be unaltered. In Figure 6.62 there are three histograms, one for each shaper reference voltage, for the slope values of all 128 channels that were tested. The three histograms, for reference voltages of $V_{SHA} = 2.406$, 2.280 and 2.155 V, result in a mean slope value for all the channels of 0.0619, 0.0619 and 0.0618 ADC/keV respectively. These values prove that the front-end gain is independent of the shaper reference voltage.

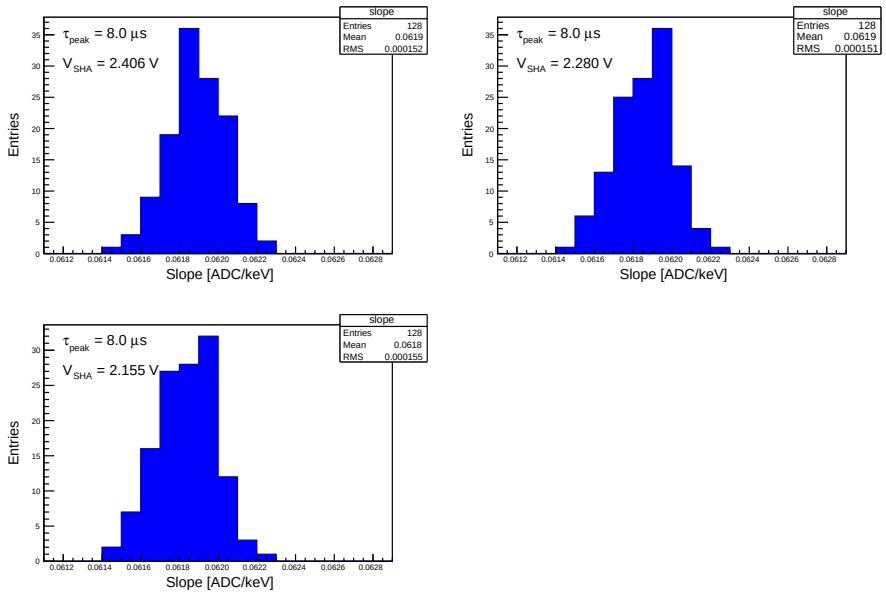


Figure 6.62: The slope values of 128 channels of an ASIC have been histogrammed for three different shaper reference voltages in electron mode for a peaking time of 8 μs. The mean value for each histogram shows that the slope does not change with shaper reference voltage.

The results show that altering the shaper reference voltage does alter the baseline of the signal at the shaper output and directly alters the intercept ADC value. The relationship between the intercept ADC and shaper bias voltage V_{SHA} has been determined and the gain of the shaper remains constant for different reference voltage settings.

Front-End Non-Linearity

Any non-linearities of the front-end can be observed by comparing the front-end output to an ideal response. This has been done for every single channel by fitting a straight line to the ADC vs input pulse relationship to calculate the average gain (slope). The linear fit has a fixed slope across the entire dynamic range and a known intercept value which allows for an ideal ADC value to be calculated for each test pulse amplitude. The ideal straight line response is then plotted and the ADC value of the real data at each pulse amplitude is subtracted the from the ADC value of the linear fit. The difference between the two will reveal small non-linearities within the front-end response at any point across the dynamic range. Using this technique, the deviation of the front-end performance from an ideal linear repsonse can be measured in units of ADC. The calculated non-linearity (NL) for a given test pulse

amplitude i is obtained via the following expression

$$\mathrm{NL}(i) = \mathrm{Fit}(i) - \mathrm{Data}(i) \ , \tag{6.15}$$

where i corresponds to the digital number of the test pulse ($i = 0 - 255$), Fit(i) is the ADC value of the ideal straight line fit and Data(i) is the measured ADC value for the same test pulse.

The difference between the ideal response and measured data is plotted for both modes in Figure 6.63 and Figure 6.64, where the non-linearity of the whole front-end and test pulse injection circuit is shown. The results show all channels of the ASIC have a non-linearity, which deviates from an ideal response by up to approximately 10 ADC across the majority of the dynamic range. A deviation of 10 ADC (0.24% of the ADC range) is approximately 160 keV according to the measured average ADC bin width. The largest non-linearities are observed for the smallest test pulse amplitudes of $V_{test} < 2$ MeV, where the difference between the data and fit is as large as 20 ADC. Large non-linearities occur for small amplitude signals due to the constant current feedback of the preamplifier. The constant current feedback of the preamplifier results in a continuous small quantity of charge being integrated onto the feedback capacitance. For large signals, this additional current accounts for an insignificant fraction of the total charge, but for small signals the additional charge makes up a more significant portion of the total charge.

For both electron mode and hole mode, abrupt changes in the non-linearity can be seen to occur across the entire dynamic range at fixed intervals. Across the full dynamic range there are a total of seven regions where a sharp discpreancy occurs between the measured ADC and the ideal output. The first notable discrepancy occurs for a test pulse of approximately 8 MeV and the second occurs at approximately 16 MeV. A quick observation confirms the existence of a sudden deviation from the ideal output at intervals of every ≈ 8 MeV. A better understanding of this observation can be obtained by examining the test pulse amplitude in its digital number form. In Figure 6.65 the non-linearity is plotted for both modes and the vertical grid lines indicate the test pulse values at which the non-linearities occur.

As mentioned previously, the test pulse amplitude is programmed via an 8-bit binary number thus allowing $2^8 - 1 = 255$ possible digital numbers for the pulse amplitude. The digital numbers (test pulse amplitudes) at which the deviations occur are presented in Table 6.23 along with their binary equivalent. For example, at digital number 16 the amplitude of the injected test pulse is significantly smaller

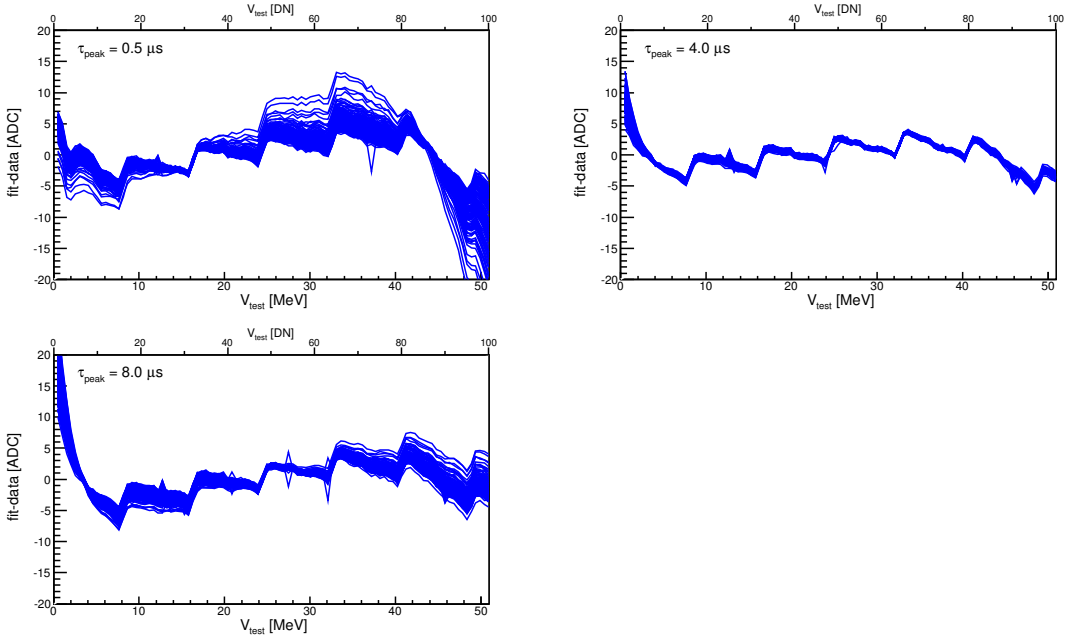


Figure 6.63: The ADC value measured at each test pulse has been subtracted from the straight line fit for three peaking times in electron mode. Only the data from V_{test} =1-100 DN has been fitted.

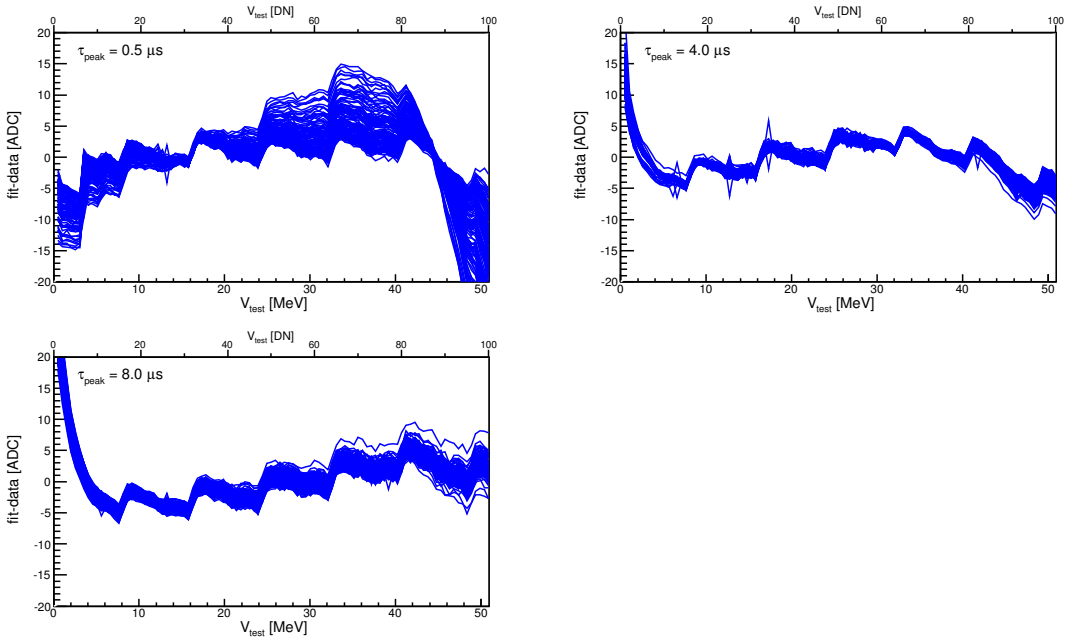


Figure 6.64: The ADC value measured at each test pulse has been subtracted from the straight line fit for three peaking times in hole mode. Only the data from V_{test} =1-100 DN has been fitted.

than the expected output according to the relationship seen for digital numbers 1-15. This feature is seen to be repeated for digital numbers that are multiples of 16, and can hence be attributed to the differing DAC properties of the test pulse injection. The pulser uses an 8-bit DAC where the 4 least significant bits LSBs) control values of V_{test} = 1-15 and one of the 4 MSBs (most significant bit) is changed every 16th digital number. The sharp non-linearities are due to a different linearity of the 4 MSBs relative to the 4 LSBs.

The discrepancies seen in the non-linearity can be attributed to non-linearities of the test pulse injection and are not associated with the analogue front-end or ADC. This means that the real front-end non-linearity is, at the very least, better than the measured non-linearity shown here. Unfortunately it is not possible to precisely determine the non-linearity of the front-end using test pulse injection system alone.

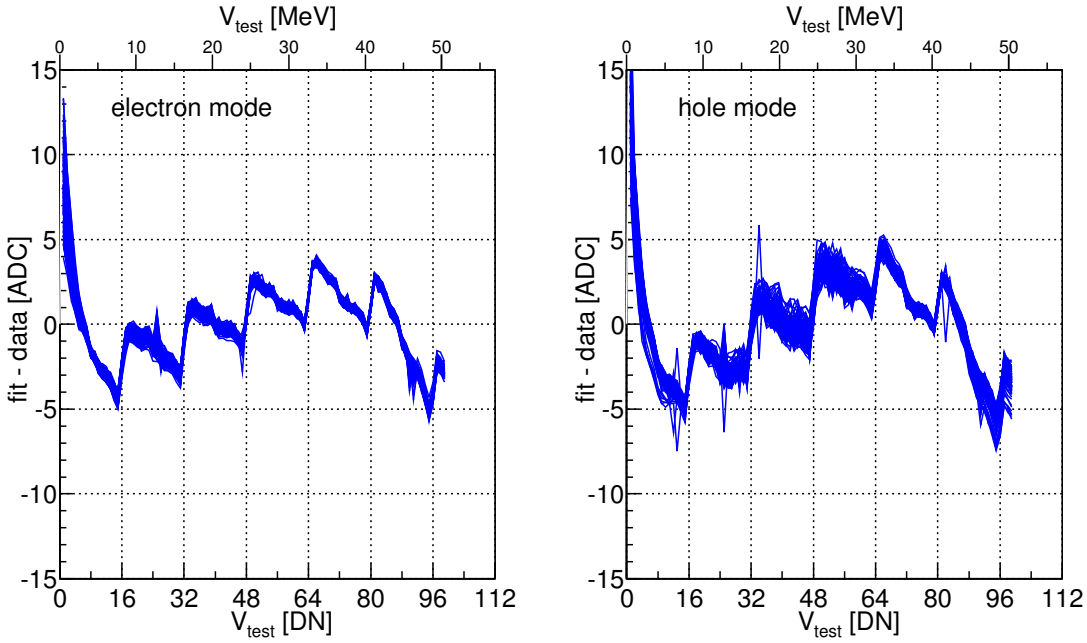


Figure 6.65: Non-linearities for both hole and electron mode are observed at the same test pulse amplitudes.

The irregularities of the test pulse amplitude at certain amplitudes, means that fitting a straight line to the measured linearity data produces a fit that is heavily influenced by the sudden non-linearities in the test pulse. The test pulse non-linearities can be somewhat circumvented by fitting the data for only the test pulse amplitudes in a range where none of the MSBs are changed. Fitting the data for the ranges V_{test} = 1-15, 17-31, 33-47, 49-63, 65-79, 80-95 and 97-111 will provide a measurement of the non-linearity which is independent of the mismatch between

Table 6.23: The digital numbers at which large non-linearities occur are shown along with their binary equivalent form.

Digital No.	Binary
16	00010000
32	00100000
48	00110000
64	01000000
80	01010000
96	01100000
112	01110000

the 4 MSBs and 4 LSBs. The results of the mean slope and mean intercept values obtained by fitting only within these ranges are shown in Table 6.24. The result of fitting for only the range V_{test} = 33-47 DN is shown in Figure 6.66. The data demonstrates that by fitting only within ranges where the MSB does not change, it is possible to achieve a highly linear ADC vs V_{test} plot with almost all channels having a deviation of less than ± 1 ADC from an ideal straight line fit.

Table 6.24: The mean slope and intercept values from performing a straight line fit to data in ranges where only the 4 LSB of the pulse injection DAC are changed.

V_{test} [DN]	Slope [ADC/keV]		Intercept [ADC]	
	Mean	RMS	Mean	RMS
1 - 15	0.0601	0.000296	248.250	9.010
17 - 31	0.0612	0.000126	245.719	9.303
33 - 47	0.0613	0.000112	248.406	9.183
49 - 63	0.0612	0.000114	254.125	9.446
65 - 79	0.0610	0.000114	264.781	9.173
80 - 95	0.0606	0.000114	285.719	9.788
97 - 111	0.0606	0.000116	287.438	9.093

6.11.3 ADC Non-Linearity

The ASIC is equipped with a built in test pulse injection circuit which has an 8-bit resolution. This granularity is not sufficient to test every possible output code of the 12-bit ADC. More precise testing of the ADC linearity has been conducted by the ASIC designer at Rutherford Appleton Laboratory using an external test pulse

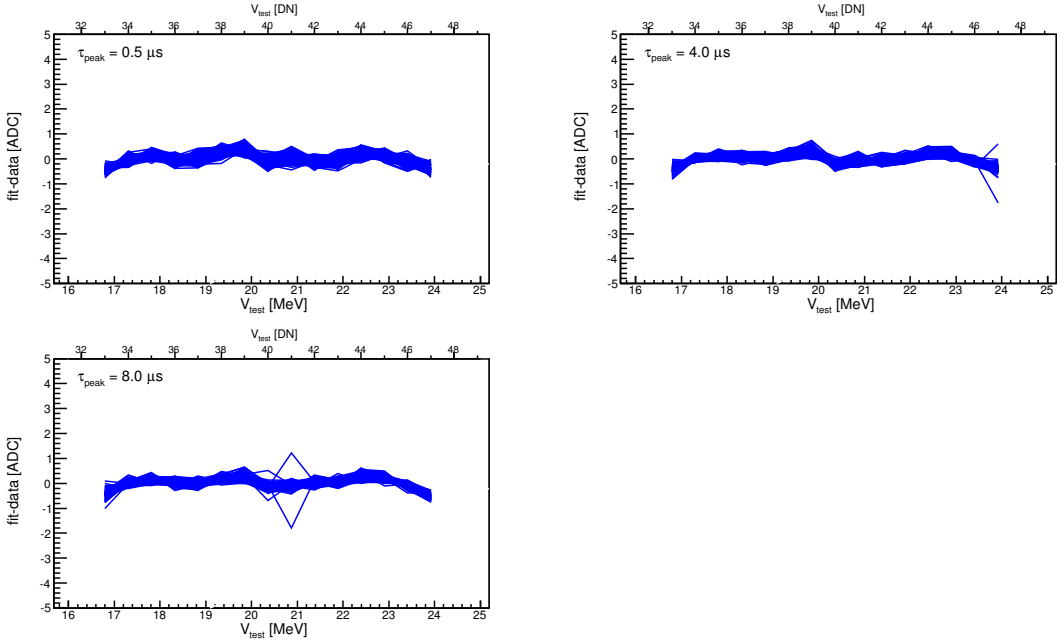


Figure 6.66: The ADC value measured at each test pulse has been subtracted from the straight line fit for three peaking times in electron mode where only the data from V_{test} = 33-47 DN has been fitted.

injection with much finer granularity (greater than 16-bit). These tests focussed specifically on the non-linearities associated only with the 12-bit ADC. The external test pulse has been used to inject pulses directly into the ADC via the ADC bondpad.

In order to understand the differential non-linearity (DNL) and integral non-linearity (INL) [52] [53] for a 12-bit ADC, a test pulse with a step size much smaller than

$$1 \text{ LSB} = \frac{2}{2^{12}} = 0.4883 \text{ mV} , \tag{6.16}$$

is required in order to measure the response for individual ADC output codes. The DNL is a property of the ADC, which concerns the actual width of each ADC bin compared to the ideal value of 1 LSB. The DNL may be tested by measuring what change in input voltage is required for a change in ADC output code. For an ideal ADC, which has a DNL value of 0 for every output code, the difference between each ADC code transition is 1 LSB. For an ideal ADC, an increase in the input voltage of 1 LSB would result in a change in the ADC output code. In reality, a real ADC may sometimes have an output which holds the same value for more or less than 1 LSB. If the ADC holds the same output code for 2 LSB, this effectively means that the ADC bin is twice as wide as ideally expected which results in DNL = + 1 LSB. A positive value of DNL means the ADC output code remains constant for a voltage

greater than 1 LSB. Conversely, it is also possible for the output code of a real ADC to hold the same value for an input voltage less than 1 LSB thereby having a DNL less than 0. The equation by which differential non-linearity is calculated is

$$\mathrm{DNL}(i) = \frac{V_{in}(i+1) - V_{in}(i)}{V_{LSB}} - 1 \ , \tag{6.17}$$

where i is the ADC output code, $V_{in}(i)$ is the transition input voltage corresponding to the ADC output code i, $V_{in}(i+1)$ is the transition input voltage corresponding the next ADC output code $i+1$ and V_{LSB} is the ideal voltage separating neighbouring ADC codes. A transition voltage is defined as the input voltage for which there is an equal probability that the ADC will ouput either of the flanking codes. Inspection of equation 6.17 shows that if $V_{in}(i) = V_{in}(i+1)$, the ADC output code has no associated physical input voltage which is what is known as a missing code and results in a value DNL = -1.

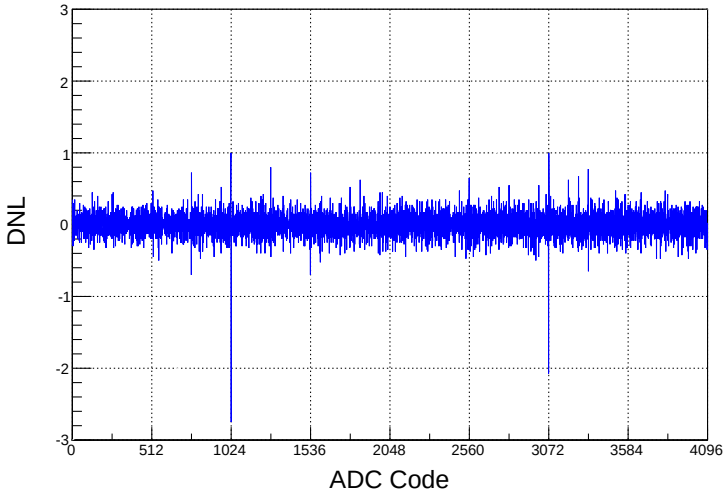
The INL is another property of the ADC which quantifies the maximum deviation of the ADC output code from an ideal ADC response represented by a straight line. The INL of an ADC is firstly measured by sweeping the input voltage across the entire ADC dynamic range and measuring the voltage at which all ADC output code transitions occur. A plot of the ADC output code against the voltage input signal yields a transfer function for which a straight line of known slope and intercept can then be fitted. An alternative to fitting a straight line is to plot a straight line connecting the two end points of the transfer function. The INL is the difference between the voltage at which the real code transition occurs and the ideal transition voltage. The INL for an output code i is expressed as

$$\mathrm{INL}(i) = \frac{V_{in}(i) - (V_{LSB} \times i + V(0))}{V_{LSB}} \ , \tag{6.18}$$

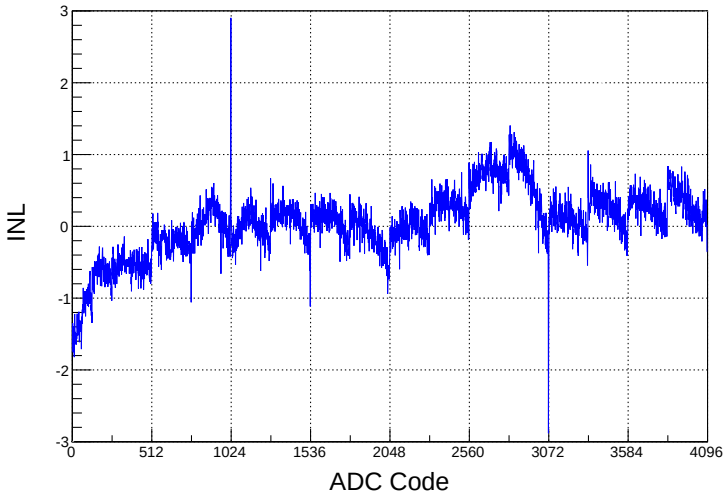
where $V(0)$ is the input voltage corresponding to the 0th ADC code transition and $V_{in}(i)$ and V_{LSB} are previously defined for DNL. The term $V_{LSB} \times i + V(0)$ represents the ideal linear response. Therefore, the difference between the ideal ADC output code and the real ADC output code is determined as a fraction of 1 LSB. The INL for a given ADC output code is an accumulation of all DNL values of the previous output codes, hence it is given the name integral non-linearity and the INL and DNL are related via the expression

$$\mathrm{INL}(n) = \sum_{i=1}^{n-1} \mathrm{DNL}(i) \ . \tag{6.19}$$

The measured DNL and INL values for the ASIC's 12-bit ADC are plotted in Figure 6.67a and Figure 6.67b respectively. At ADC output codes of 1024 and 3072, the DNL and INL values clearly exhibit the presence of missing codes where there is no physical input voltage that corresponds to these ADC values.



(a) The measured differential non-linearity (DNL) of the 12-bit ADC.



(b) The measured integral non-linearity (INL) of the 12-bit ADC.

Figure 6.67: The properties of every ADC output code has been tested using a high granularity external pulse injection.

6.12 Modifications for ASIC Version Three

The findings of the ASIC version two functionality testing revealed several issues which have been addressed for ASIC version three, the final production version. The two key issues that have been addressed relate to the preamplifier and the properties of the ADC.

The front-end exhibited the greatest non-linearities when small test pulse amplitudes were injected. For test pulses less than 5 MeV, the non-linearity was particularly sizeable with some channels measuring a difference of up to 20 ADC compared to an ideal straight line fit. These large non-linearities were believed to be associated with the constant current feedback circuit of the preamplifier. The preamplifier is equipped with a leakage current compensation circuit and a constant current feedback circuit. For version two, the constant current feedback resulted in an small continuous quantity of charge being integrated onto the feedback capacitance to provide stability. The constant current feedback thereby adversely affected the ASIC's performance for measuring the smallest signals.

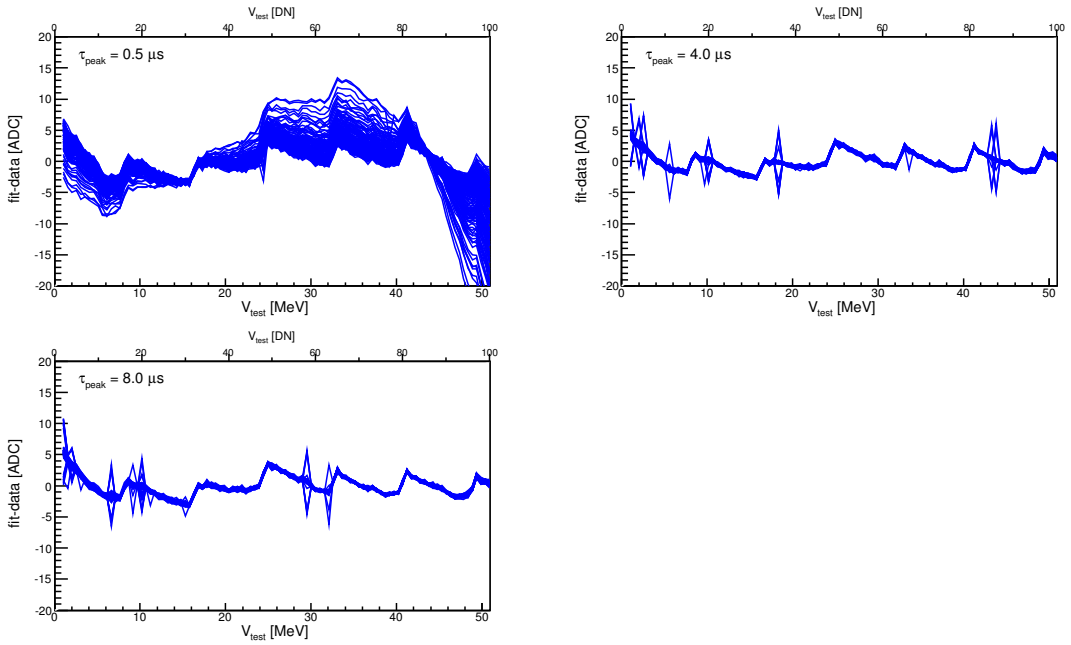


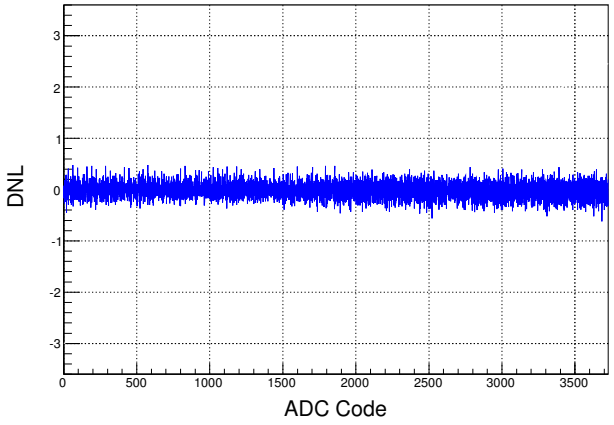
Figure 6.68: The measured non-linearity for ASIC version three showing a more linear response for small amplitude pulses. Only the data from V_{test} = 1-100 DN has been fitted.

For ASIC version three, the constant current feedback circuit has been altered to improve the performance for small amplitude signals. A resistor was removed from

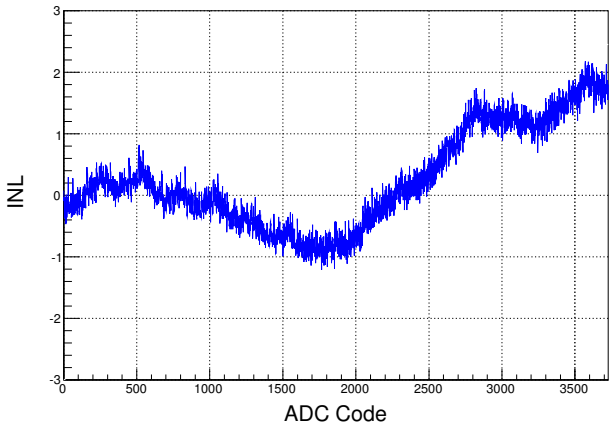
the constant current feedback circuit which means that the circuit has now been disabled. A front-end linearity test was carried out for ASIC version three using the exact same processes as in section 6.11. The result of calculating the difference between the measured front-end linearity (ADC vs V_{test}) and an ideal straight line fit is plotted in Figure 6.68 for ASIC version three. The sharp non-linearities are still observed at pulse amplitudes of 16, 32, 48, 64, 80, 96, 112 DN as the test pulse DAC non-linearity has not been addressed. When comparing the results for ASIC version three with the same measurement for ASIC version two (see Figure 6.63 and Figure 6.64), it is clear that the front-end non-linearity for ASIC version three is significantly improved. For version two, the non-linearity was measured to be as large as 20 ADC for the smallest signals ($\approx$ 1 MeV) and the non-linearity increased as the pulse amplitude decreased. For version three, the measured front-end non-linearity is approximately 5 ADC for a 500 keV test pulse. The maximum observed non-linearity NL_{max} can be quoted as

$$\mathrm{NL}_{max} = |\mathrm{Fit}(i) - \mathrm{Data}(i)| \approx 5 \text{ ADC} . \tag{6.20}$$

The second key improvement for ASIC version three is the redesigned 12-bit ADC. For version two it was shown during the DNL and INL measurements that missing ADC output codes existed at 1024 and 3072. For the final ASIC version this has been rectified so that all ADC codes from 0-4095 are present and as such the ADC has improved linearity. The results of the INL and DNL measurements have been carried out by the ASIC designer at Rutherford Appleton Laboratory and are included in Figure 6.69b.



(a) DNL measurement showing no missing codes.



(b) INL measurement showing no missing codes.

Figure 6.69: The measured differential non-linearity (DNL) and integral non-linearity (INL) for the 12-bit ADC of ASIC version three.

6.13 Summary of Results

An investigation of the key performance criteria for the ASIC's front-end has been performed and the findings of each test are as follows:

- ***Stability Over Time*** - Multiple tests were carried out using the same register settings and injecting a fixed number of test pulses into every channel of an ASIC. The mean ADC values that were measured for the different tests were compared and determined to be within 1 ADC of each other, when comparing data for the same front-end channel. A small number of channels were observed to measure mean ADC values that differed by more than 1 ADC for the separate tests. Tests that were carried out several weeks apart measured a mean ADC value differing by less than 2 ADC, when comparing data for the same channel.

  Tests on the same day showed a higher level of consistency compared to tests taken weeks apart. For a programmed shaping time-constant of 4.0 μs, all channels were observed to have an RMS noise in the range 0.75-1.05 ADC, which indicates an RMS noise in the range 12-17 keV.

- ***Readout Timing Logic*** - A variety of register settings have been tested to alter and understand the timing and sequence of the readout logic signals. The timing of the readout sequence has been investigated by changing register 4 and register 3. It has been shown that it is possible for the readout timing logic and the width of the test pulse to be configured in such a way that the readout is triggered twice for a single injected pulse. It has been deduced that the falling edge of the test pulse must occur prior to all of the reset signals to prevent undershoot effects from causing the energy comparator to fire more than once for the same pulse. It was initially expected that a falling edge occurring prior to the end of the peak-hold reset signal would ensure normal readout conditions. However, the occurrence of undershoot effects, which occur when the test pulse amplitude is restored to the baseline, can be greater than several microseconds in duration. The undershoot can subsequently be shaped and hence cause the energy comparator to fire thus resulting in a second readout for the same injected pulse.

  It has been shown that register 4 (DAPB) can be implemented to change the time at which the pulse amplitude is sampled and also the time at which the

reset signals begin. It has been demonstrated that register 3 can be utilised to enable alteration of the peak-hold reset duration.

- ***Energy Threshold*** - The comparator which receives shaped signals has been trimmed for both electron and hole mode for every channel for three different shaping time-constants. A trim DAC has been successfully programmed to finely adjust the baseline signal of every channel so that all channels have the same threshold conditions at the energy comparator. The trimming procedure was carried out using noise generated hits to determine the required DAC value (offset) for each channel of an ASIC, in order to align the baseline and threshold signals for an energy threshold setting of 128 DN (1.5 V).

  After trimming, a scan of the energy threshold reference voltage Eth (register 15) revealed the number of channels that were succesfully trimmed for an energy threshold setting of 128 DN (1.5 V). The minimum noise level was determined for each channel, by scanning the energy threshold and observing the number of hits for threshold settings greater than 128 DN. The minimum signal amplitude that the ASIC can measure has been deduced to the nearest threshold setting (1 DN $\approx$ 25 keV). The highest percentage of successfully trimmed channels was achieved for electron mode using a shaping time-constant of 8.0 μs and the worst alignment was for a shaping time-constant of 0.5 μs for electron mode. Hits generated at energy thresholds greater than 128 DN are attributed to noise at the energy comparator input.

  For electron mode, a threshold voltage equivalent to 100 keV (132 DN) resulted in no hits for shaping time-constants of 4.0 and 8.0 μs, but the 0.5 μs data set suffered from much greater noise and required a threshold of 150 keV (136 DN). For hole mode, a threshold setting equivalent to 75 keV (131 DN) resulted in only a single channel recording a hit for a shaping time-constant of 0.5 μs, whilst the 4.0 μs and 8.0 μs shaping-time constants recorded no hits for a threshold setting of 131 DN. The smallest amplitude signal that can be detected for electron mode must be greater than 100 keV, and for hole mode the smallest detectable signal must be greater than 75 keV.

- ***Timestamp Threshold*** - The comparator which receives signals from the preamplifier via the $\times$10 gain amplifier ($PRE10$) has been trimmed using noise generated hits. Using the trim DAC, the comparator has been trimmed for both modes to determine the minimum detectable signal amplitude, at

the time comparator, which can generate a timestamp. The comparator's programmable reference voltage Tth and the baseline signal from the $\times 10$ gain amplifier V_{PRE10} were aligned for a threshold of $Tth = 128$ DN.

After trimming, a scan of the threshold voltage has been performed to determine the noise level for each channel. All channels were successfully trimmed for electron mode but a very small number of channels were not correctly trimmed for the hole mode data. Very little variation is observed when trimming is performed with different shaping time-constants as expected, unlike for the energy threshold comparator trimming. For electron mode, there are no channels with a noise level exceeding 75 keV (125 DN) and all shaping time-constants show similar behaviour. For hole mode, the three shaping time-constants show a similar noise level with all but two channels recording a maximum noise level smaller than 75 keV (125 DN). A timestamp threshold setting of $Tth = 125$ DN resulted in only one or two channels firing, due to high noise levels or mistrimming for the three shaping time-constants that were tested, for both modes.

- ***Shaping Time-Constant*** - All possible shaping time-constants and sampling times have been tested by using every possible register 4 setting available (256 possible settings). The peaking-time was measured using two independent techniques. For every shaping time-constant, the peak amplitude was observed later than the expected peaking time but always within 0.5 μs of the expected value. This small discrepancy between measured peaking time and expected peaking time could possibly be attributed to variation of shaper capacitances or the timing resolution capabilities of the two measurements.

  It was observed that sampling at different times after the peak amplitude resulted in a variation of the mean ADC of $\pm$ 2-3 ADC for electron mode. For hole mode, the mean ADC was seen to increase for larger sampling times with variations of up to 20 ADC. The dependency of the RMS noise was investigated for different shaping time-constants and the minimum RMS noise of $\approx$ 0.8 ADC (13 keV) was observed for both electron mode and hole mode for a shaping time-constant of 2-2.5 μs. Some integer values of shaping time-constant for the hole mode setting showed slightly higher RMS noise than the non-integer time-constants when sampling close to the peak-amplitude, but for electron mode no such relationship was observed. Both modes experience the largest RMS noise for a shaping time-constant of 8.0 μs (electron mode

RMS $\approx$ 1.4 ADC and hole mode $\approx$ 1.7 ADC).

The dependency of the RMS noise on pulse amplitude and rate was also investigated for different shaping time-constants using test pulse amplitudes covering the full dynamic range and pulse rates up to the maximum 5 kHz. A larger RMS noise was measured for larger pulse amplitudes when using large shaping time-constants but at small time-constant values the effect was noticeably reduced. Similarly, a larger RMS noise was observed for faster pulse rates at large shaping time-constants but at smaller time-constants the effect was lessened but still present. A shaping time-constant of 2-3 μs should result in minimising the system noise for both large and small amplitude pulses as well as fast pulses whilst allowing a relatively small system dead-time.

- ***Front-End-Linearity*** - A test of the linearity for the entire front-end and test pulse injection system was conducted for both modes for three shaping time-constants. All possible test pulse amplitudes were injected until the ADC became saturated. The dynamic range of the ADC was investigated and compared to the value of 2 V quoted in the specifications. It has been shown that a test input voltage of 0.975 V, theoretically results in a 2.022 V signal at the ADC input. A test was conducted with a test voltage amplitude of 0.975 V (125 DN) which saturated the ADC of all channels in electron mode and all but three channels in hole mode. A test voltage of 0.967 V (124 DN), which theoretically results in a 2.007 V signal at the ADC input, did not result in saturation of all channels for electron mode and six channels remained unsaturated for hole mode.

  The relationship between meaured ADC and test pulse amplitude was studied and the gain (slope) of each channel was calculated via a straight line fit. The front-end gain, for the dyanmic range 0-50 MeV, was calculated and the average ADC bin width has been shown to be between 16.29 and 16.10 keV for both modes for all tested shaping time-constants. The measured values compare well with the theoretically calculated value of 16.20 keV. The small variation in gain for different shaping time-constants has been attributed to slightly differing capacitances at the shaper, for the different time-constants, resulting in different shaper gains. Using exact values for the shaper capacitances, an ideal value for the shaper gain of $A_{sha} = 0.96$ was calculated. It was thus shown that if the shaper gain is equal to 0.96, the preamplifier gain for test pulse injection is $A = 2.06$, the expected ADC bin width according to

theoretical calculations is 16.20 keV.

The ADC value corresponding to the smallest signal amplitude (intercept ADC) was analysed for each channel and succesfully related to the programmed shaper reference voltage. It was subsequently proved that the intercept ADC could be altered by changing the value of the shaper reference voltage. Three different shaper reference voltages were tested using the same settings for all other registers.

Non-linearities in the front-end have been revealed by plotting the difference between the measured ADC and an ideal ADC (from straight line fit) for each channel. Sudden non-linearities were observed at certain pulse amplitudes due to non-linearities in the pulse injection circuitry. Across the dynamic range of 0-50 MeV, the largest non-linearities (up to 20 ADC) were observed for small pulse amplitudes < 2 MeV. Across the remainder of the dynamic range, variations of up to $\pm$ 10 ADC from the ideal response were observed. The linearity of only the ADC has been tested by the ASIC designer, using an external pulse injection system, and missing ADC output codes were discovered which have since been rectified for the newest ASIC version.

Chapter 7

Conclusion and Discussion

The R^3B experimental setup has been outlined and the properties of the various particles, which are intended to be measured, have been explained. An overview of the different detector technologies has been given and the demand for the inclusion of a silicon micro-vertex tracker is justified. The silicon tracker will provide high resolution position measurements for charged particles which will be useful for a wide range of possible experiments at R^3B.

The initial design of the tracker included three layers of double-sided-silicon. At the time of writing this thesis, the minimum tracking configuration of two layers has been completed with the possibility of constructing a third layer in the future. There are a sufficient number of detectors to form one inner layer and one outer layer with several spare detectors available for each layer. The design considerations and geometry of the assembled silicon tracker has been explained along with a discussion of the reasons for utilising a lampshade geometry. The initial design included an additional outer layer to negate the effect of dead channels in the two other layers. The results of the silicon quality assurance tests have shown there to be a very small number of dead strips present in the final detectors, so that the absence of a third layer should result in very little reduction in efficiency.

7.1 Silicon Quality Assurance

The four types of silicon sensor that have been used for detector construction have been described and the quality assurance process, by which sensors were deemed to be acceptable, has been explained. All sensors were subjected to the quality assurance process and the percentage of acceptable sensors varied depending on sensor

type. The most common reason for a sensor failing the quality assurance process was due to high current (leaky) strips, which could only have been observed by probing individual strips. Without the probe station, many faulty sensors would have passed the quality assurance testing which would have resulted in many detectors with high current strips. The probe station has ensured that detectors have been constructed for which the total number of dead strips is much less than the initial target of 3%. All constructed detectors have a total number of dead strips that is less than 1% of the total number of strips.

The silicon manufacturer quotes a minimum value of 53 V to achieve full depletion for every type of sensor. All IV measurements were carried out from 0 to 200 V and the lifetime tests used a fixed voltage of 150 V. For all probe station testing, a fixed reverse bias voltage of ±65 V was applied to one side of the sensor and the side to be probed was grounded. The probing data reveals a consistent leakage current across the entire sensor on the strips of the n-side, as expected. On the p-side there is a significant variation in leakage current across localised areas of the sensor with some regions measuring a leakage current up to two times greater than other regions. This localised variation in leakage current on the p-side is due to incomplete lateral depletion of the silicon on the junction side. A later test, whereby a D sensor was probed using a range of voltages from 65-165 V, proved that the localised variation in leakage current on the p-side is not present at larger bias voltages. This confirms that a reverse bias voltage greater than 65 V is required to achieve full lateral depletion on the junction side.

A process was developed whereby the silicon sensors, carbon fibre frame, ASIC, PCB and copper block were combined to form a complete detector. Throughout the construction process, IV measurements were taken at different stages to identify whether the sensor's characteristic IV behaviour had been altered. The data obtained for the final IV measurement for every completed detector has been presented.

7.2 R^3B ASIC

The R^3B ASIC has been custom designed specifically for the needs of the silicon tracker and is envisaged to form the front-end electronics for other future detector systems. The ASIC specifications, key functions and design have been described in extensive detail. Using ideal calculations, the front-end gain for the ASIC has been calculated as 0.06174 ADC/keV so that a single ADC is equivalent to 16.20 keV.

7.2.1 ASIC Version Two Testing

A range of different tests have been performed using a bare ASIC setup with four ASIC and no silicon sensor connected to the ASIC. The ASIC testing focussed on aspects including reproducibility of results, readout timing logic, energy threshold, timestamp threshold, shaping time-constant and front-end linearity. Results of the testing were compared with the design specifications and used to identify possible defects whilst understanding optimum register settings.

Reproducibility tests showed that data taken several weeks apart can be directly compared as the mean ADC values are within 2 ADC for the same channel and within 1 ADC when comparing data taken on the same day. The readout timing logic can be altered using register 4 to change the sampling time, and register 3 to change the peak hold reset duration. When using the test pulse injection system, it is essential that the falling edge of the test pulse occurs prior to the start of the reset signals to prevent more than one hit occurring for a single test pulse.

The energy threshold has been trimmed using noise generated hits so that every channel of an ASIC has the same threshold conditions. For a tracking detector, where relatively small amplitude signals can be expected ($\approx$ 100-200 keV), the ability to trim the energy threshold and determine the minimum detectable signal amplitude is vital. The programmed energy threshold can be incremented in steps of approximately 25 keV (1 DN). The smallest energy threshold setting which resulted in no hits due to noise was equivalent to approximately 100 keV (4 DN) for electron mode and approximately 75 keV (3 DN) for hole mode. The measured minimum detectable signal level is significantly greater than the 40 keV quoted in the ASIC specifications. A theoretical value for the maximum programmable energy threshold was calculated to be 3.2 MeV.

The timestamp threshold has also been trimmed using noise generated hits so that all channels have the same threshold conditions at the timestamp comparator. For electron mode, a threshold setting equivalent to approximately 75 keV (3 DN) ensured that the timestamp threshold was greater than the noise level for all channels. For hole mode, a threshold setting of 75 keV (3 DN) yielded only two firing channels due to the noise level being greater than 75 keV.

Two different techniques were used to test the shaping time-constant so as to determine whether the observed peaking time and programmed shaping time-constant were in agreement. All possible shaping time-constants were tested and all observed peaking times were found to be within less than 0.5 μs of the programmed time-

constant. The effect of sampling at different times after the peaking time was studied and the variation in measured ADC was of the order 2-3 ADC for electron mode. For hole mode, sampling at different times after the peaking time yielded a measured ADC that varied by up to 20 ADC depending on the sampling time. Therefore, independent hole mode data sets that are taken with the same register settings but only differing by the DAPB (register 4) setting, cannot be directly compared.

The variation in RMS noise due to changes in shaping time-constant was examined to determine the minimum noise configuration. For both electron and hole mode, the minimum RMS noise of 0.8 ADC was observed for the shaping time-constants of 2-2.5 μs. This indicates a minimum RMS noise of approximately 13 keV (30 keV FWHM) which is larger than the value of 8 keV (19 keV FWHM) quoted by the design specifications.

The front-end linearity has been tested for the full dynamic range until saturation of the ADC. The specifications quote a dynamic range of 0-50 MeV, the linearity data analysis only focussed on data within this range. The front-end gain was measured to be within the range 0.0614-0.0621 ADC/keV (1 ADC = 16.10-16.23 keV) for the three different shaping time-constants that were used for testing. The value of 0.0616 ADC/keV obtained for the 4.0 μs shaping time-constant (for both modes) shows a very strong agreement with the theoretical front-end gain calculation (theoretical value = 0.0617 ADC/keV). These values provide substantial confirmation of the validity of both the theoretical calculations and the measurement procedures.

The non-linearity of the front-end was examined by comparing the ADC vs injected pulse amplitude data with a fitted straight line. The difference between the two was plotted for every pulse amplitude that was tested. This revealed non-linearities in the test pulse injection system when specific values for the test pulse amplitude were programmed. The largest non-linearities of up to 20 ADC were observed for the smallest test pulse amplitudes. The results presented for the front-end non-linearity are dominated by the non-linearities in the test pulse injection DAC.

The ASIC designer has tested the ADC linearity using an external test pulse injection system with a much finer granularity than the ASIC's built in test pulse injection circuitry. The ADC linearity has been tested by injecting pulses directly to the ADC, thereby bypassing the front-end functional blocks, and testing every possible ADC output code from 0-4095. The ADC differential non-linearity (DNL) and integral non-linearity (INL) results are included for completeness and expose the presence of two missing codes at 1024 and 3072.

7.2.2 ASIC Version Three Improvements

For the final production version ASIC, key adjustments were made to 12-bit ADC and the linearity has been significantly improved for small amplitude signals. The missing ADC codes, observed for version two, are not present in version three. The constant current feedback circuit for the preamplifier has been disabled for version three which has improved the linearity for small signals.

7.2.3 Future Work

This work has provided the first essential foundation for understanding the properties of the R^3B ASIC and its front-end capabilities with comparative ideal calculations. This work may serve as a useful guide for any future detector systems intending to use the R^3B ASIC for front-end readout purposes. The energy comparator trimming process has given an indication as to the smallest detectable signal amplitude, which is a crucial property of an ASIC for a tracking detector. When the preamplifier of the ASIC is directly coupled to a strip of the sensor, the effect of the strip capacitance may slightly alter the front-end performance. It will be important to repeat some of the ASIC testing, seen in this work, with a fully bonded detector, which will allow the effect of the additional strip capacitance to be determined. Initial detector tests can be repeated with the ASIC's test pulse injection system for a direct comparison with the results in this work. Preliminary detector testing has been carried out at Daresbury Laboratory using a mixed alpha source. The use of a lower energy radiation source or possibly a proton beam is desirable to generate signals of the order of hundreds of keV. This will provide the ultimate test as to whether the noise of the ASIC is sufficiently small, and if the comparator trimming technique is satisfactory to measure signals from traversing high energy protons.

The current number of completed detectors is adequate for the construction of one complete inner layer (six inner detectors) and one outer layer (twelve outer detectors). The detectors will be transferred to Daresbury Laboratory where the full tracker will be assembled, under clean room conditions, with all eighteen detectors mounted within the vacuum chamber. The full tracker assembly will be tested using a radioactive source with the system under vacuum. This will signify the first test of the entire tracker system and data acquisition system prior to installing the system at FAIR in the future.

Appendices

Appendix A

ASIC Functionality Testing

A.1 Pulse Amplitude and Energy Threshold

A test has been conducted using a test pulse of fixed amplitude where several different energy threshold values have been programmed to verify the independence of measured amplitude and energy threshold. Three different energy threshold settings were tested, Eth = 138, 186 and 234 DN (1.08, 1.46 and 1.84 V) whereby the mean and RMS ADC values of 512 pulses were compared. Figure A.1 and Figure A.2 show the results for electron mode and hole mode, where the effect of changing the energy threshold appears to have no influence on the sampled pulse height. The difference in the mean ADC for the different energy thresholds is displayed for electron mode in Figure A.3 and for hole mode in Figure A.4.

The data shows that the difference in the mean ADC measured for the different threshold measurements is within $\approx$ 1 ADC value for both electron mode and hole mode for all channels. For electron mode, the mean ADC values are within 0.5 ADC of each other for all channels, whereas the hole mode shows a slightly larger disparity of ΔMean $\approx \pm$ 1 ADC for some channels. The variation in measured ADC is consistent with the findings in section 6.2, where it was found that measurements taken with the same settings on the same day resulted in a mean ADC that differed by less than 1 ADC.

Table A.1: Settings used for testing the dependency of pulse amplitude and noise on the energy threshold Eth.

DAPB [μs]	τ_{peak}[μs]	Eth [DN]	ΔV [DN] [MeV]	Width (μs)	Delay (μs)
15.0	4.0	138, 186, 234	[26] [13.2]	10.0	600

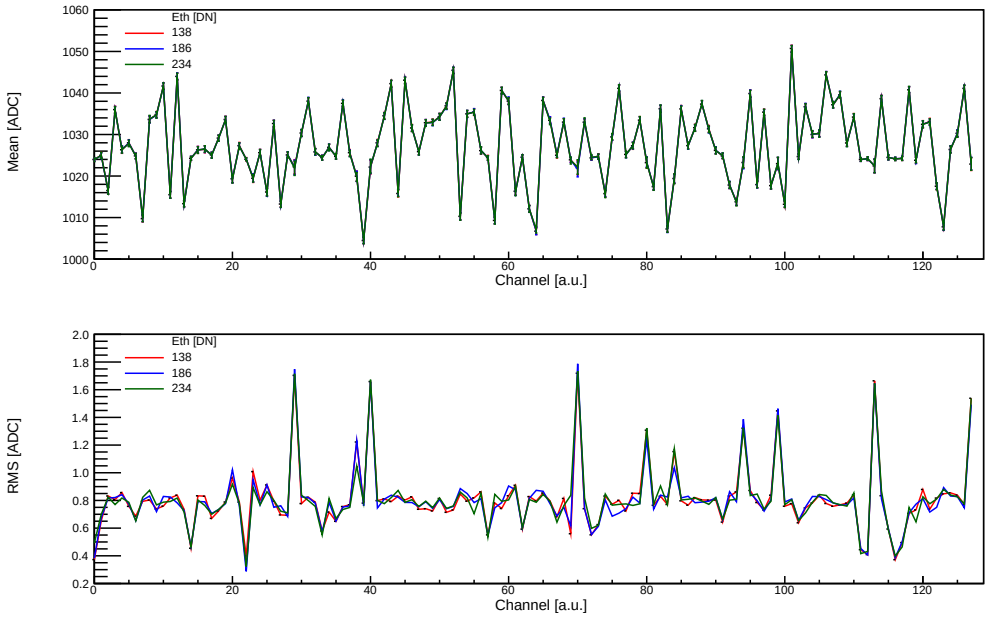


Figure A.1: The mean and RMS ADC values are plotted for electron mode where only the energy threshold Eth is changed.

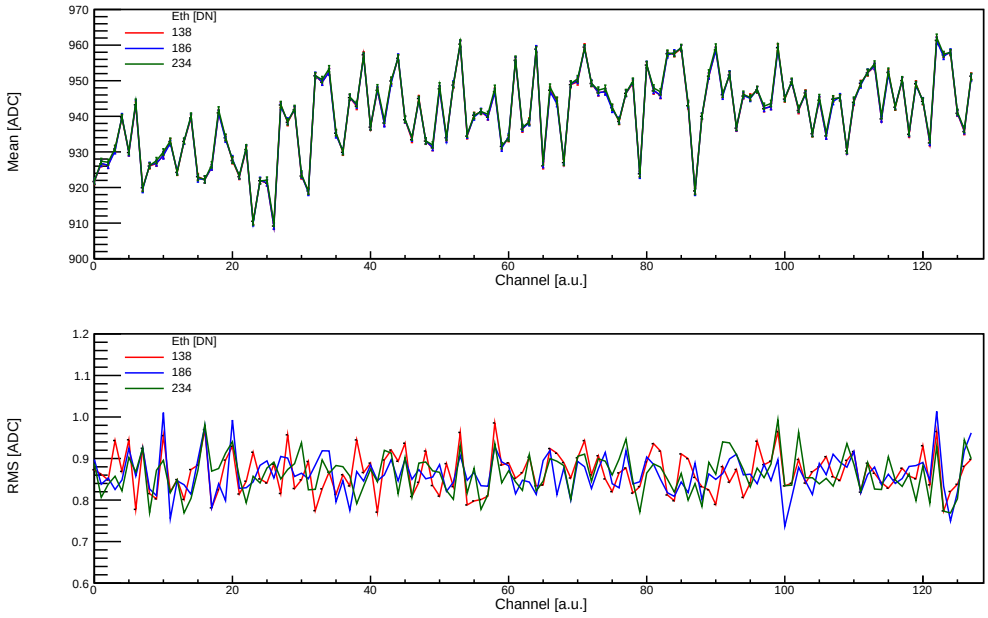


Figure A.2: The mean and RMS ADC values are plotted for hole mode where only the energy threshold Eth is changed.

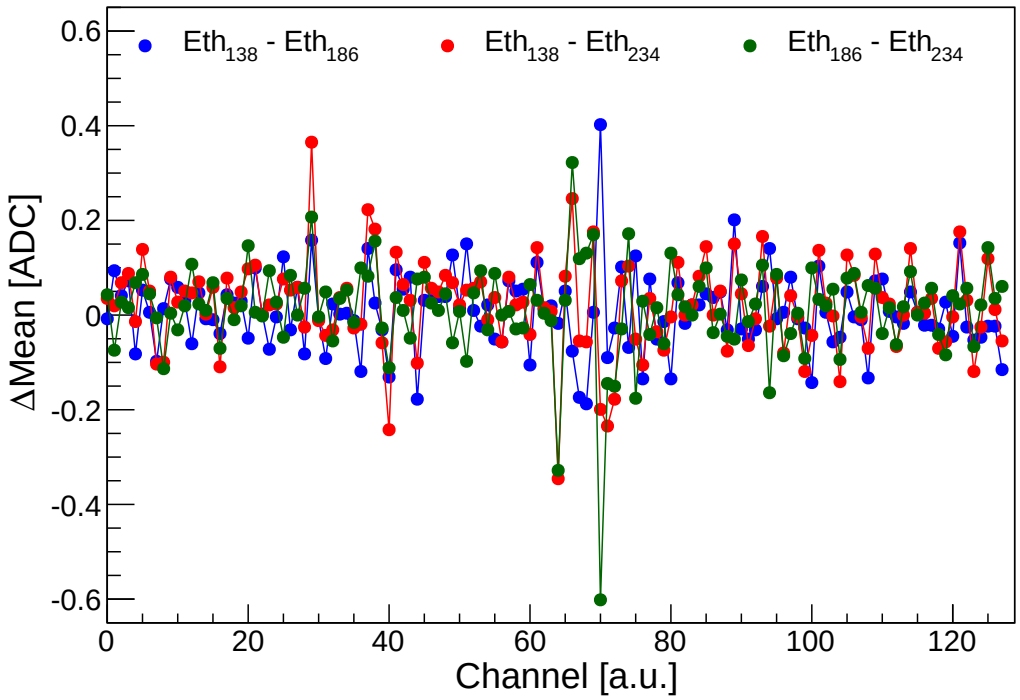


Figure A.3: The difference in measured mean ADC ΔMean is plotted for three data sets with different energy threshold settings for electron mode. The difference in ADC is less than 1 ADC for all channels for all measurements.

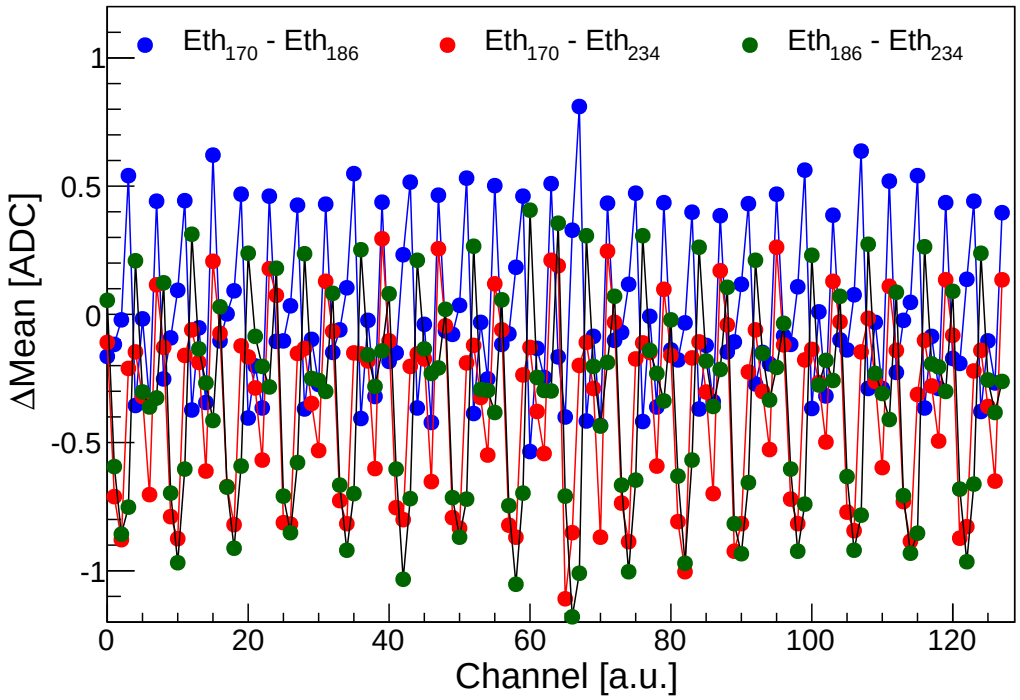


Figure A.4: The difference in measured mean ADC ΔMean is plotted for three data sets with different energy threshold settings for hole mode.

A.2 Peaking Time Measurement

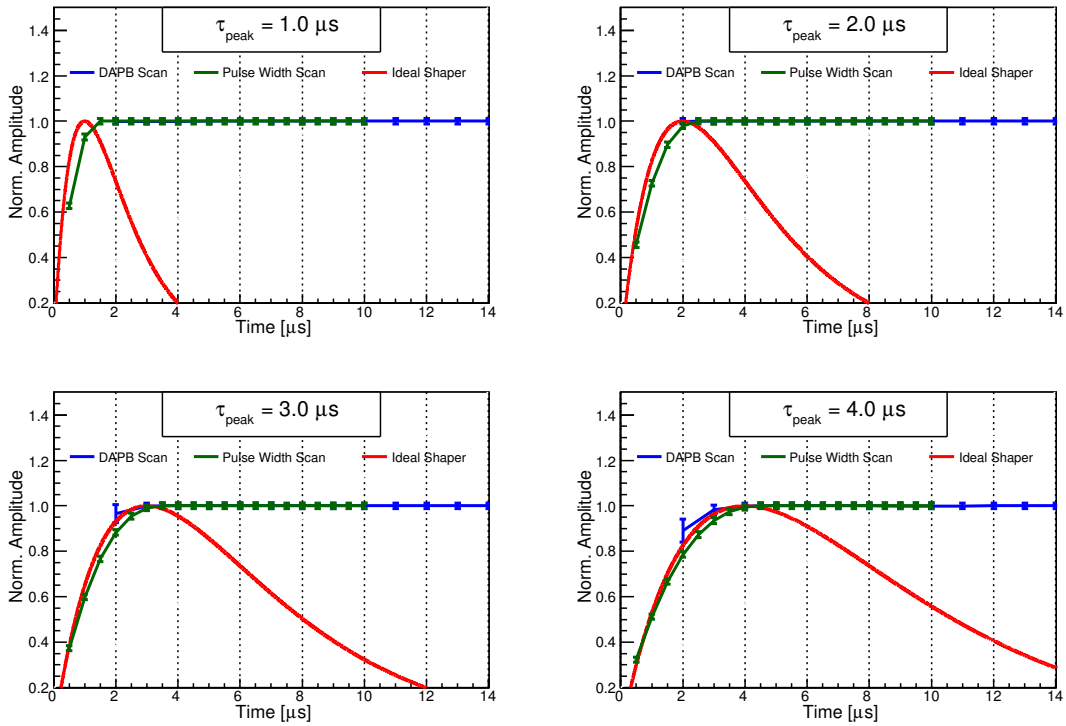


Figure A.5: For electron mode: the two independent measurements of the peaking time of the shaper output are shown for shaping time-constants of 1, 2, 3 and 4 μs along with the theoretical shaper repsonse in red.

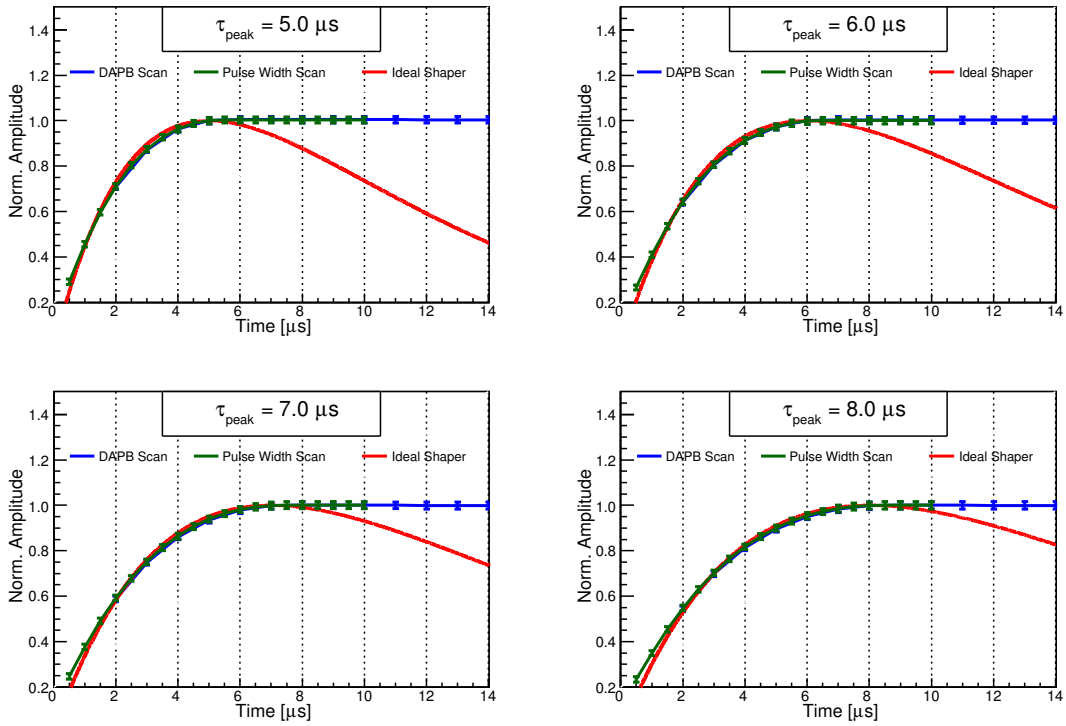


Figure A.6: For electron mode: the two independent measurements of the peaking time of the shaper output are shown for shaping time-constants of 5, 6, 7 and 8 μs along with the theoretical shaper repsonse in red.

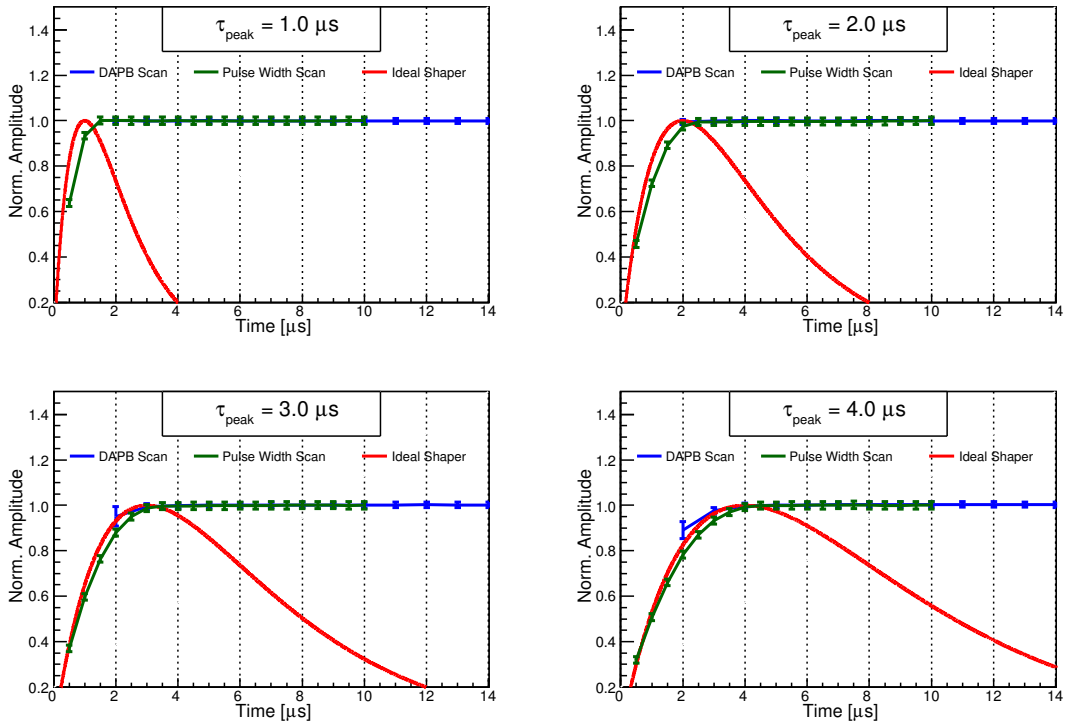


Figure A.7: For hole mode: the two independent measurements of the peaking time of the shaper output are shown for shaping time-constants of 1, 2, 3 and 4 μs along with the theoretical shaper repsonse in red.

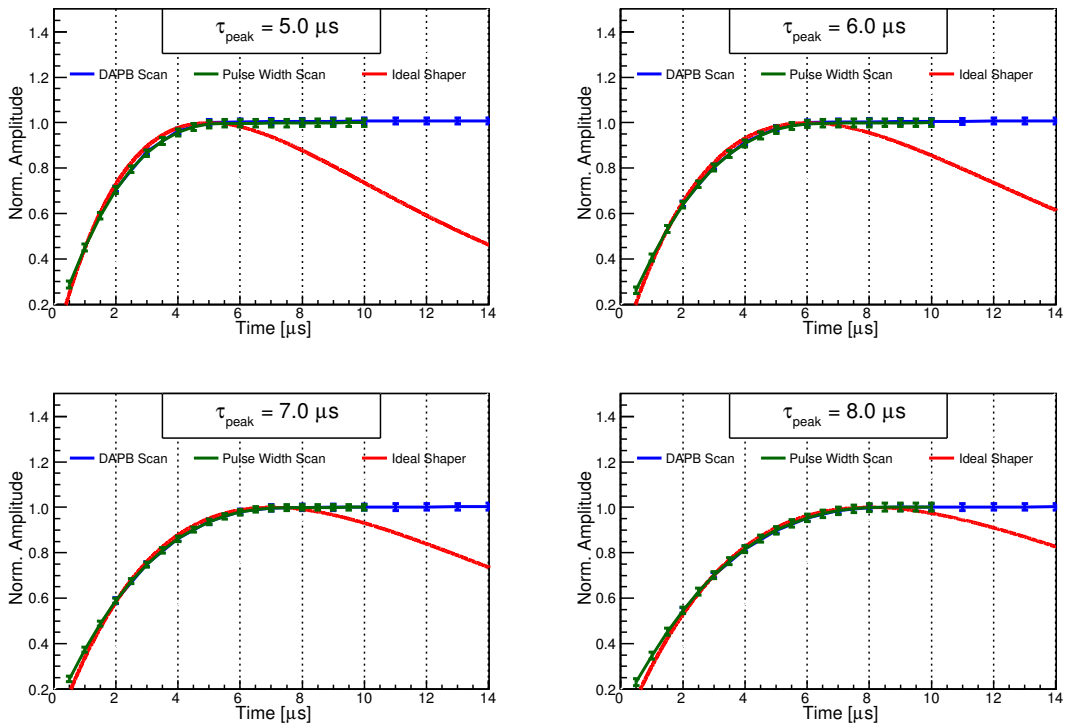


Figure A.8: For hole mode: the two independent measurements of the peaking time of the shaper output are shown for shaping time-constants of 5 6, 7 and 8 μs along with the theoretical shaper repsonse in red.

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