Custom Logic registers including MWD in Lyrtech VHS-ADC cards.

updates to rev 4_1 code- added triggering based on a hit pattern 4.1 updated Aug 2014 to add 1 control bit for sync via GPIO for IDS at CERN
update to rev 4.2- added flag to check that the digital gain doesn't overflow un-noticed. Extra flag only
update 5.2/5.3 added PSA control in register 0x90 upwards and option of PSA data in place of MWD 5.2 fixed integration times, delay always 0, 5.3 programmable integration and averaging

1. Register Memory Map:

Reg add (hex)	**Per card/chan**	**Function**	**Notes**
0-F	Channel	MWD control and status	*2-15 not yet allocated*
10-1F	Channel	MWD Parameters	*Accesses regs inside MWD code*
20-2F	Channel	Other per-channel parameters	*Threshold. 21-2F not yet allocated*
30-3F	Card	Readout parameters (common)	*Trace length etc. 31-3F not yet allocated*
40-4F	Channel	Diagnostics	*Not yet allocated*
50-6F	TBD	Dead time/ live time counters and other diagnostics	*Not yet allocated*
70-7F	Card	Veto, GPIO and TDRI control	
80-8F	Card	Code version data	
90-9F	Card	Used for PSA	
C0-FF	Channel	Reserved for diagnostics	*Not yet allocated*

2. Register Access protocol:

All registers in this document are accessed via user reg 1 and 2.

To **write** the registers in this document:

Write to user reg 1

31			28	27											16	15														0
Chan (0-11)				Register address (0-2047)												Register value (data)														

To **read** the registers in this document, use a 2 stage process:

First write to user reg 2 to define the read address:

31			28	27											16	15														0
Chan (0-11)				Register address (0-2047)												Don't care (0)														

Then read user reg 2

31			28	27											16	15														0
Chan (0-11)				Register address (0-2047)												Register value (data)														

3. MWD Control and Status registers (0x0 to 0xF)

MWD Control Word (r/w register address 0x0; resets or powers up to 0x0001, disabled)

0 Disable MWD (=1) (also resets mwd and TFA to reload new parameters when disabled)
1 Disable Baseline subtraction (=1)
2 Data Shift 0 (lsb) (00 = shift 0; 01 = shift 1; 10 = shift 2; 11= shift 3)
3 Data Shift 1 (msb)
4 Trigger Polarity (0 for +ve preamp signals, 1 for -ve preamp signals)
5 Test_sel bit 0 *(select the MWD test output data word 0 = MWDin, 1= DEC2MAUsig,)*
6 Test_sel bit 1 (*2= MAU2NORM, 3 = Signed ADC (in), 4 = TFA(top), 5= TFA(mid))*
7 Test_sel bit 2 *(6= MWDsig, 7 = trapezsig. Visible via GPIO and TDRI card)*
8 Test_sel digital_gain bit 0 *(00 = x1 read d15-2; 01 = x2 read d14:1;*
9 Test_sel digital_gain bit 1 *(10 =x4 read D13:0, 11 = x8 read d12:0 and lsb = 0)*
10 Enable Hit Pattern triggering input (1 = enable, 0 = disable)
11 OR my trigger with Hit pattern trig locally (1 = OR my trigger, 0 = use only hit pattern trigger1)
12 Use internal trigger (CFD) when =1 or Ext_TRIG = 0 to make this channel's trigger.
(The CFD signal always contributes to the Hit Pattern Trigger regardless of this bit's setting because Ext Trig is common to all channels. This bit is not used when bit 10 = 1 and bit 11=0).
13 Reset ~~tx_rtdex logic and also~~ latched status bits when 1
~~14 When =1, put pileup status on MSB of energy (no pileup information when = 0)~~
~~15 When =1 put ADC over-range status on MSB of baseline (no over-range information when = 0)~~

MWD Status Word (ro register address 0x1)
Bits 4-8 for ch 1 only as diagnostic- not reset until reset signal

0 myready
1 mwd_pileup
2 watch_pu
3 decclk_locked
4 watchdog_happened;
5 received_trigger;
6 started_reading_circbuf;
7 finished_reading_circbuf;
8 got_energy from MWD;
9 mwd_1_active (not latched)
10 waiting4energy (trace sent, but waiting for energy)
11 energy_sent to circ buff
12 reading_flag (not latched)
13 not used
14 short break between MWD Active pulses (10ns)
15 short break between MWD Active pulses (20ns)

MWD Register address 0x2-0xF not used

[1] The neighbour trigger pattern can be set to include this channel's CFD. In this case it might be useful not to trigger with the local CFD signal but wait a few ns for the hit pattern trigger so that all channels start at exactly the same time.

4. MWD Parameter Access- register addresses 0x10-0x1F

MWD Parameter	Register Address
First shaping time	0x10 (16) r/w
Trapezoid shaping	0x11 (17) r/w
peak sample	0x12 (18) r/w
peak separation	0x13 (19) r/w
baseline average	0x14 (20) r/w
baseline update clocks	0x15 (21) r/w
baseline threshold	0x16 (22) r/w
decay time	
decay time (low 16)	0x17 (23) r/w
decay time (top 8)	0x18 (24) r/w
decimation	0x19 (25) r/w
mode	0x1A (26) r/w
read-only from here down	
read zero	0x1B (27) ro
read baseline (low 16)	0x1C (28) ro
read baseline (top 16)	0x1D (29) ro
read energy (low 16)	0x1E (30) ro
read energy (top 16)	0x1F (31) ro

In this case the bus addr lines will be driven from algorithm_register_write_sel(3..0) when algorithm_register_write_sel(11..4) = 00000001 (binary) and reg_write(n) is true.
And the bus addr lines will be driven from algorithm_register_read_sel(3..0) when algorithm_register_read_sel(11..4) = 00000001 (binary) and reg_read(n) is true.

NB- the 2 shaping parameters changes only take effect when MWD Control Word (r/w register address 0x0) bit 0, Disable MWD is toggled 0-1-0.

5. Other per-channel parameters- register addresses 0x20-0x2F

CFD Threshold register (r/w register address 0x20)
CFD register default value is 0x0078 (120 dec)

Veto control for each channel (r/w register address 0x21)
D0 = Apply Veto 1
D1 = Apply Veto 2
D2 = Apply Veto 3
D3 = Apply Veto 4
D4 = Apply Veto 5
D5 = Apply Veto 6
D6 = Apply Veto 7
D7 = Apply Veto 8
D8-D15 not allocated.
(Where more than 1 Veto is applied the bits are OR'ed together).

ADC Header register r/w (register address 0x22)

ADC Header values (defaults embedded in VHDL)

Channel	Header	Decimal value
0	0EAD	3757
1	1EAD	7853
2	2EAD	11949
3	3EAD	16045
4	4EAD	20141
5	5EAD	24237
6	6EAD	28333
7	7EAD	32429
8	8EAD	36525
9	9EAD	40621
10	AEAD	44717
11	BEAD	48813
12	CEAD	52909
13	DEAD	57005
14	EEAD	61101
15	FEAD	65197

TS control Header register r/w (register address 0x23)

TS Control Header values (defaults embedded in VHDL)

Channel	Header	Decimal value
0 (sync)	0DAC	3500
1 (pause)	1 DAC	7596
2 (resume)	2 DAC	11692

TFA decay_time register 0x24 (r/w register, 16 bits wide)
Per channel parameter
Low 16 bits of the decay time correction parameter calculated as follows (top 16 bits set to 0):
2**24 x (1-(exp(-CST/50000))/(CST/10) where CST is TFA (CMWD) shaping time in ns

- CST = register 0x25 parameter
- 50,000 = decay time in ns (not us) same decay time as 0x17,18 in MWD parameters.
- 10 is clock step in ns (assumes 100MHz clock).

For example for CST = 80ns:and decay time constant of 50us:
*decay time parameter = 2**24 *(1-exp(-80/50000))/(80/10) = 3353 = 0D18 hex*
Default assumes CST = 120ns, decay 50us = 3351 (0D16 hex)

TFA shape_time register 0x25 (r/w register, 16 bits wide)
Per channel parameter
Low 8 bits used to define TFA (CMWD) shaping time parameter. Decimation factor = 1, clock = 10ns. So CMWD_shape_time value = 256- (CST(ns)/10)
for example for CST = 80ns: 256-80/10 = 248 (0xF8)
Default assumes CST = 120ns so value = 244 (0xF4)
NB- the shaping parameter changes only take effect when MWD Control Word (r/w register address 0x0) bit 0, Disable MWD is toggled 0-1-0.

Hit pattern Trigger mask register 0x26 (r/w register, 16 bits wide)
Per channel parameter
D0 = Use Channel 1 Trigger when = 1
D1 = Use Channel 2 Trigger when = 1
D2 = Use Channel 3 Trigger when = 1
D3 = Use Channel 4 Trigger when = 1
D4 = Use Channel 5 Trigger when = 1
D5 = Use Channel 6 Trigger when = 1
D6 = Use Channel 7 Trigger when = 1
D7 = Use Channel 8 Trigger when = 1
D8 = Use Channel 9 Trigger when = 1
D9 = Use Channel 10 Trigger when = 1
D10 = Use Channel 11 Trigger when = 1
D11 = Use Channel 12 Trigger when = 1
D12 = Use Channel 13 Trigger when = 1
D13 = Use Channel 14 Trigger when = 1
D14 = Use Channel 15 Trigger when = 1
D15 = Use Channel 16 Trigger when = 1
(Where more than 1 trigger is applied the bits are OR'ed together).

0x27-0x2F are not yet allocated

Readout parameters (per card)- register addresses 0x30-0x3F

Trace length register (r/w register address 0x30)
Trace length register maximum is 1024 (10 bits) (default 0x100)

Pretrigger position register (r/w register address 0x31)

Pretrigger position register maximum is 2048 (11 bits) (default 0x010)

RTDEX Read status register (ro register address 0x32)
Used for all RTDEX reads (channel address ignored)
D0 = data available (when = 1) (trigger received)
D1= FIFO_available (live status- not latched)
D2 = waiting for rtdex (in loop) (Latched)
D3 = rtdex_start_req (live)

D4 = 1 if dword_cnt_sig = x"00000400" (live status- not latched)
D5 = read_req_FIFO read out was zero.
D6 = txenable (live status- not latched)
D7 = rtdex_available (live status- not latched)

D8 = FIFO_event_count_vec(0) (live)
D9 = 0
D10 = ext_trigger received (latched)
D11 = rtdexready1sig (live status)

D12 = FIFO prog_full
D13 = FIFO prog_empty
D14 = FIFO_full
D15 = FIFO_empty

D0-D15 are cleared by control register (0x38) bit D0 going to 1 and enabled when it is 0.

rd_req_fifo live status (read only) (ro register address 0x33)
this is the output of the request fifo (live) (channel address ignored).

FIFO Write count register (read only) (ro register address 0x34)
Used for all RTDEX traces (channel address ignored). Status report only.

FIFO event counter register (read only) (ro register address 0x35
(event = 512 words) Used for all readout traces (channel address ignored).
Status report only.

Ro_enable (status of sequencer) (read only) (ro register address 0x36)
Used for all channels- bit field says which channel is enable for readout (channel address ignored).

Chan_sel_ro (status of sequencer) (ro register address 0x37)
Used for all channels- 0-15: says which channel sequencer is reading (channel address ignored).

Read_req (current value from mux) (ro register address 0x38)
Used for all channels- pattern of read requests from active channels (channel address ignored).

RTDEX Control register (r/w register address 0x39)

D0 = 1 resets the "data available" bit in RTDEX Read status register (at 0x32 hex)
D0 = 0 allows "data available" to be used again.

D1 = 0 permit hardware reset/rearm of the trigger as soon as it is received
D1 = 1 block hardware reset/rearm of trigger- only runs with software re-arm

D2 = 0 to stop (global disable, set to 0 by MIDAS stop)
D2 = 1 to go (global enable, set to 1 by MIDAS Go)

D3 unused

D4 =1 resets the RTDEX FIFO while set to 1 (direct from register, not from sequencer)
D4 = 0 Idle state- doesn't reset the RTDEX FIFO.

D5=0 Time Stamp runs normally
D5=1 Clear Timestamp

D6= 0 Use front panel trigger input as external trigger
D6= 1 Use front panel trigger as timestamp synch pulse

D7 = 0 allows- RTDEX_available to be controlled by sequencer (status_rst)
D7 = 1 force RTDEX_Available always on

~~D8 = 0 allows- FIFO_available to be controlled by sequencer (status_rst)~~
~~D8 = 1 force FIFO_Available always on~~ deleted rel 4.1.9; now unused

D9 = 0 normal state- allows buffer FIFO to operate normally.
D9 = 1 is FIFO reset (resets buffer FIFO prior to RTDEX- *don't reset if data available*).

D10 = 0 ext trigger uses adac_trig
D10 = 1 ext trigger uses the direct external trigger pulse

D11 = 0 normal
D11 = 1 force reset of adac_trigger while set to 1

D12 = 0 livetime/deadtime counters running
D12 = 1 latch livetime/deadtime counters

D13 = 0 normal operation- (use ext trigger always as either trigger or synch according to D6)
D13 = 1 Use 1st ext trigger or sync after global enable to load timestamp counters from 0x3A-3C
(This bit over-rides the settings of D6 in this register(ext trigger/synch selection) and of MWD control word bit 12, reg offset 0, (internal/external trigger selection).)

D14 = 0 If D13 = 1 then add a 5ms delay onto global enable before looking for trigger to load TS
D14 = 1 Disable 5ms delay and (if D13 = 1) look for trigger straight after global enable to load TS

D15 = 0 for normal diagnostic lines; = 1 for chan_sel_ro(4:0) & mwd_active_sig (4.1.8 onwards)
(up to 4.1.7 it was CSP state when 0, RCB state when 1)

Timestamp Low Preload Value (default 0x001A) (rw register address 0x3A)
Used for all channels- low word of timestamp (15..0)- loaded every synch or at resynch

Timestamp Mid Preload Value (default 0x0000) (rw register address 0x3B)
Used for all channels- middle word of timestamp (31..16)- loaded at resynch only

Timestamp High Preload Value (default 0x0000) (rw register address 0x3C)
Used for all channels- top word of timestamp (48..32)- loaded at resynch only

Timestamp logic latency correction (default 2) (r/w register, 4 bits wide, address 0x3D)
Used for all channels- added to TS Low Preload value to correct for sequencer pipelining in steps of 1 clock from 0-15 (4 bits only).

FIFO_Status register (r/o register 16 bits wide, address 0x3E)

D0-D6 = req_rtdex_count
D7-11 not used
D12 = FIFO prog_full
D13 = FIFO prog_empty
D14 = FIFO_full
D15 = FIFO_empty

0x3F not yet defined (use PSA moved to 0x90)

6. Diagnostics - register addresses 0x40-0x4F

Registers 0x40-0x4F re- allocated (Header moved to 0x22)

0x40 (read only) Next Cycle counter
0x41 (read only) ext trig rst req counter
0x42 (read only) rf_rd_en counter
0x43 (read only) rf_wr_en counter
0x44 (read only) valid_rd_req counter
0x45 (read only) rf_valid counter
0x46 (read only) Status bits for readout sequencers (live)

0	Readout active
1	Ro seq busy
2	reading
3	Ext trig rst req
4	Next cycle
5	Chan sel ro5(0)
6	Chan sel ro5(1)
7	Chan sel ro5(2)
8	Chan sel ro5(3)
9	Chan sel ro5(4)
10	Valid read req
11	mwd_active_sig
12	rf_empty
13	rf_full
14	rf_prog_empty
15	rf_prog_full

0x47 (read only) Status bits for pause and resume (live)

0	Pause Tag
1	Resume Tag
2	Rd Req Fifo(16)
3	Pause
4-7	0
8-11	Csp sequencer stat
12-15	Rcb sequencer stat

0x48 (read only) Trace Done counter
0x49 (read only) Mwd Finished counter
0x4A (read only) Readout Active counter
0x4B (read only) Readout Seq Busy counter
0x4C (read only) Clock_TS_Active counter
0x4D (read only) Resume Request counter
0x4E (read only) Pause Request counter

7. Livetime registers 0x50 to 0x5f *(from rel 1.c onwards)*

0x50 rtdx_LT_count(15:0) (r/o)
0x51 rtdx_LT_count(31:16) (r/o)

0x52 rtdx_DT_count(15:0) (r/o)
0x53 rtdx_DT_count(31:16) (r/o)
0x54 fifo_LT_count(15:0) (r/o)
0x55 fifo_LT_count(31:16) (r/o)
0x56 fifo_DT_count(15:0) (r/o)
0x57 fifo_DT_count(31:16) (r/o)
~~0x58 test register (r/w)~~

8. Diagnostics register addresses 0x60-0x6F

0x60 (read only) clockts(0) counter
0x61 (read only) clockts(1) counter
0x62 (read only) clockts(2) counter
0x63 (read only) clockts(3) counter
0x64 (read only) clockts(16) counter (synch)
0x65 (read only) last length count (write to pre-rtdex fifo)
0x66 (read only) length count status
D15:12 = error count
D11:3 = low 9 bits of length count
D2 = length < tracelength
D1 = length > tracelength
D0 = length = tracelength (normally =1)
0x67 (read only) local_rd_req_fifo(15 downto 0)
0x68 (read only) local_rd_req_fifo(18 downto 16)
0x69 (read only) length_count_err
0x6a (read only) chan_sel_error (should be 0)
0x6b (read only) ~~make_rf_rd_en_count~~ (up to 4.1.12) count wd_reset on diag chan (4.1.13 on)
0x6c (read only) pause count from rf_fifo
0x6d (read only) pause count from buffer full
0x6e (read only) ~~request start of write to rtdex when pre-rtdex buffer is 0 (4.1.8 on)~~
0x6f (read only) ~~sync_queue_pause count~~
0x6e (read only) rcb error count (sequencer undefined) (4.1.9 onwards)
0x6f (read only) csp error count (sequencer undefined) (4.1.9 onwards)

9. TDRI and Veto control registers (common) 0x70-0x7F

TDRI Control register 0x70 (r/w register, 16 bits wide)
~~D0 = DAC output signals enable (0 = off, 1 = enabled)~~ (no longer used)
D1 = DAC Channel select bit 0
D2 = DAC Channel select bit 1
D3 = DAC Channel select bit 2
D4 = DAC Channel select bit 3
D5 = Force resynch to TS=0x00000000001A (0-1 edge) *added June 2014*
D6-15 not yet allocated

D1-D4 select one of the 16 channels (0000 = ch1, 1111 = ch16, D4=1, D3,2,1,=0 selects ch 9 etc)

Signals displayed on the DAC are not controlled here- they are controlled via MWD Control word (offset 0x00) the test sel bits and gain bits.

Veto Coincidence Window Register 0x71 (r/w register, 16 bits wide)
D0-D13 Number of 10ns steps used for Veto Coincidence window (either counts from Veto and looks for trigger or counts from trigger and looks for Veto depending which comes first).
Minimum = 10ns, so e.g. 0x10 = 170ns or 0x80 = 128x 10 ns +10ns = 1.29us window.
Default value is 0x80
D14 = disable Early Veto Window (1=disable; 0 = normal operation)
D15 = disable Veto Window (1=disable; 0 = normal operation)

GPIO Control register 0x72 (r/w register, 16 bits wide)
D0 = TDRI Loop back (0 = diagnostic signals out of TDRI, 1 = loop back out of TDRI)
D1 = Diagnostic Signals Channel select bit 0
D2 = Diagnostic Signals Channel select bit 1
D3 = Diagnostic Signals Channel select bit 2
D4 = Diagnostic Signals Channel select bit 3
D5-15 not yet allocated

D0 controls whether TDRI is in loop-back mode to test internal connections or sending out the ADC's diagnostic signals on TDRI ECLoutputs
D1-D4 select one of the 16 channels (0000 = ch1, 1111 = ch16, D4=1, D3,2,1,=0 selects ch 9 etc)
Signals output are: Channel Busy, CFD, Veto, veto window, early veto window and peak sample on the gpio spare lines which the TDRI sends out on the ECL outputs.

veto_delay_0 0x73 (r/w register, 16 bits wide)
D0-D6 veto delay in 10ns steps from 0 to 1270ns (D6 is MSB, D0 is LSB)
D7 enable Veto 0 when =1 (disabled when 0)
D8-15 unused.

veto_delay_1 0x74 (r/w register, 16 bits wide)
D0-D6 veto delay in 10ns steps from 0 to 1270ns (D6 is MSB, D0 is LSB)
D7 enable Veto 1 when =1 (disabled when 0)
D8-15 unused.

veto_delay_2 0x75 (r/w register, 16 bits wide)
D0-D6 veto delay in 10ns steps from 0 to 1270ns (D6 is MSB, D0 is LSB)
D7 enable Veto 2 when =1 (disabled when 0)
D8-15 unused.

veto_delay_3 0x76 (r/w register, 16 bits wide)
D0-D6 veto delay in 10ns steps from 0 to 1270ns (D6 is MSB, D0 is LSB)
D7 enable Veto 3 when =1 (disabled when 0)
D8-15 unused.

veto_delay_4 0x77 (r/w register, 16 bits wide)
D0-D6 veto delay in 10ns steps from 0 to 1270ns (D6 is MSB, D0 is LSB)

D7 enable Veto 4 when =1 (disabled when 0)
D8-15 unused.

veto_delay_5 0x78 (r/w register, 16 bits wide)
D0-D6 veto delay in 10ns steps from 0 to 1270ns (D6 is MSB, D0 is LSB)
D7 enable Veto 5 when =1 (disabled when 0)
D8-15 unused.

veto_delay_6 0x79 (r/w register, 16 bits wide)
D0-D6 veto delay in 10ns steps from 0 to 1270ns (D6 is MSB, D0 is LSB)
D7 enable Veto 6 when =1 (disabled when 0)
D8-15 unused.

veto_delay_7 0x7A (r/w register, 16 bits wide)
D0-D6 veto delay in 10ns steps from 0 to 1270ns (D6 is MSB, D0 is LSB)
D7 enable Veto 7 when =1 (disabled when 0)
D8-15 unused.

10.Code version data (per card)- register addresses 0x80-0x8F

All code version registers are read only

Code Major Release Version number (major changes) register (ro register address 0x80)
Hex values 0x0000 to 0xFFFF are valid

Code Incremental Release number (update for every change) (ro register address 0x81)
Hex values 0x0000 to 0xFFFF are valid

Number of channels supported in this version (ro register address 0x82)
Decimal value from 1-16 (hex value 0x0001 to 0x0010)

Date of this version (ro register address 0x83)
Hex version of date (day/day/month/year) so 21st July 2009 is coded as 1579

11. PSA Control (per card)- register addresses 0x90-0x9F

Use PSA (r/w register 16 bits wide 0x90)

D0 =1 means replace MWD with PSA in channel 1 = 0 means use MWD (no PSA)
D1 refers to channel 2 etc (D15 refers to ch 16)

PSA Int 1 start delay 0x91 (r/w register, 9 bits wide)
Sets delay in 10ns clocks after trigger before start of integration int 1
Max permissible value is 511 (5.1us) (bits 9-16 ignored) default is 0

PSA Int 1 Int period (0x92) (r/w register, 9 bits wide)
Sets integration period in 10ns clocks after Int 1 delay default is 1.2us (total int)

Max permissible value is 511 (5.1us) (bits 9-16 ignored)

PSA Int 2 start delay 0x93 (r/w register, 9 bits wide)
Sets delay in 10ns clocks after trigger before start of integration int 2
Max permissible value is 511 (5.1us) (bits 9-16 ignored) default is 0

PSA Int 2 Int period (0x94) (r/w register, 9 bits wide)
Sets integration period in 10ns clocks after Int 2 delay
Max permissible value is 511 (5.1us) (bits 9-16 ignored) default is 100ns (fast int)

PSA Ave period start delay 0x95 (r/w register, 10 bits wide)
Sets delay in 10ns clocks after trigger before start of baseline averaging
Max permissible value is 1023 (10.2us) (bits 10-16 ignored) default is 4.8us

PSA Ave period width (as power of 2) (0x96) (r/w register, 3 bits wide)
Low 3 bits sets averaging period as power of 2 (000=1, no averaging (sample 1 clock only) 001 = 2 clocks (20ns), 010 = 4 clocks (40ns), 011 = 8 clocks (80ns), 100 = 16 clocks (160ns), 101 = 32 clocks (320ns), 110 = 64 clocks (640ns) 111 = 128 clocks (1.28us)) Bits 4-15 are ignored. Default is 320ns

PSA Control (0x97) r/w register 16 bits wide
Bit 0 = 1 divides integral by 64 to ensure it fits in the 16 bit output (13 bit data, max integration 512 so divide by 256 needed to avoid overflow). (if bit 0 = 0 there is no division so use small signals or short integration and check overflow flags).
Bit 1 = 1 disables subtraction of average (bit 1 = 0 subtracts the calculated average)
Bits 2-15 not yet allocated

12.Data format for Lyrtech readout

D31 to D16	**D15 to D0**
TS_low (15:0)	Header
TS_High (47:32)	TS_Mid (31:16)
Trace word 2	Trace word 1
Trace word 4	Trace word 3
etc	etc
Trace word (tracelength-8)	Trace word (tracelength-7)
Baseline (or int2 (fast) in PSA mode)	Energy (or int1 (total) in PSA mode)
TS_Mid (31:16)	Flags (d0=Veto; d1=pileup, d2=adc ovr; d3= algorithm ovf OR dig gain ovf OR PSA ovf, d4=dig gain ovf d5= PSA d6 = ps ovf d7-d15 unused=0)