

Moving window deconvolution module

Introduction:

The moving window deconvolution (MWD) module despite implementing simple calculations has relatively high complexity due to the use of fixed point arithmetic and need for time synchronisation. This document explains the calculation flow, number formats and delays through the MWD hardware.

Brief notes on Q format:

Q format is used to denote numbers with a 'virtual' binary point in fixed point arithmetic systems. E.G the value "0101" in a conventional binary representation would be decimal 5, if this were in Q2.2 format this would be 1.25. From the left the value of each binary place is $2^1, 2^0, 2^{-1}, 2^{-2}$. By keeping track of the Q format we are using for values in our digital signals processing, padding and selecting appropriate bits we can use binary multipliers to perform division. Rounding (floor) can be performed by truncating fraction bits. When numbers are represented as signed twos complement I have elected to explicitly denote they are signed and count the sign bit as a Q value. For example direct conversion of an unsigned Q16 value without additional positive range would be to a Q17 (signed) value as the first bit is used by the sign bit.

Notes on custom float16 format used to export waveforms:

The FEBEX waveform memory is only 16 bits wide, therefore unless multiple data words are used there must be some loss of precision to store numbers greater than $2^{16}-1$. The 'T' waveform that is viewed to adjust the moving window deconvolution parameters is internally a 34 bit signed number therefore a custom 16 bit floating point format has been designed to store it in the waveform memory. This format has the following specification (from MSB to LSB):

- 1 sign bit ('1' indicates negative number, '0' positive)
- 5 bit power of 2 exponent with no pre-bias (fractional numbers cannot be represented)
- 1 bit significand (implicit 1 allows extra bit)
- 34 bit input word is truncated to remove 3 least significant bits

Example conversions:

1000 => 0x63D0

-1000 => 0xE3D0

0 => 0x0000

VHDL code (simulation) to convert custom floating point back to 34bit signed:

```

221 : --Convert output float to real number again
222 ⊖ Pregen : PROCESS(export_T)
223   variable sign_bit : std_logic;
224   variable signif : unsigned(9 DOWNT0 0);
225   variable exp : unsigned(4 DOWNT0 0);
226   variable bit_store : std_logic_vector(34 DOWNT0 0);
227   variable bit_store2 : std_logic_vector(34 DOWNT0 0);
228   BEGIN
229     sign_bit := export_T(15);
230     exp := unsigned(export_T(14 DOWNT0 10));
231     signif := unsigned(export_T(9 DOWNT0 0));
232     bit_store(34) := '0'; --we will encode sign later
233     bit_store(33) := '1';
234 ⊖   if ((signif = to_unsigned(0,signif'length)) and (exp = to_unsigned(0,exp'length))) then
235     bit_store(33) := '0'; --special zero case
236   end if;
237   bit_store(32 DOWNT0 23) := export_T(9 DOWNT0 0); --fraction
238   bit_store(22 DOWNT0 0) := (OTHERS=>'0'); --set all remaining bits to zero
239 ⊖   if (sign_bit = '1') then
240     --need to take into account sign (invert all bits and add 1 to find complment)
241     bit_store2 := std_logic_vector(shift_right(unsigned(bit_store),to_integer(exp))); --shifts done by exponent
242     regen <= std_logic_vector(unsigned(not(bit_store2))+to_unsigned(1,bit_store2'length));
243   else
244     --twos complement of unsigned is the same as signed
245     regen <= std_logic_vector(shift_right(unsigned(bit_store),to_integer(exp))); --shifts done by exponent
246 ⊖   end if;
247 ⊖ END PROCESS Pregen;

```

Illustration 1: VHDL code to convert custom 16 bit floating point format to signed number

the input 16 bit word is export_T. Firstly all the bit fields are read. Secondly the special zero case is handled, this is detected by a zero exponent and a zero significand. The exponent then applies a bit shift to the the significand which has its bits flipped and 1 added if its negative. A special value that no number will encode can be encoded with -0 (0x8000).

The maximum and minimum value that can be encoded is $\pm 2^{31} * 1.999023437 = 4292870144$. The maximum value of a 32bit signed number (truncated 35 bit) is 2147483647 and minimum -2147483648 so there is a large range of values that will never be used by the waveform available for special signal encoding (E.G triggers, sample points).

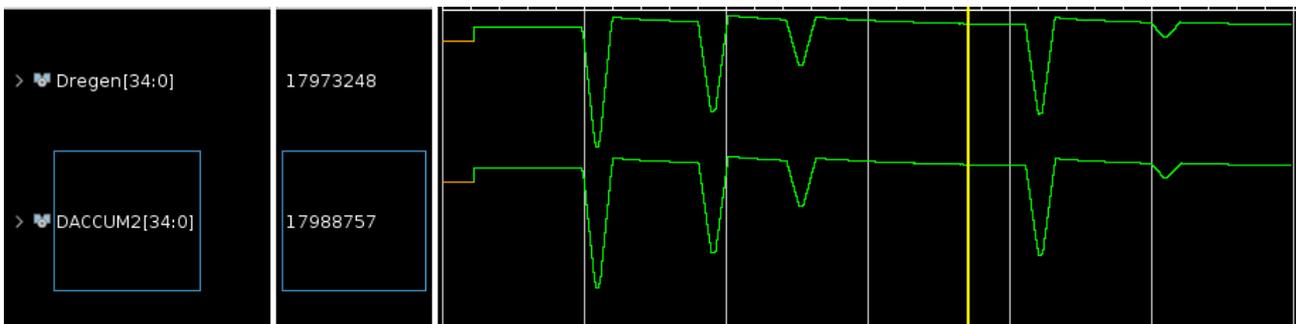


Illustration 2: Comparison of regenerated from 16 bit float waveform (Dregen) and original 35 bit signed number

Data format and delivery:

The results of the moving window deconvolution are placed in the 'dummy' trace buffer. When this trace buffer reaches a user set threshold [details] or once a time-out time threshold is reached [details] a trigger event is generated. This mode of trigger is activated by [details] and replaces the normal triggering mode whereby CFDs or global triggers cause acquisition of trace data. The MWD units for each channel are addressed in the 'round robin' fashion whereby each unit is checked in turn and serviced if a result is ready. This constrains the maximum time to service a MWD module. If a result is ready its recorded in the trace buffer. The trace buffer uses circular

address pointers and so when results are read out space again becomes available. If readout does not occur before buffer full the MWD modules become blocked and will miss events. The data is stored in the trace buffer (8192 16 bit words long) in the following format:

| Word | Format (16 bit words) |
|------|-------------------------------------|
| W0 | [channel] "0000" Timestamp[D0.. D7] |
| W1 | Timestamp [D8.. D23] |
| W2 | Timestamp [D24.. 39] |
| W3 | Timestamp [D40.. D55] |
| W4 | Energy |

Channel is stored as a 4 bit unsigned number giving the channel of the result. The time stamp is the FEBEX time stamp for the event and is given as a 56 bit unsigned number. The energy is a 16bit floating point value in the custom format defined earlier in this document.

Design:

Moving average calculation (Delay 7 clocks):

This hardware calculates a moving average of trace values (achan), implementing the MATLAB code:

$$MA(loop) = \text{sum}(\text{Waveform}((loop-M):loop-1))/\text{torr}; \% \text{Moving average}$$

where loop is the loop index incrementing over the waveform length. Note that Wavefom(loop-1) is the first sample acted on by this calculation and so there is a sample delay required relative to the derivative calculation.

Firstly the trace data is accumulated, this has a delay of one clock cycle due to the final unit delay in the accumulator been used as a pipeline register.

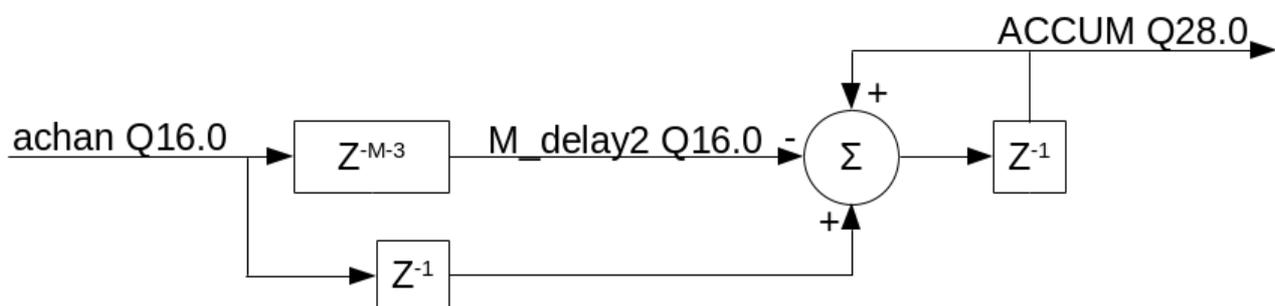


Illustration 3: Calculation of sample accumulator

next the division by torr is accomplished using a multiplier which has a delay of 6 clock cycles. By padding achan and torr with differing numbers of zeros leading zeros pre-devision by 4096 is accomplished on ACCUM and torr represents only the fractional part of the Q16.16 input words to the divider.

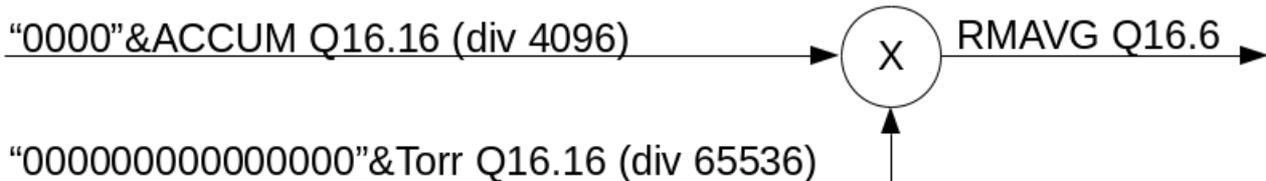


Illustration 4: Calculation of moving average

The value torr is the preamp time constant in clock cycles to divide by. FEBEX uses a 100MHz sample clock. For example if the preamp had a time constant of 200µS this would be a divide by 20,000 clock cycles, we have an existing pre-divider of 4096 so we actually need to divide by 4.883 clock cycles. This is equivalent to multiplication by 0.2048, in Q16.16 format this is 0000000000000000.0011010001101110 (torr_calcs.ods shows how to perform these calculations).

Numerical differentiation calculation (Delay 7 clocks):

This hardware calculates a numerical derivative implementing the MATLAB code:

```
D(loop) = Waveform(loop)-Waveform(loop-M); %Numerical differentiation
```

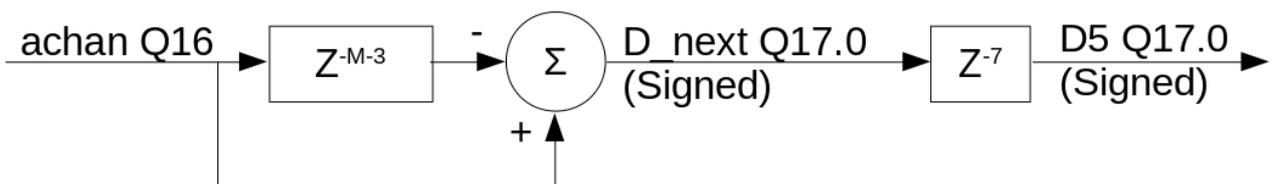


Illustration 5: Numerical derivative calculation

A 7 cycle delay is used to align the result with the RMAVG waveform for which should have synchronized results with this module for the MWD waveform calculation.

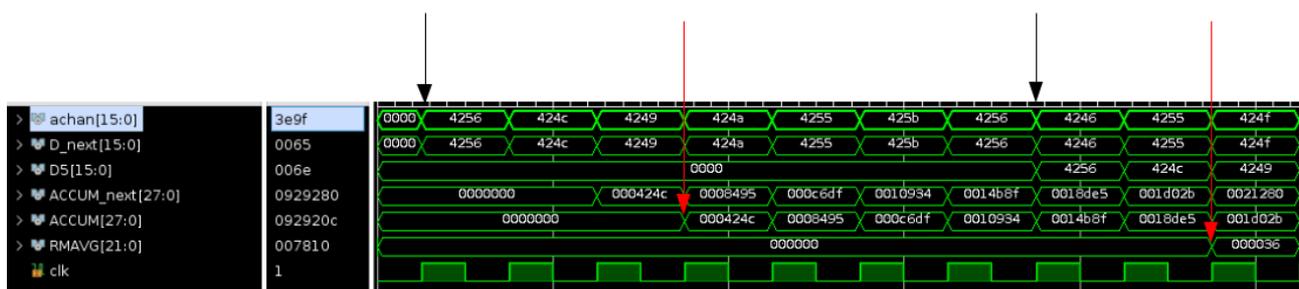


Illustration 6: Delay verification at startup for differentiation calculation alignment (D5) with moving average (RMAVG). Black lines show time to first data (7 clocks) for derivative and red for MAVG (6 clocks) however ACCUM has an extra cycle delay from ACCUM_next balancing the delays at 7 clocks. The startup of ACCUM is delayed W.R.T RMAVG to avoid corrupt data entering the accumulator where it cannot be cleared (mainly simulation issue).

MWD waveform calculation (1 clock delay):

This hardware calculates:

```
MWD(loop) = D(loop)+MA(loop);
```

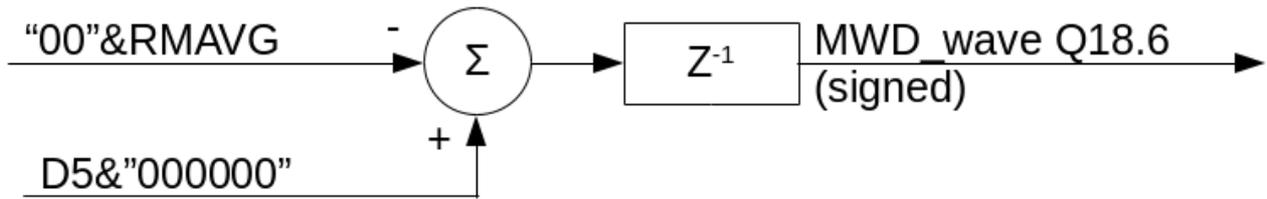


Illustration 7: MWD waveform calculation

The delay to this point is now 8 clock cycles relative to the input waveform (achan).

Calculation of 'T' wave (1 clock delay)

This calculates:

$$T(\text{loop}) = \text{sum}(\text{MWD}(\text{loop-L}:\text{loop-1}))/L; \% \text{Moving average}$$

however the final division by L has been omitted as this is a common factor in the energy calculation and so only acts as a scaling factor on the final energy value that can be removed in software.

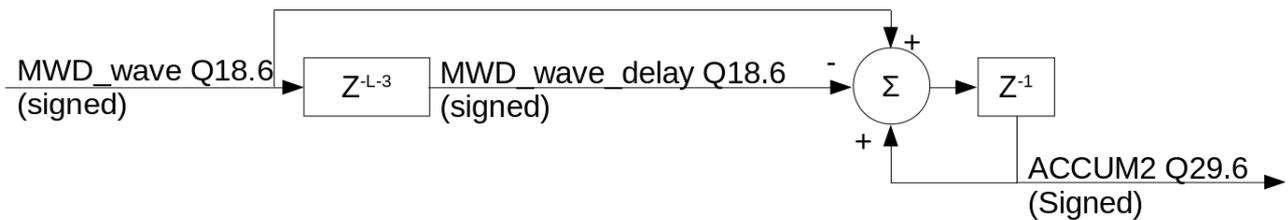


Illustration 8: 'T' wave calculation

ACCUM2 is sampled to determine the energy along with the baseline. This waveform displayed by the end user as a trace to adjust the MWD parameters, in this process triggers are (optionally) overlaid on the 'T' waveform. This waveform is 9 clock cycles behind the trigger signal and so a delay is required.

Visualisation processing of T waveform (2 clock delay):

To adjust the moving window deconvolution parameters it is required to display the 'T' waveform with triggers and energy sampling points overlay. A barrier to this is that the waveform is Q29.6 (signed) requiring 35 bits to display it, however the FEBEX only has 16 bit trace memory buffers. A solution to this problem is to use a custom 16 bit floating point format which has been defined in 'Notes on custom float16 format used to export waveforms:'. Generating this floating point number takes 2 clock cycles using the module 'S35_to_float16'.

The module 'S35_to_float16' performs all possible bit shifts to generate the significand in parallel and then selects the smallest bit shift that results in the implicit '1' of the significand been set. This would only take a single clock cycle but a pipe line register has been used on the output of the significand selector to increase timing flexibility.

For visualisation the output of this module can be overwritten by setting a register [details]. When this register is set a trigger causes the special floating point values outside of the used range:

- Trigger special value: 0xEFFF
- Energy sample point special value: 0xFFFF

A 11 clock cycle delay line is used to delay the trigger signal for visualisation and a 2 cycle delay line for the energy sampling such that the sample they overwrite on the waveform is the sample they are acting upon. There is no waveform value available when a special value is used and so its recommended that the previous waveform value is displayed.



Illustration 9: Regenerated to signed number floating point waveform with extraction of trigger and energy sampling points. Also using previous value hold technique to disguise missing samples.

Calculation of baseline (no clock delay):

The baseline must be subtracted from the peak values to determine the energy. The baseline is calculated by blanking ACCUM2 during events; during blanking the pre-blanking value of ACCUM2 is retained until the blanking period is completed. The blanking period is $M+L+6+\text{extra_blank}$ where `extra_blank` is a user set value 0 to 4095 clock cycles long (upto $40.95\mu\text{S}$) that can be used to extend blanking to eliminate tail effects. The +6 is to take into account that the M and L values have +3 added to them by the operation of the delay lines in earlier calculations.

To ensure that the blanking is aligned with the ACCUM2 waveform the blanking is started by a 9 clock delayed trigger signal.

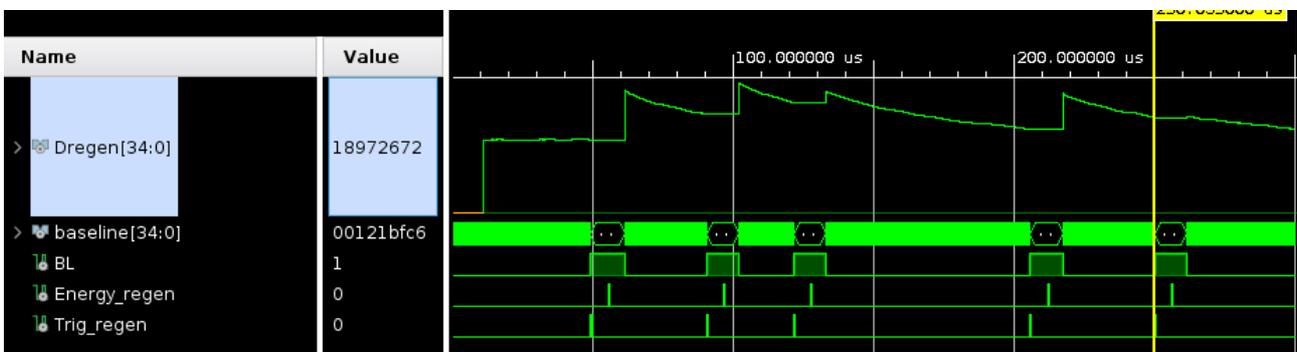


Illustration 10: Baseline waveform selected as trace showing blanking (when BL='1')

Operation:

Addressing:

Only one register is used to communicate with the trigger peripheral with the GOSIP address [address]. The writes to this register are 32 bits with the most significant byte used to distinguish which sub register the write is for and the nibble below this used to select the channel. The least significant bits are used for the data payload.

If settings are needed to be read back the same address is written to but with the most significant bit set (E.G M becomes 1000 0001). To read a write should be undertaken and then a subsequent read of the register [address] will have the correct data payload. (similar to how the SPI read/write is performed (see memory map)).

The channel is selected using the 3rd most significant nibble. Channels are numbered 0 through to 15 (16 total).

| Parameter | Data word (32bit, x= don't care) | Format |
|-----------------|---|--------------------------|
| M | 0000 0001 [chan] xxxx xxxx [data] [data] [data] | 12 bit unsigned |
| L | 0000 0010 [chan] xxxx xxxx [data] [data] [data] | 12 bit unsigned |
| Torr | 0000 0011 [chan] xxxx [data] [data] [data] [data] | 16 bit unsigned |
| Extra blank | 0000 0100 [chan] xxxx xxxx [data] [data] [data] | 12 bit unsigned |
| Options | 0000 0101 [chan] xxxx xxxx xxxx [data] [data] | 8 bit logic and unsigned |
| cfid_trig_delay | 0000 0110 [chan] xxxx xxxx [data] [data] [data] | 12 bit unsigned |

Write example:

In this example the M value is set to 500 on channel 15, this involves a data payload of 497 as M values have 3 added to them internally.

```
goc -w -x 1 0 [address] 0x01F001F1
```

Read example:

In this example the cfd_trig_delay is read from channel 1

```
goc -w -x 1 0 [address] 0x86100000
```

```
goc -r -x 1 0 [address]
```

```
0x00000111
```

Detailed description of input parameters:

M:

length of step signal from exponential tail (samples), note actual value in module is +3 on input value. I.E input of 0 results in 3. This is due to the delay line logic. Measured in clock cycles at

100MHz, I.E input value of 497 results in M value of 500 which is 5 μ S. This value is unsigned and the maximum is 4095 (4098 effective).

L:

Length of moving average (L < M to get trapizoid) (samples), note actual value in module is +3 on input value. I.E input of 0 results in 3. This is due to the delay line logic. Measured in clock cycles at 100MHz, I.E input value of 497 results in L value of 500 which is 5 μ S. This value is unsigned and the maximum is 4095 (4098 effective).

Torr:

The value torr is the preamp time constant in clock cycles to divide by. FEBEX uses a 100MHz sample clock. For example if the preamp had a time constant of 200 μ S this would be a divide by 20,000 clock cycles, we have an existing pre-divider of 4096 so we actually need to divide by 4.883 clock cycles. This is equivalent to multiplication by 0.2048, in Q16.16 format this is 0000000000000000.0011010001101110 (torr_calcs.ods shows how to perform these calculations).

1. Calculate number of clock cycles to divide by: $\alpha = \text{round}(100e6 * \text{torr}[s])$
2. Calculate value to encode right of decimal point taking into account pre-divider: $\beta = 1/(\alpha * 4096)$
3. Calculate the decimal Torr value: $\text{Torr} = \text{round}(2^{16} * \beta)$ this is the value (in hex) that is sent to set the register on FEBEX.

Extra_blank:

This is the extra number of clock cycles to blank the baseline after a trigger. If this is set to 0 the blanking time is M+L+6 (to take into account the extra 3 added to each value). This can be used to eliminate tail effects from the baseline estimate.

Options:

This register is used to configure multiple parameters

D0 – D3: The magnification factor of the readout of the internal MWD waveform if this is selected using Read_MWD='1'. The magnification factor is in binary places and is used to increase the resolution of the visualisation of the MWD waveform at the expense of reducing the clipping point of this waveform. It is not anticipated that users will want to view this waveform.

D4: (Read_MWD) When set to '1' the trace exported from the MWD module is set to an internal 16bit signed value that contains the MWD waveform amplified by the magnification factor. This setting has priority over TorB.

D5: (mark_sp) When this option is set '1' and read_mwd='0' the exported floating point waveforms will have trigger and energy sampling points encoded onto them which allows tuning of the MWD parameters. See 'Visualisation processing of T waveform'.

D6: (TorB) '0' sets the floating point waveform export to the 'T' waveform while '1' sets it to the baseline waveform. This setting is overwritten by Read_mwd.

D7: (WaveSel) '1' makes the trace data be moving window deconvolution data (16 bit custom floating point format), '0' makes the trace data be normal ADC data.

cfid_trig_delay:

cfid_trig_delay : number of clocks after the trigger signal to sample the energy. Note in the case of pileup the 1st event causes the energy readout (subsequent events do not restart countdown) this is to avoid very high rates causing no data to be written. Using the option mark_sp and a pulsar this value can easily be tuned to the correct point on the trapezoids.