FEBEX ADCCLK peripheral

Summary:
This document describes the functionality and interface of the ADCCLK peripheral that has been implemented on the FEBEX4A. This provides the following functions:

- ADC_OUT_CLK – a 100 MHz output clock line for the ADC that can be generated using a PLL from the EXPLODER 20MHz clock to keep the FEBEX cards commonly clocked. Alternatively this can be generated from the GTX tranciver clock of the FEBEX cards (not in sync). There is automatic fallback to the GTX clock if the EXPLODER clock isn't present and status is reported.
- Time-stamp counter in the ADC_OUT_CLK domain of 56 bits length, 10nS granularity. This time-stamp can be reset from signal on input 1 of EXPLODER (RC1) in order to synchronize timestamps of all FEBEX cards.
- Selectable forwarding of EXPLODER input 1 to the SYNC input of the two ADC chips. This allows synchronization of the ADCs clock dividers (and therefore aperture) across all FEBEX cards.

Correct use of this peripheral should result in synchronized ADC samples and timestamps across all FEBEX cards.

Sync Procedure:

1. Prevent pulses to trigger input 1 of EXPLODER (RC1)
2. Write to all cards to expect sync
3. Check status bits indicate waiting for sync
4. Supply sync pulse (300nS - 10uS) to input 1 of EXPLODER (NIM) this is directly passed to the ADCs
5. Check status bits indicate sync is 'done' for all cards

Status bits:

Status bit	**Description**
Status(0)	'0' = EXPLODER clock in use, '1' = GTX clock in use
Status(1)	'0' = EXPLODER clock requested, '1' = GTX clock requested
Status(2)	'1' = Waiting for RC1 sync pulse, goes low once sync received
Status(3)	'1' = Sync pulse sent, stays high until next write to card to expect sync

Fall-back to GTX clock is indicated by status(1 DOWNTO 0) = "01". Sync status shouldn't be checked until 10uS after sync pulse is sent.

Addressing:

Only one register is used to communicate with the ADCCLK peripheral with the

GOSIP address 0x200034. The reads/writes to this register are 32 bits. Write to read is used to read status. For example to read the status word the data payload is set to the value indicated in the table and written to 0x200034, then a read of 0x200034 is initiated which will return the status bits.

Parameter	**Data word (32bit, x = don't care)**
Sync	1000 0001 xxxx xxxx xxxx xxxx xxxx xxxx
EXPLODER clock	1000 0010 xxxx xxxx xxxx xxxx xxxx xxxx
GTX clock	1000 0011 xxxx xxxx xxxx xxxx xxxx xxxx
Status	1000 0100 xxxx xxxx xxxx xxxx xxxx xxxx
Time stamp upper	1000 0101 xxxx xxxx xxxx xxxx xxxx xxxx
Time stamp lower	1000 0110 xxxx xxxx xxxx xxxx xxxx xxxx

Sync:
Writing this data word puts the card into sync mode. This can be verified by reading Status(2) = '1' . When in sync mode the card will reset the ADC timestamp and the ADC clock dividers on the next AQU trigger input to exploder (input 1 also known as RC1).

EXPLODER clock:
Writing this data word requests that the EXPLODER 20MHz clock is used to clock the ADCs (via a PLL taking it to 100 MHz). If this clock is not present this will fall back to the clock provided by the GTX transceiver. Selection can be verified by checking Status(1); Exploder clock selected = 0.

GTX clock:
writing this data word requests that the GTX 100MHz clock is used to clock the ADCs. This clock is free running with respect to other FEBEX cards. Selection can be verified by checking Status(1); GTX clock selected = 1.

Status:
Writing this data word causes the status bits to update the output word of the peripheral (see Status bits).

Time stamp upper/lower:
Writing this data word causes the output word of the peripheral to contain the right aligned time stamp upper or lower word. The time stamp is 56 bits long and unused bits are set to '0'. The time stamp will update between a write read cycle and so this should only be used for indication of the range the time stamp could be in. For example if the time stamp is read from card 0 and then card 1 we would not expect

them to be the same even if the cards are in sync.