FEBEX4A Trigger Matrix

Summary:
This document describes the functionality and interface of the Trigger Matrix module implemented on the FEBEX4A. The trigger matrix modifies which traces are read out in response to triggers that are aggregated over 1 to 65535 clock cycles (10 nS to 655.36 uS).

Features:

- 18 trigger sources (16 CFDs on ADC channels + 2 external global triggers).
- 17 trace memories which can selectively be read out in response to triggers (16 Channels + Dummy register).
- Each of the 18 trigger sources has a 17 bit long row in the 17*18 trigger matrix. Setting a bit in the trigger matrix causes the corresponding channel to be read out when the trigger source is received in the trigger window.
- Acquisition window allows aggregation of triggers up to 65535 clock cycles. This is for the circumstance that triggers arrive not at the same clock cycle. I.E an implant close to a readout wire and one further away at the same time instance but the charge transport taking longer from the further away implant. In such circumstance attempting to trigger twice is undesirable.
- Acquisition window can have internal FEBEX trigger signal that causes data capture to occur fire at start of window or at end of window. Firing the trigger at the start is useful if the window is long enough that the trace buffer would not longer contain the desired waveforms.

Diagram/Example:

		D16	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		T15	**T14**	**T13**	**T12**	**T11**	**T10**	**T9**	**T8**	**T7**	**T6**	**T5**	**T4**	**T3**	**T2**	**T1**	**T0**	**Du**
R17	**NAQU**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R16	**AQU**	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R15	**C15**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R14	**C14**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R13	**C13**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R12	**C12**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R11	**C11**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R10	**C10**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R9	**C9**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R8	**C8**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R7	**C7**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R6	**C6**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R5	**C5**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4	**C4**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R3	**C3**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R2	**C2**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R1	**C1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R0	**C0**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

R(17 DOWNTO 0) = register of row (use channel bits to access)D(16 DOWNTO 0)= data bit of row (the data bits written to the registers that control which traces are selected for readout)C(15 DOWNTO 0) = CFD from channel trace trigger sourceNAQU = global don't acquire trace trigger (RC3) (not anticipated to be used)AQU = global acquire trace trigger (RC1) (used as global trigger lineDu = Dummy memory (will be used for trace energies, timestamps ETC.)
In this example a trigger matrix has been configured to ignore NAQU and all channel triggers apart from C0 and C8 which when triggered read out just the 'dummy' memory.
If aggregation is set and multiple triggers are received during the window, at the end of the window the channels selected for readout is the OR of all channels selected by each trigger.

Addressing:
Only one register is used to communicate with the peripheral at GOSSIP address: 0x200032. The writes to this register are 32 bits with the most significant nibble used

to distinguish which sub register the write is for. The byte below this used to select the channel, the number of channels has increased to 18 with NAQ and AQU trigger sources occupying channel 17 and 16 respectively. The least significant bits are used for the data payload which varies between 18 and 1 bit in length depending on the register. Right justification is used throughout.
If settings are needed to be read back the same address is written to but with the most significant bit set (E.G Store most significant nibble becomes 1001). To read a write should be undertaken and then a subsequent read of the register 0x200032 will have the correct data payload. (similar to how the SPI read/write is performed (see memory map)). The read data does not contain the channel number only the contents of the register for that channel.
When writing to store trigger matrix row data is right justified. “0000 0000” is the dummy channel trace memory with “0000 0001” CH0 (first physical channel) trace memory, with a total of 17 trace memories. Inside the FEBEX there are a total of 34 trace memories ordered into 17 in buffer 0 and 17 in buffer 1 which are alternatively read and written to. However the application of the memflags to each buffer does not need to be considered by the software.

Parameter	**Data word (32bit, x = don’t care)**
Store trigger matrix row	0001 [chan] [chan] xx[data] [data] [data] [data] [data]
Window length*	0010 xxxx xxxx xxxx xxxx [data] [data] [data] [data]
Start(0)/End(1) trigger	0011 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxx[data]