CCLRC

# ***ASICs for FAIR***

FAIR UK Community Meeting – Daresbury Laboratory

**Marcus French**

26th January 2006

# Summary

- Who we are
- Example technologies
  - Particle physics
  - Space Science
- ASIC Goup
  - Current Nuclear Structure physics activity
  - Ideas for Nustar
    - Details for Aida
    - Other experiments – EXL and R3B
- DAQ Systems
  - Current activity and trends
- Summary

# CCLRC

*Mission:*

*...to promote and support high-quality scientific and engineering research by developing and providing facilities and technical expertise in support of basic strategic and applied research programmes...*

**Chilbolton Observatory - 10**

**Daresbury Laboratory - 500**

**Rutherford Appleton Laboratory – 1200 staff**

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# World Class Facilities

ISIS - The World's most intense pulsed source of neutrons

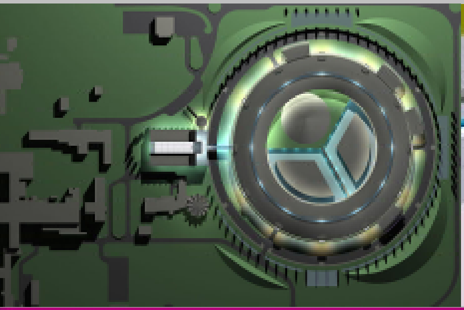
SRS - The World's first 2nd generation synchrotron source

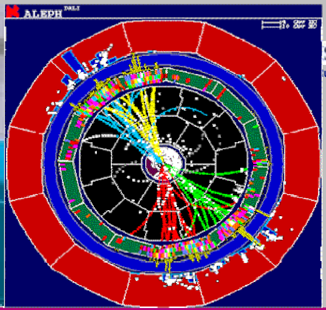
CLF - The World's highest irradiance laser

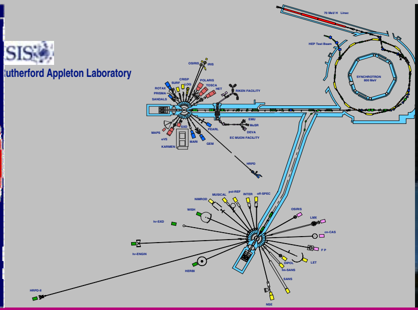
CERN LHC - The World's highest data-rate detector

Space - Largest European department with >150 orbiting instruments.

CMF – Micro-Nano facility



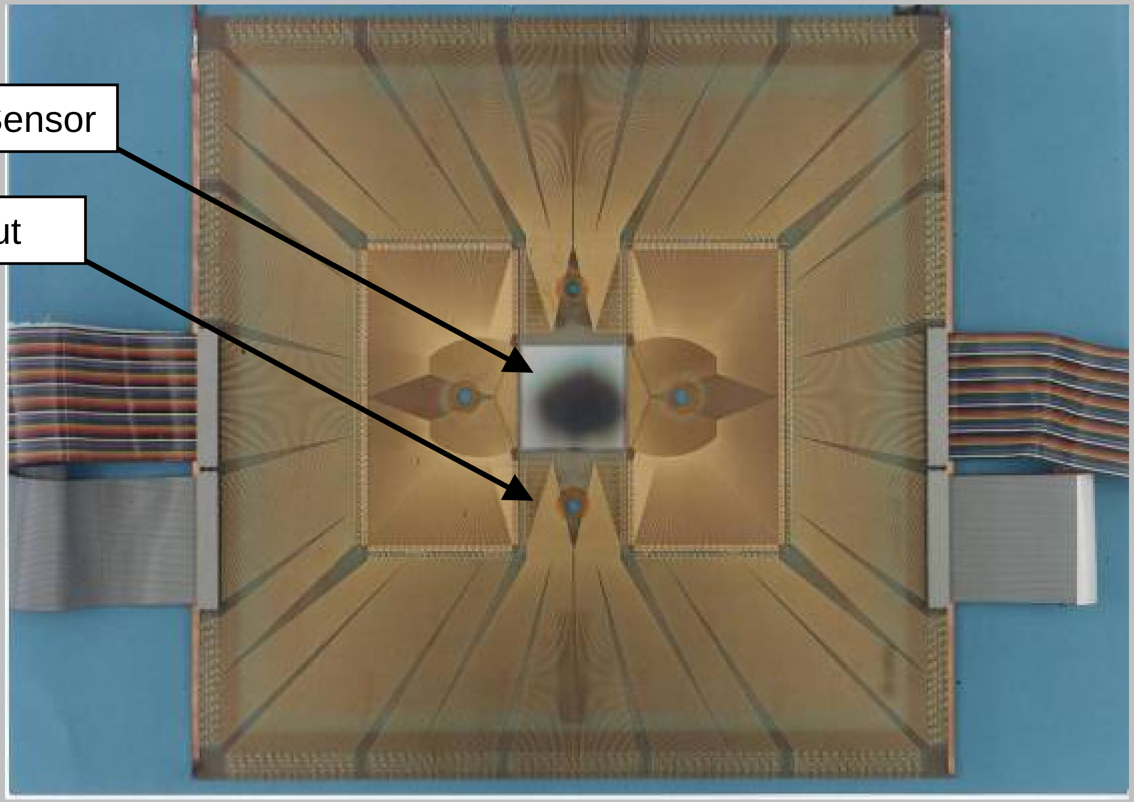





# Example Detector Technologies

- Particle Physics:
  - Sensor Instrumentation
  - Microelectronics
  - DAQ Systems
- Space Science:
  - Instrument Systems
  - CMOS Sensors
  - Data conversion
- Future Trends

# Early Microstrip Sensors

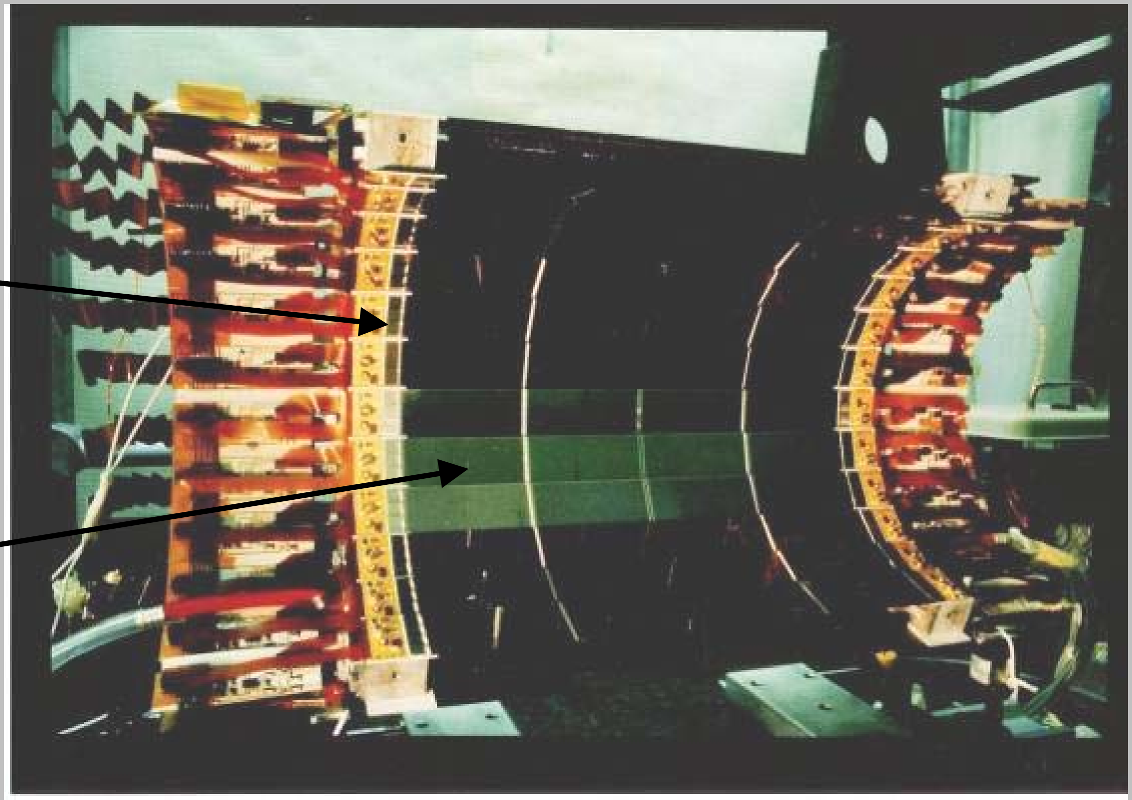



An example of a microstrip detector mounted on a PCB.

The detector, of 5cm x5cm was built for the CERN NA14 experiment and contains 1,000 strips at 50um pitch.

Ten such detectors were assembled at Imperial College to observe charmed particle physics decays.

# Delphi Micro Vertex Detector



Early Microplex ASICs

Silicon Detectors

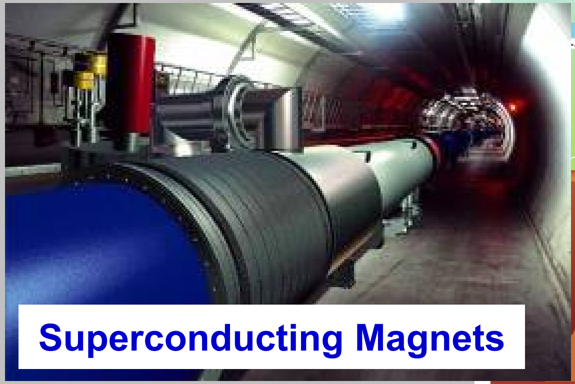
# Today's Experiment: CMS

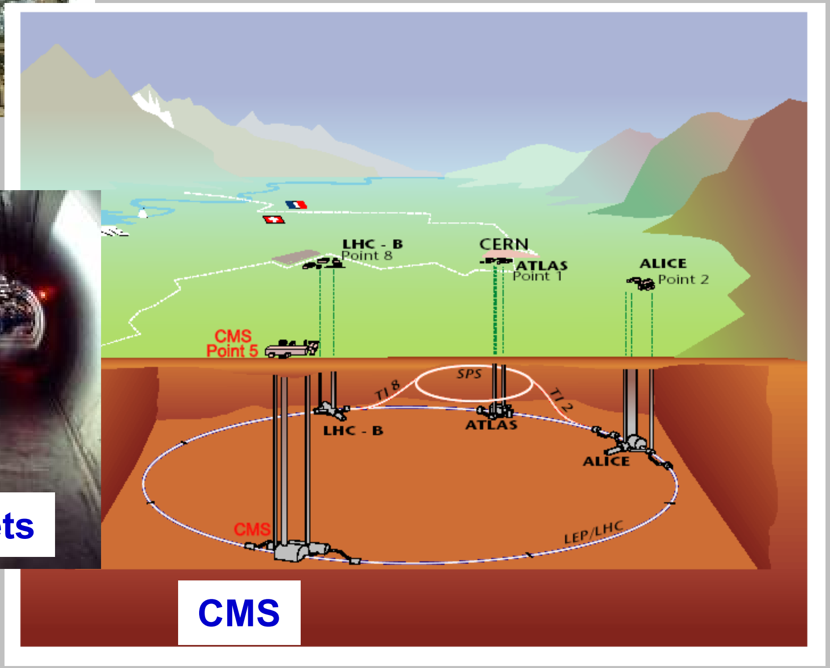
Large Hadron Collider Facility

Particle Accelerator


Tunnel 27 km

100 m underground



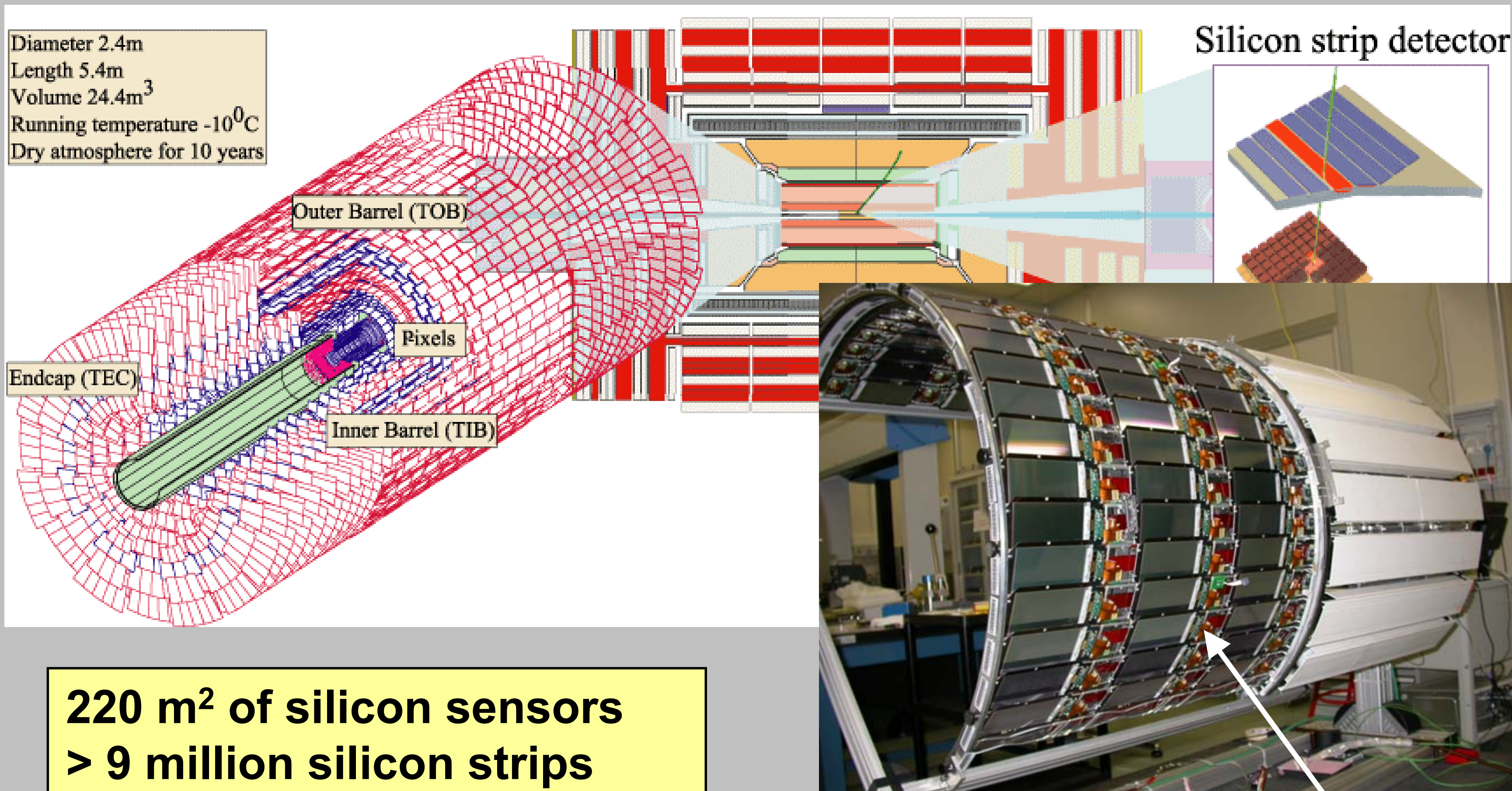




Long term project

Starts Operation 2007

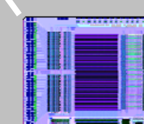
Counter rotating Proton beams ; bunch collision rate = 40 MHz ;

# CMS Construction



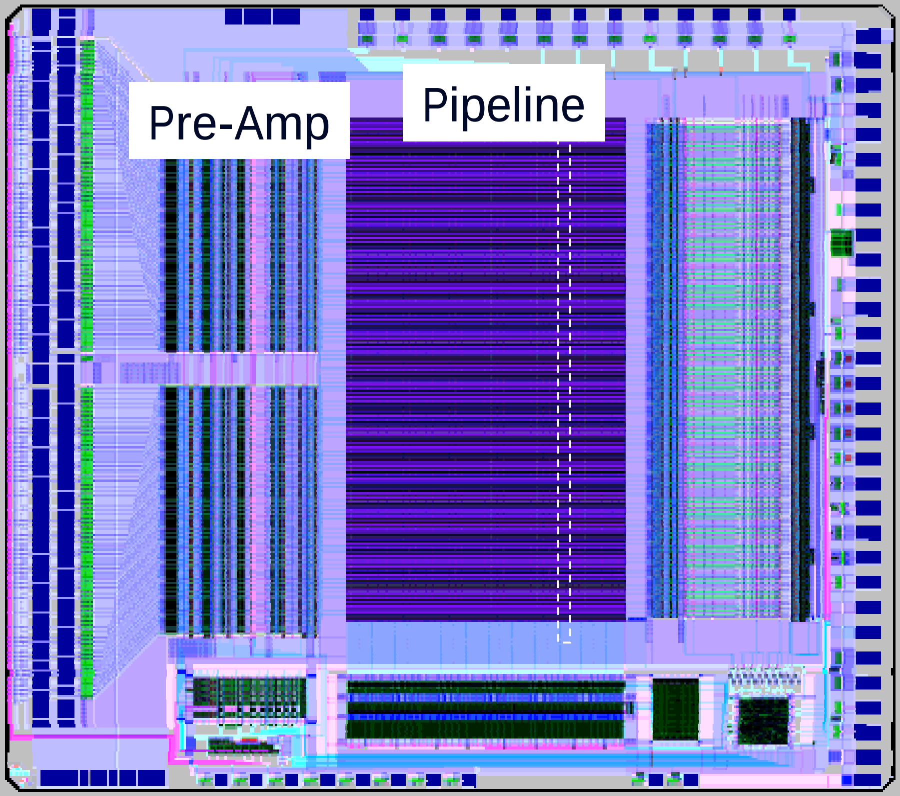

**220 m$^2$ of silicon sensors**
**> 9 million silicon strips**

**Charged Track reconstruction.**
**Very high Granularity.**



**Front End Electronics**

# Technology 1: ASIC Design




**APV25** ASIC MEDG Design

Analogue **PIPELINE** clocked @ 40 MHz

On Detector v High Radiation

Low Power ; Low Noise

0.25 IBM deep sub-micron process

Each chip handles 128 strips

Holds each 25 nsec sample till Trigger slice

Serial output of all 128 strips at 100 kHz

Total > 70,000 chips => > 9 million strips @ 100 kHz

# Technology 2: Data Acquisition

96 optical fibres inputs, each a Multiplexed pair of APVs

25,000 strips

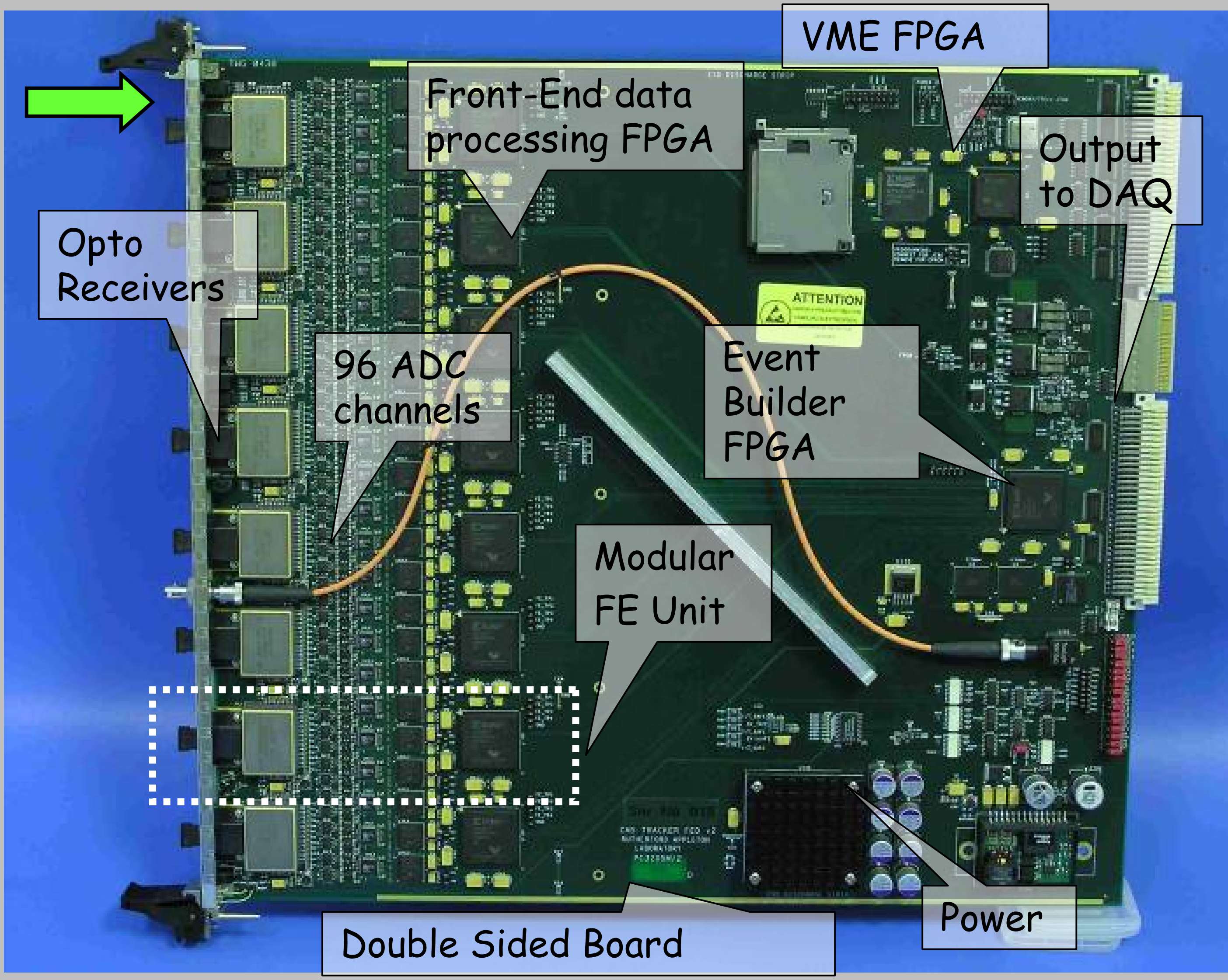
8 front end blocks each driven by a 12 way optical ribbon cable

Raw input data rate = 3.4 GB/s.

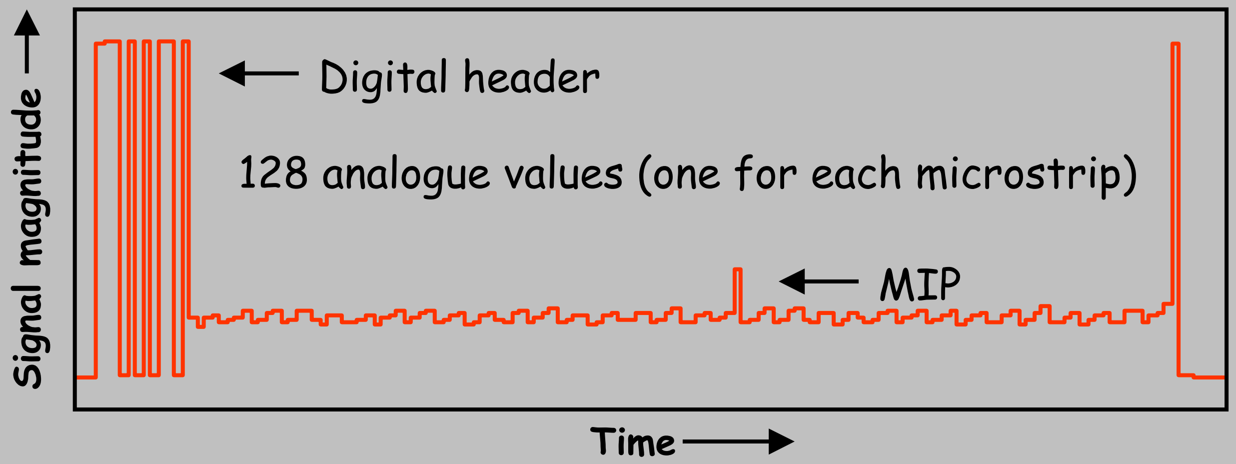
Extract hit strips

Processed Output rate

< 200 MB/s



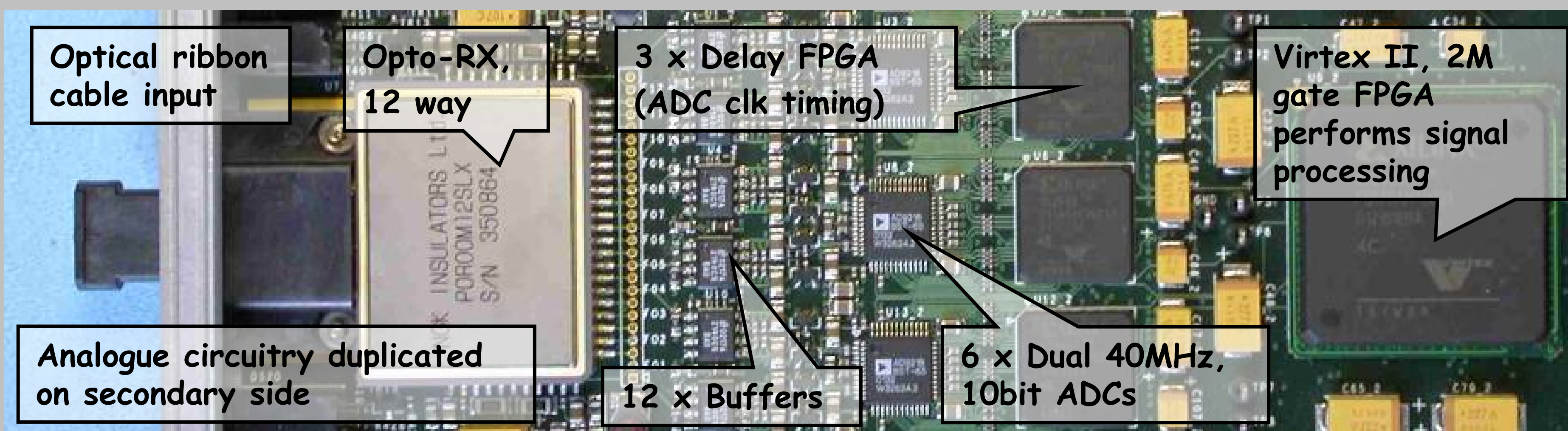
# CMS DAQ Processing



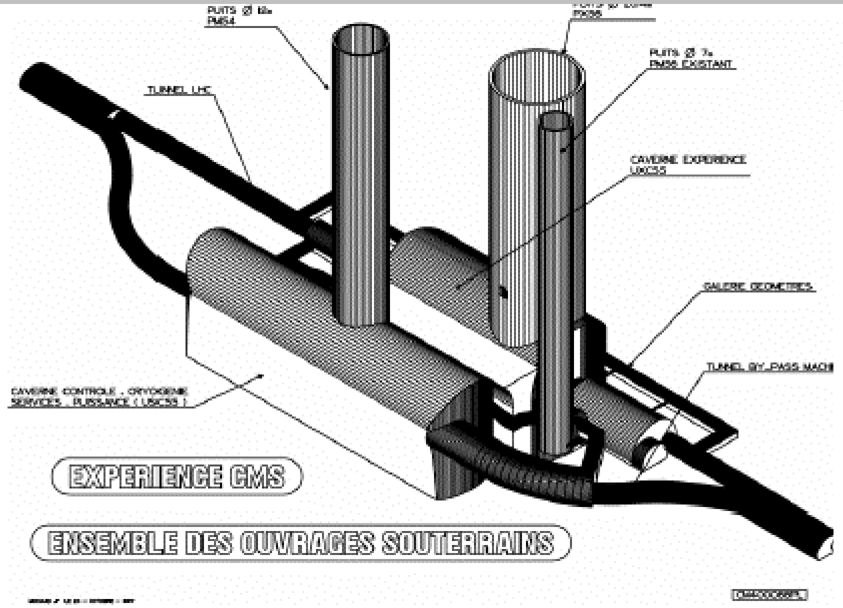

To extract hit need to perform:

- Common mode subtraction
- Pedestal subtraction
- Cluster finding
- Sync checking

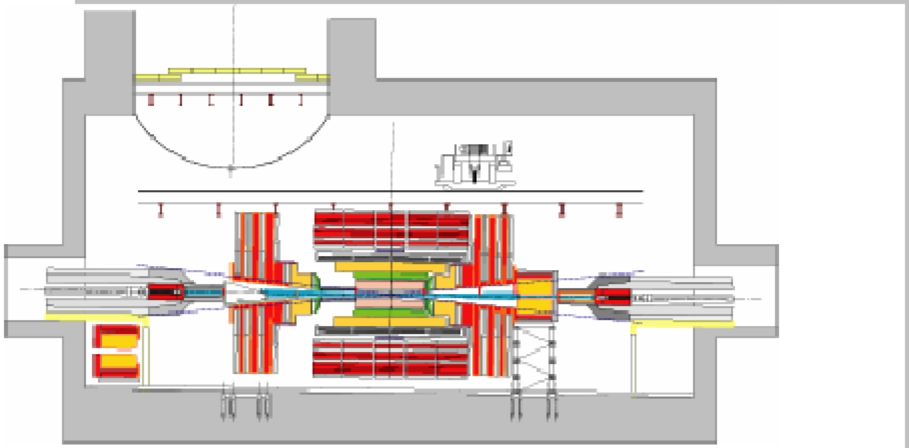
Opto-to-electrical conversion → Digitise & sync data → Find hit clusters



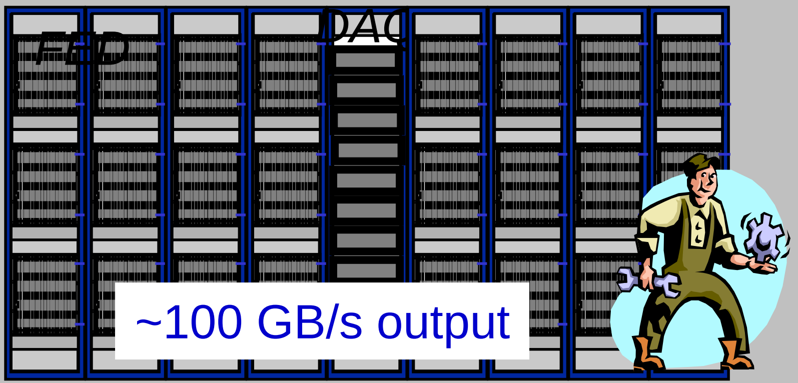
# CMS System Installation




*The underground area at point 5, showing the access shafts, the two large caverns and the wall between them*

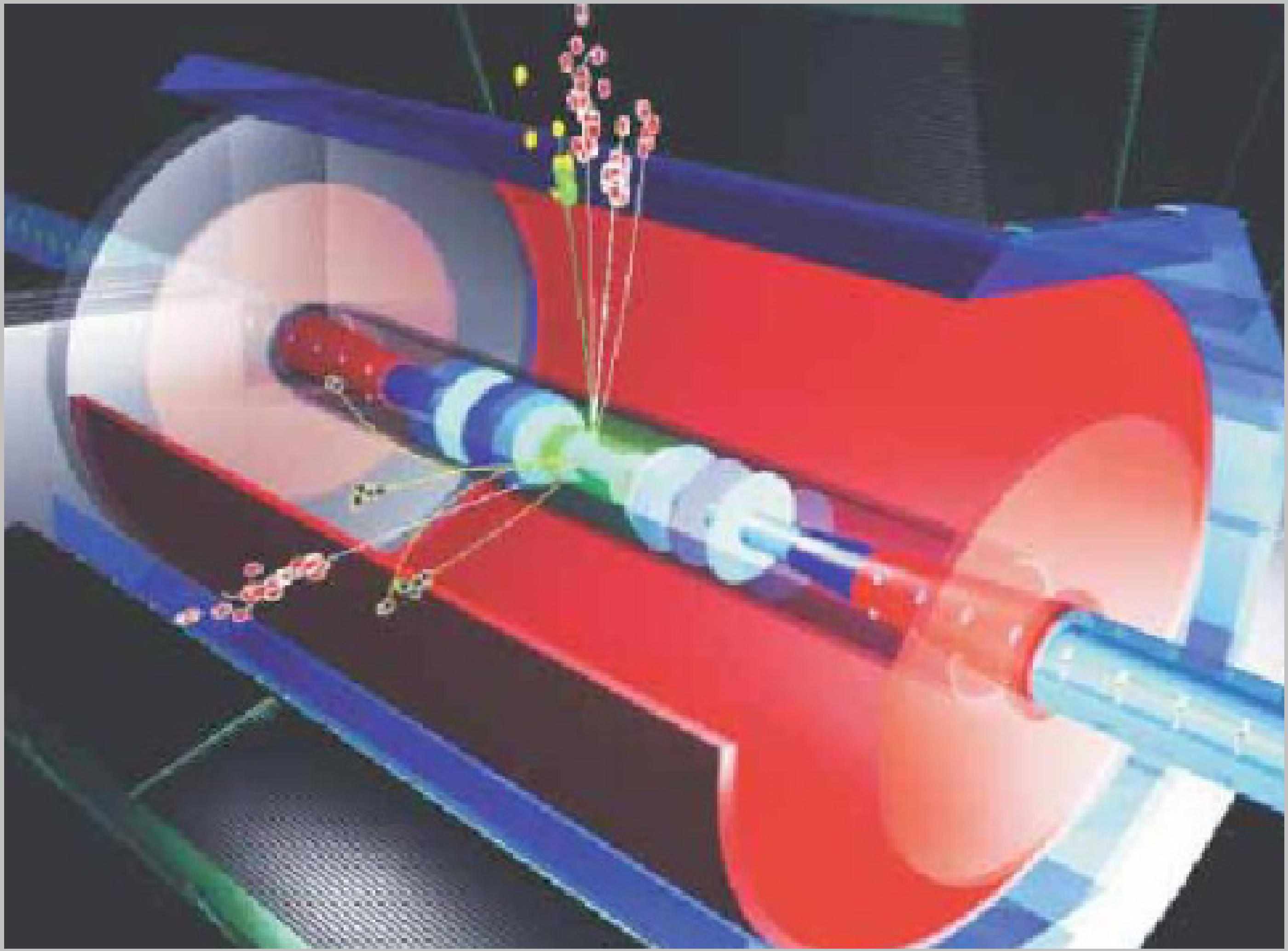


*The CMS detector being assembled in UXC55*




For 450 FEDs
30 VME crates
12 Racks electronics
Installation in Q2->Q3 / 2006

# Linear Collider Flavour Identifier (LCFI)

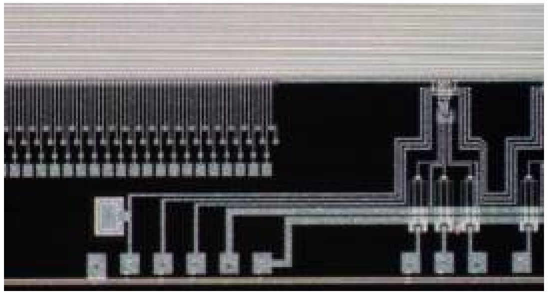


# Sensors – CPCCD (LCFI)

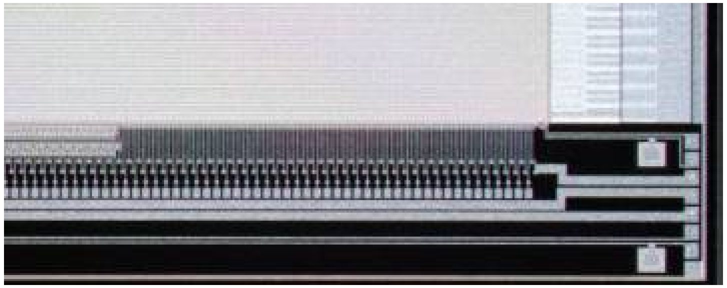
- Column parallel charge coupled device.
- First of these, CPCCD1, manufactured by e2v.

- Two phase, 400 (V) × 750 (H) pixels of size 20 × 20 μm$^2$.
- Metal strapping of clock gates.
- Two different gate shapes.
- Two different implant levels.

- Wire/bump bond connections to readout chip and external electronics.
  - Direct connections and 2-stage source followers:

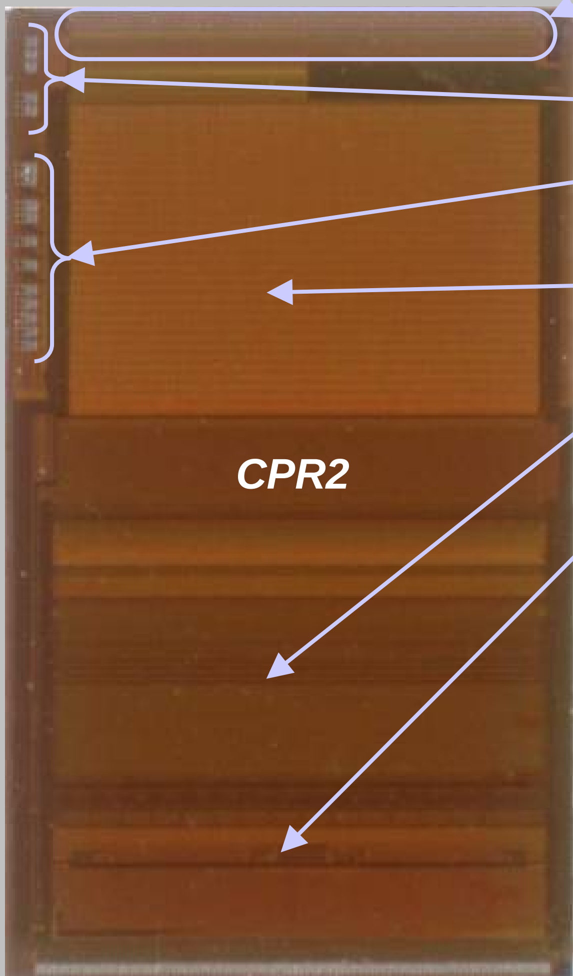


  - Direct connections and single stage source followers (20 μm pitch):



# Current ASIC Development:  CPR

**Bump bond pads**




**Wire/Bump bond pads**

**Voltage and charge amplifiers 125 channels each**

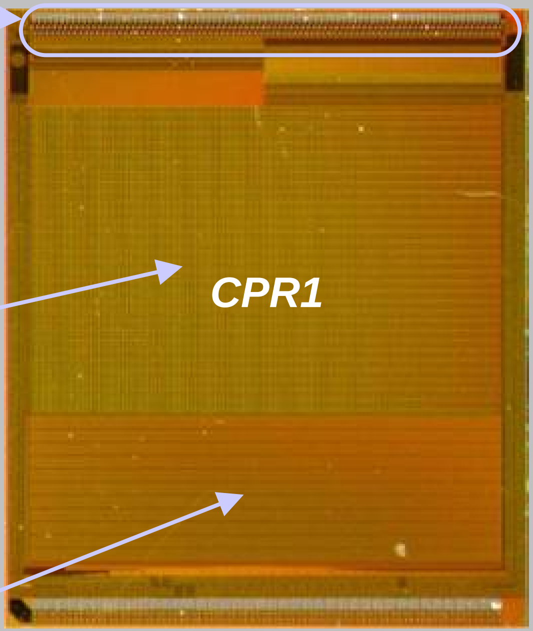
**Analogue test I/O**

**Digital test I/O**

**5-bit flash ADCs on 20 µm pitch**

**Cluster finding logic (2×2 kernel)**

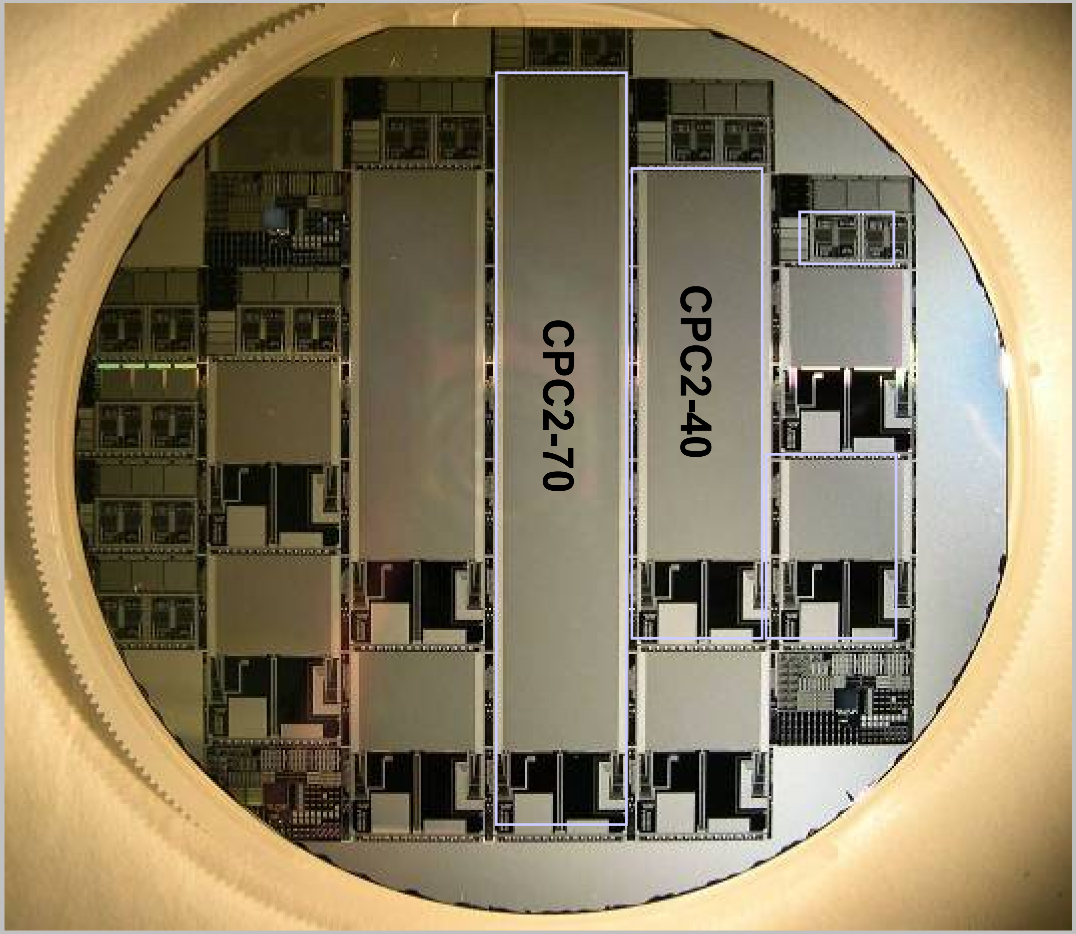
**Sparse readout circuitry**




**FIFO**

- **CPR2 designed for CPC2**
- **Results from CPR1 taken into account**
- **Designed by the Microelectronics Group at RAL**
- **Size : 6 mm × 9.5 mm**
- **0.25 µm CMOS process (IBM)**
- **Manufactured and delivered February 2005**

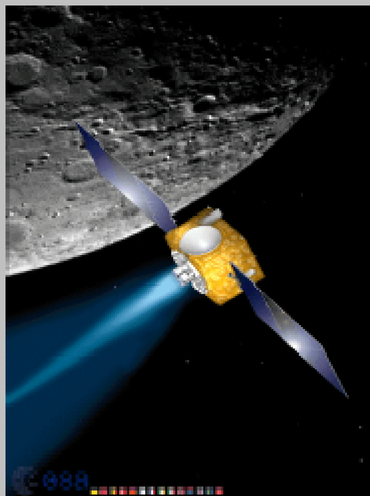
# CCD Development:  E2V



# Example Detector Technologies

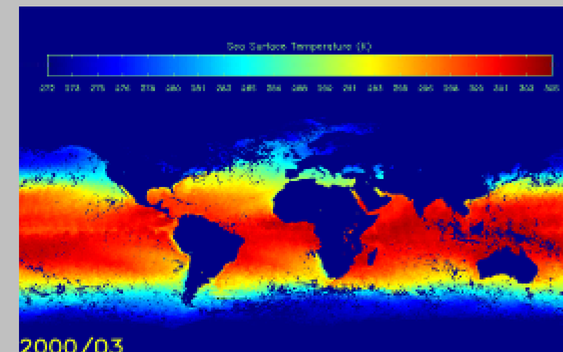
- Particle Physics:
  - Sensor Instrumentation
  - Microelectronics
  - DAQ Systems
- Space Science:
  - Instrument Systems
  - CMOS Sensors
  - Data conversion
- Future Trends

# Space

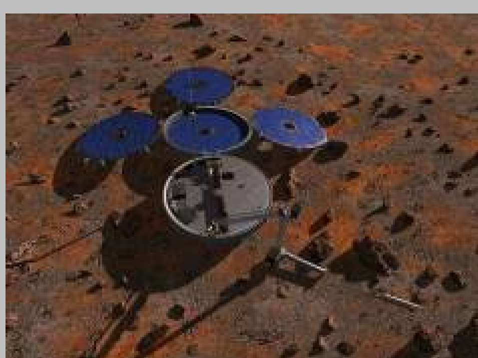


MOON

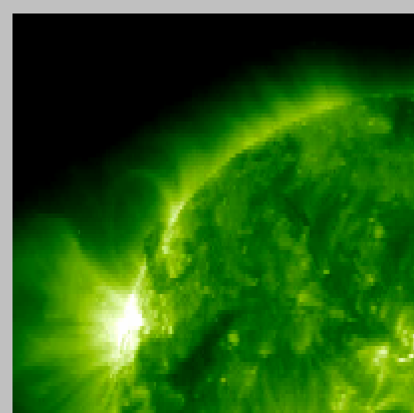
LAND



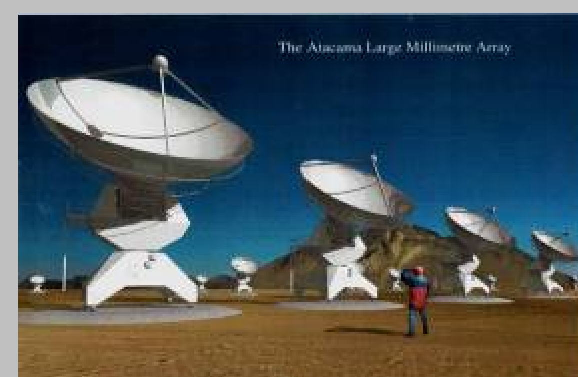

SEA



PLANETS

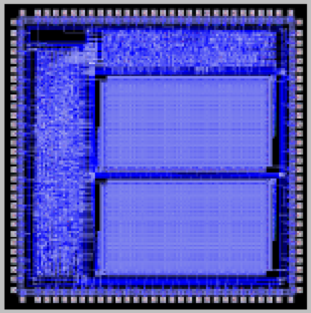


SUN




GALAXIES

# Instrument Example: Rosetta Space Craft

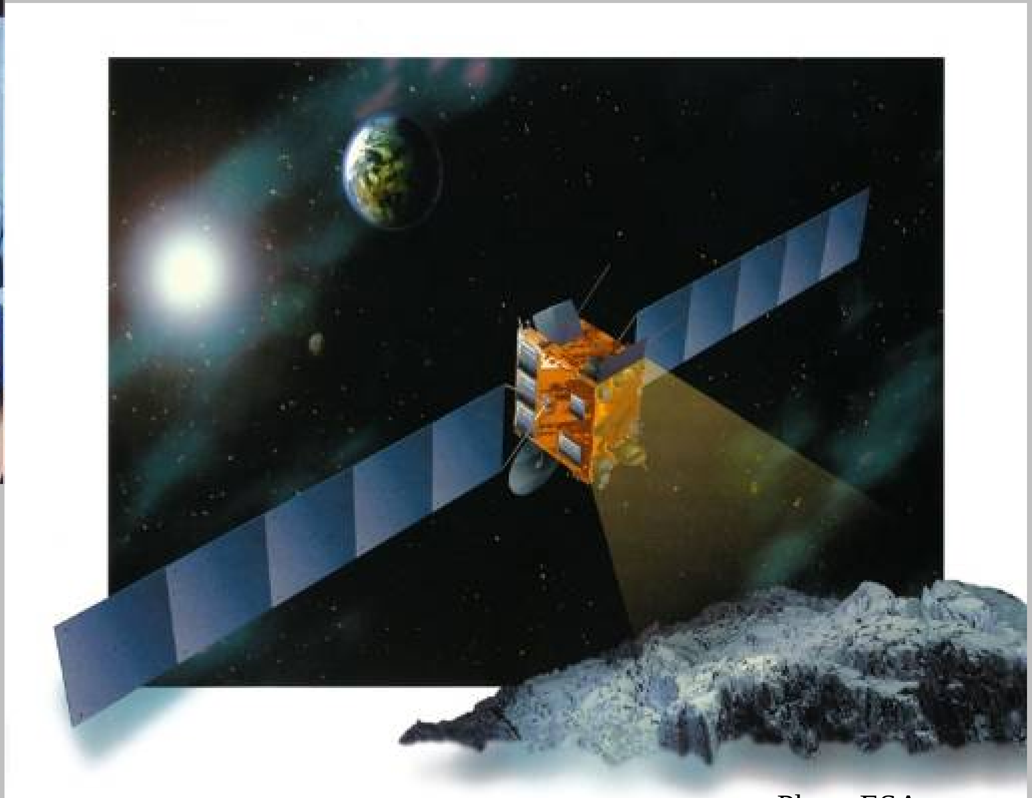
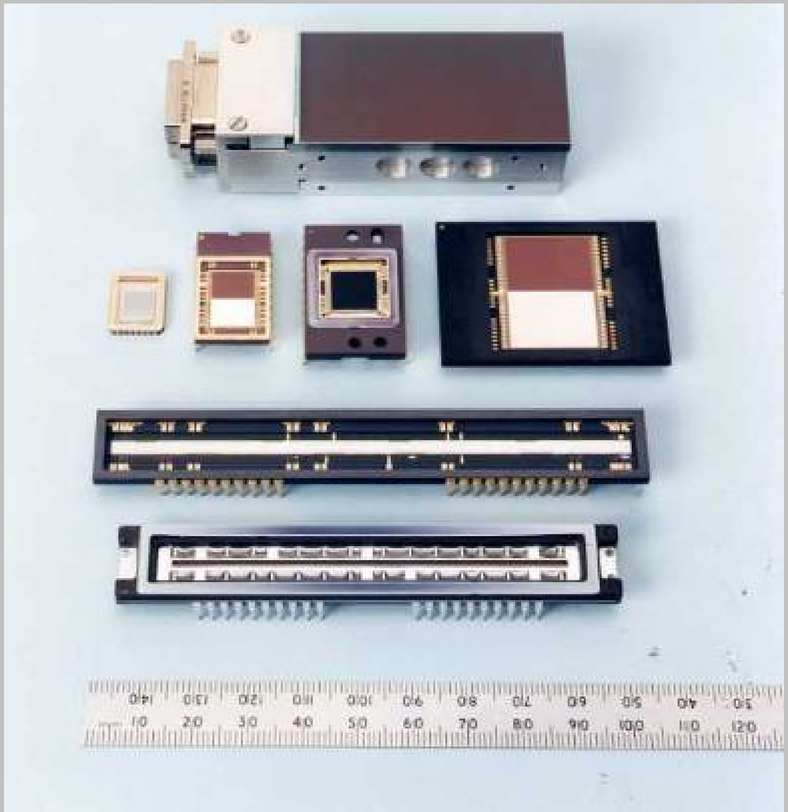


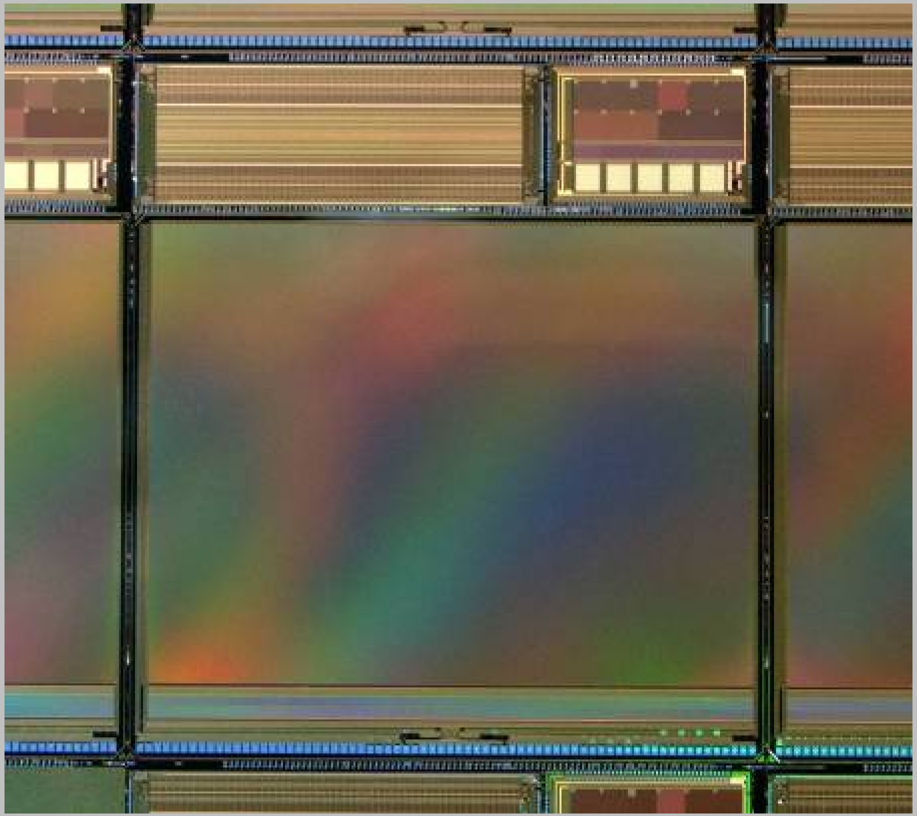
Photo ESA

ASIC: 0.8um DMILL process

# Manufactured 3Kx4K Sensor



Various CCD Sensors



Large format CMOS devices

# CMOS Imaging

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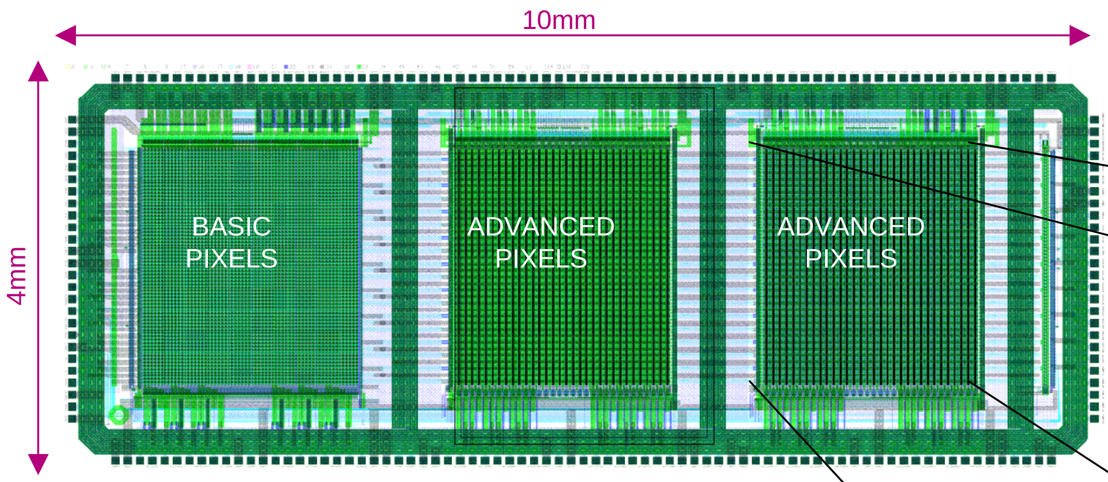
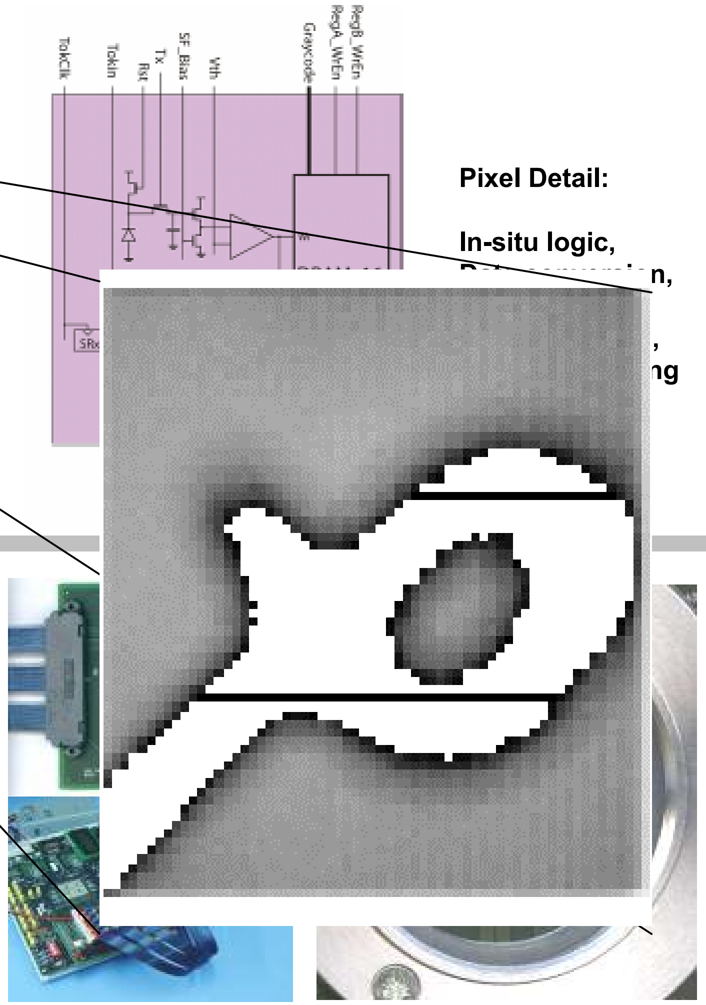
## Mi3 Project: Advanced Pixels OPIC

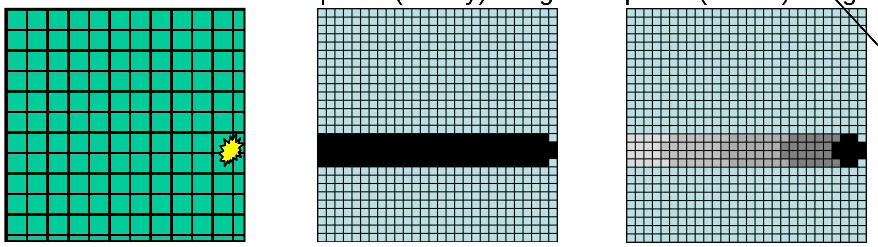



**Basic Technology MI3 Development Sensor (J Crooks)**




**Pixel Detail:**

**In-situ logic,**




Single Frame

Time-of-flight 20us

Binary image of pixels hit along the way

Timing information from hit pixels gives 80ns resolution

**Moving Image Timed Capture**

**Test Rig**

# CMOS Sensors: Current priorities

## Pixel/sensor design

- Reduce noise
- Faster readout
- Data processing

## Enhance spectral window

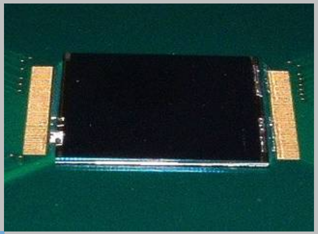
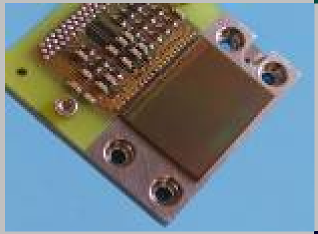
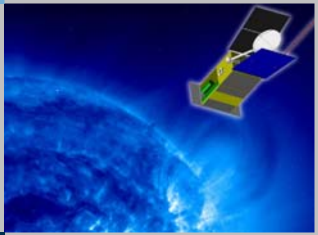
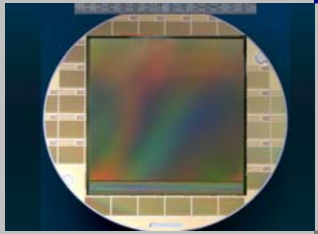
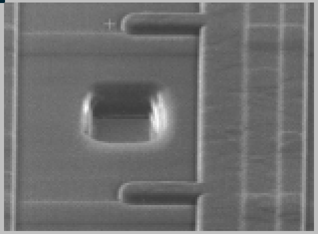
- Eliminate substrate for UV/low energy electrons
- Couple with scintillators of other materials for X and $\gamma$-rays

## Radiation resistance

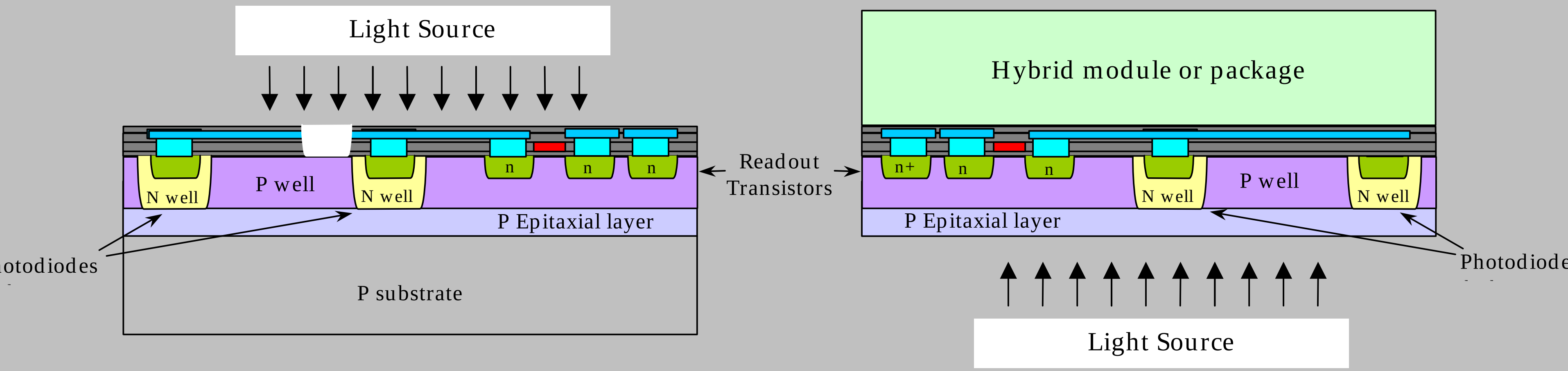
- OK for Linear Collider or in space
- what about the radiation levels found in LHC or other experiments?

## Very large area sensors

- Sensor larger than 2 cm side

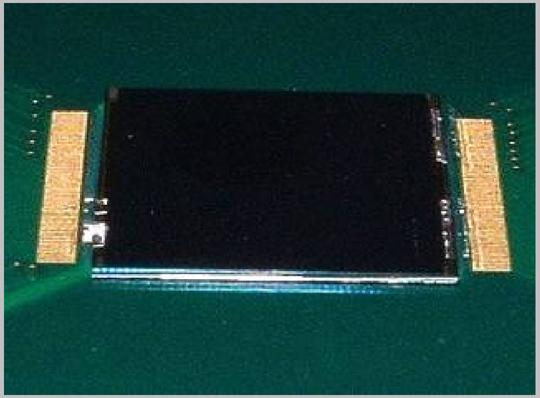
# Front & Back illumination



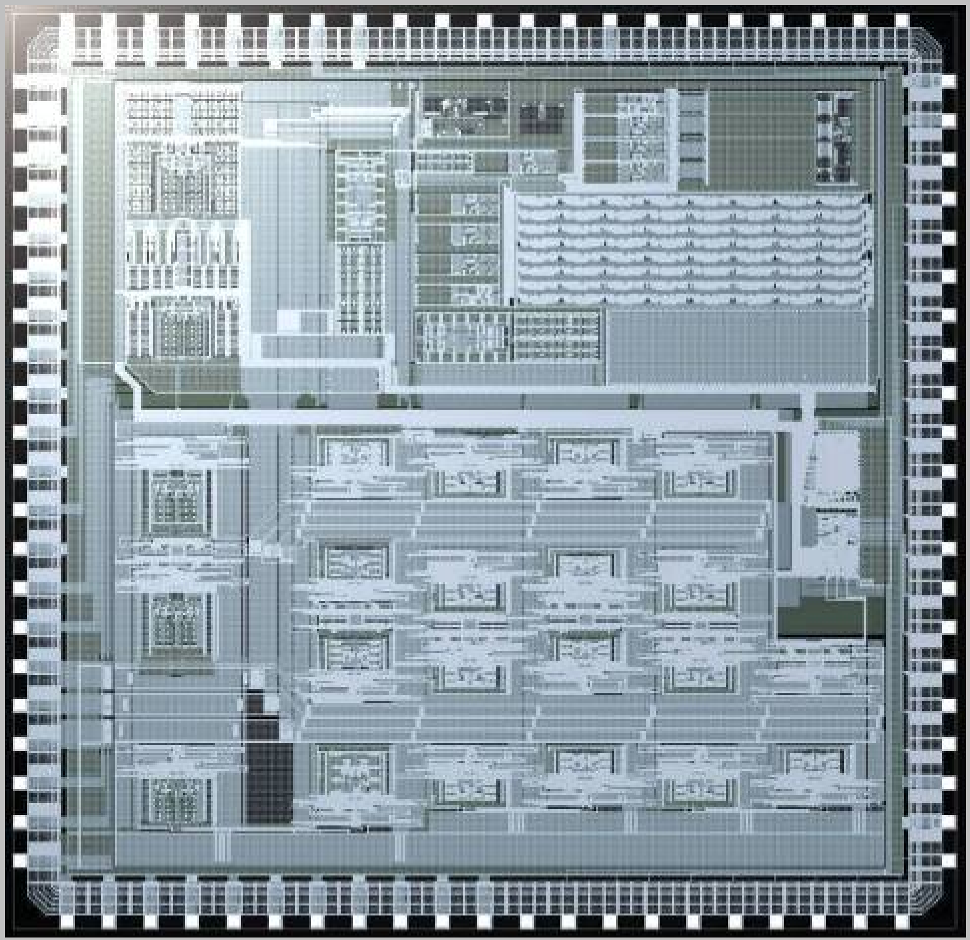

**Front illuminated Etched MAPS**

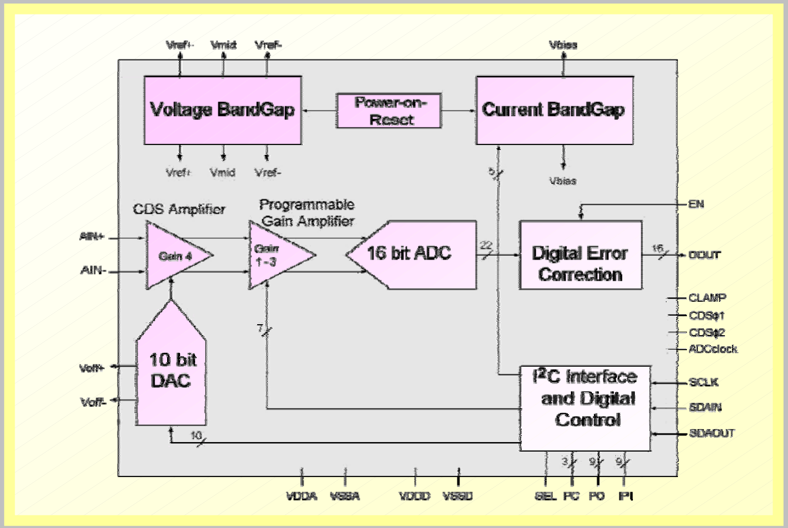
**Back illuminated Thinned MAPS**

**E2v collaboration:**
**Thinned CMOS Sensors**



# Example ASIC Development: CDS ADC



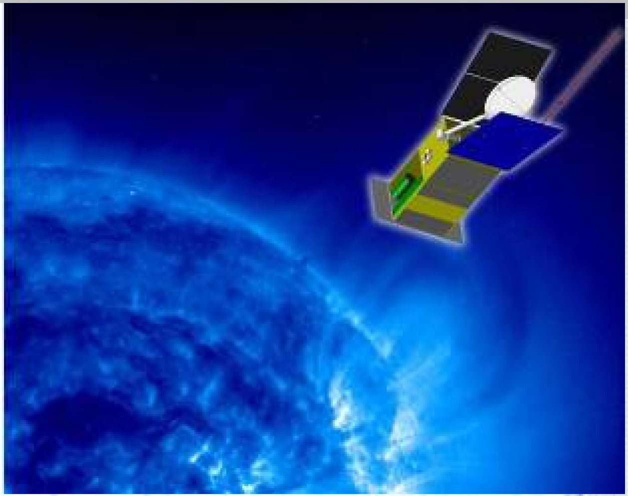


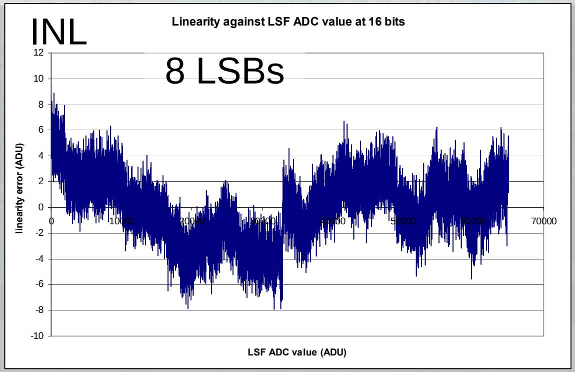

❑ **CCD Image processing chip**

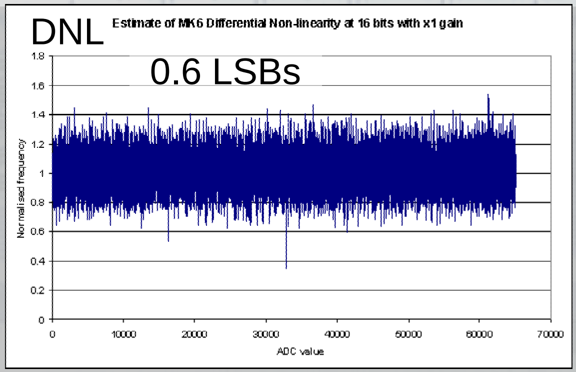
- Correlated Double Sampling
- Programmable Offset / Gain
- On–Chip Reference
- Digital Interface

# CDS ADC Performance

- A 16 bit pipelined ADC
- CCD signal processing chip
- Current Sample rate = 2.5MHz
- Fully differential architecture
- No missing or repeating codes





# Example Detector Technologies

- Particle Physics:
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- Space Science:
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- Future Trends

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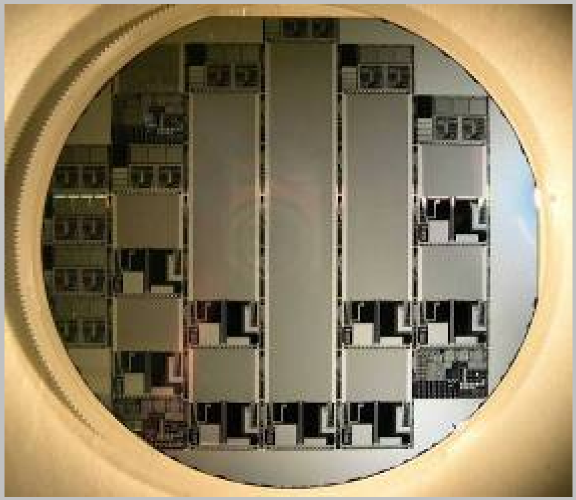
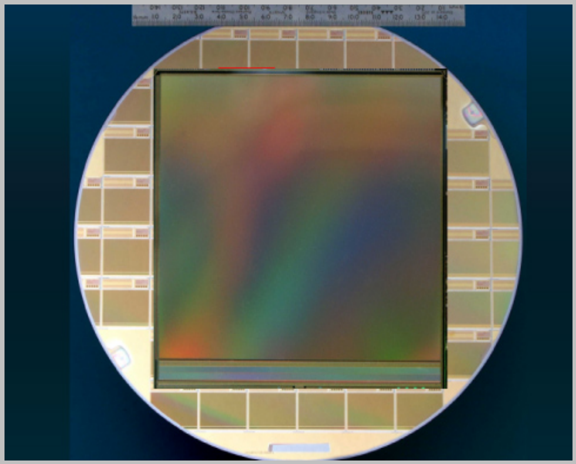
# Future Trends

- Particle Physics (2 examples):
  - LHC Upgrades
    - More stringent ASIC requirements
    - More sophisticated data processing
  - LCFI
    - CCD and APS solutions in development
    - Very large area >100Mpixels
    - Drive for low mass in detector storage
- Space Science:
  - Performance
    - Lower power and noise
    - Enhanced spectral performance
  - Reliability
    - Rugged design
    - Radiation hardness





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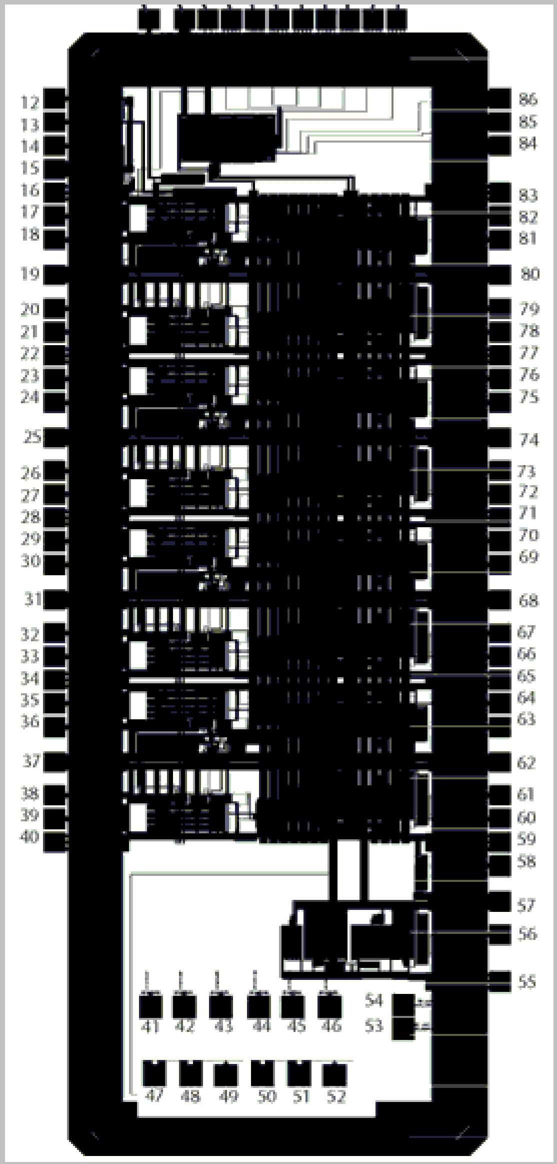
- Who we are
- Example technologies
  - Particle physics
  - Space Science
- ASIC Goup
  - Current Nuclear Structure physics activity
  - Ideas for Nustar
    - Details for Aida
    - Other experiments – EXL and R3B
- DAQ Systems
  - Current activity and trends
- Summary

# Germanium Amplifier ASIC

- Parallel High and Low Gain
- Integrated input FET
- Ramp feedback system
- Low noise 0.35um technology

For combination with DAQ:

- future ADC
- timing etc.



# ASIC Possibilities for NuSTAR

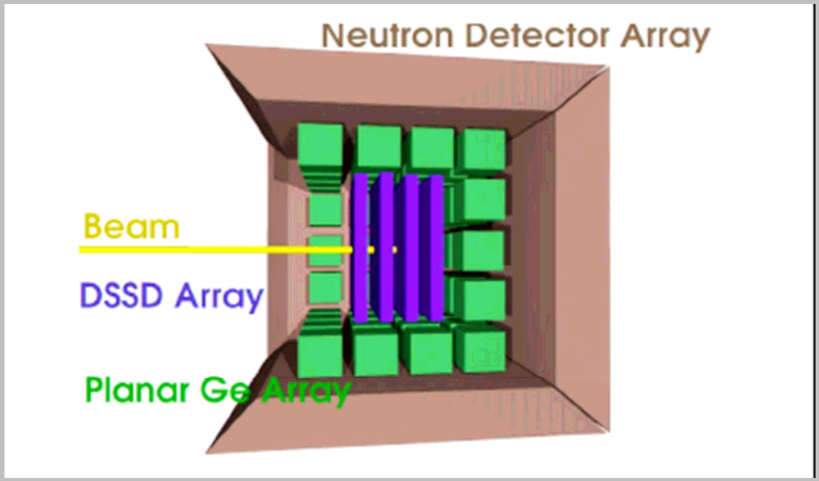
Examples currently identified:

- Fast recovery after implantation of ion in DSSD Si to measure decay in the same pixel.

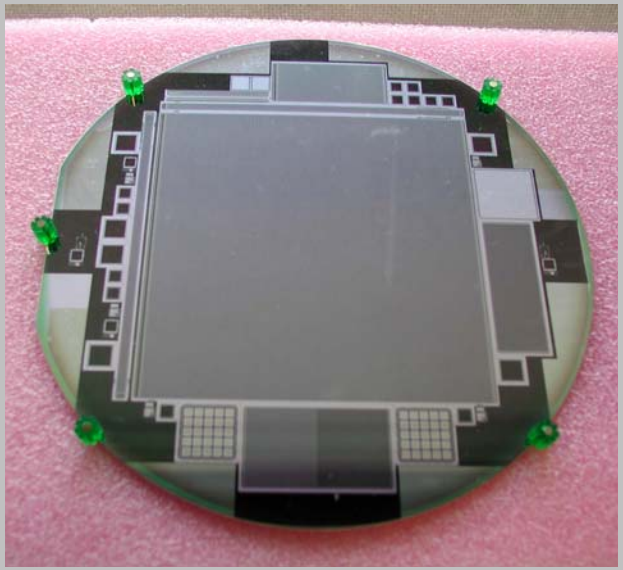
- EXL CsI calorimeters covering energy range 300keV to 500MeV. 13k channels needed.

- EXL/R3B Si strip and SiLi detector ASIC. Normal Si processing chain of preamp, shaper, mux or ADC, timing. Add PSD too. Maybe 2 ASIC solution?

# Concept and the detector

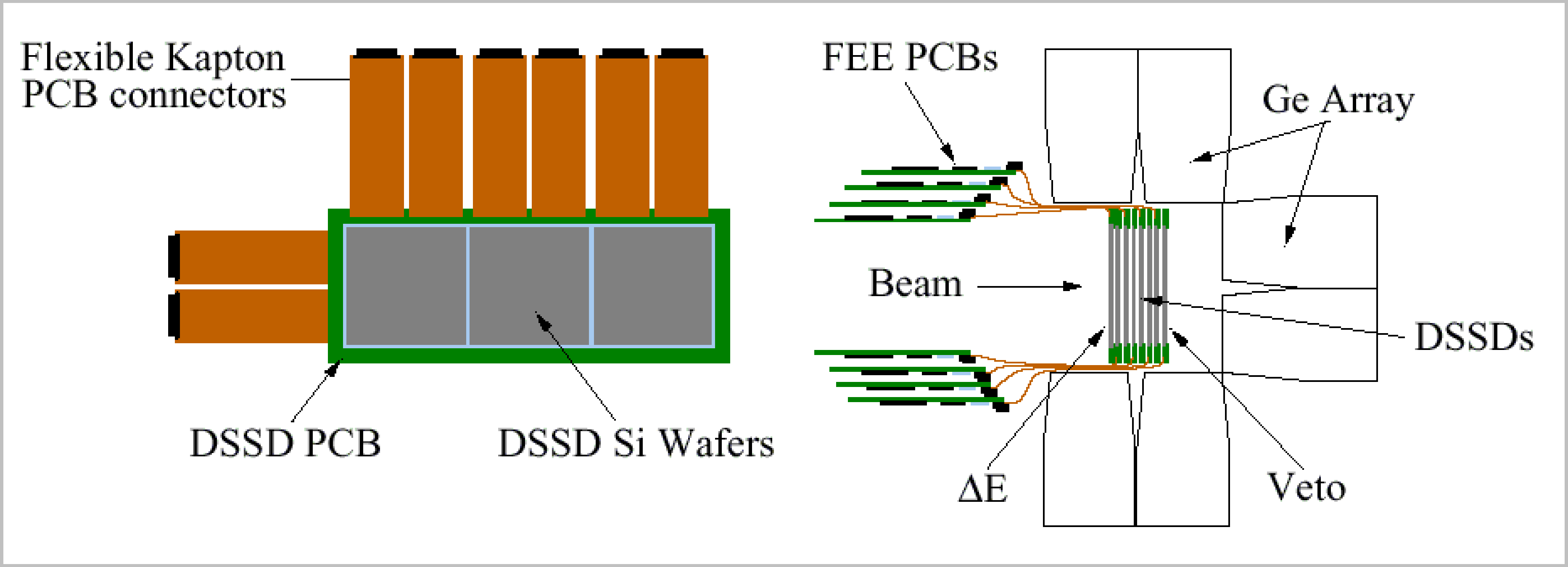



- Super FRS Low Energy Branch (LEB)
- Exotic nuclei – energies ~50-150MeV/u
- Implanted into multi-plane DSSD array
- Implant - decay correlations
- Multi-GeV DSSD implantation events
- Observe subsequent p, 2p, $\alpha$, $\beta$, $\gamma$, $\beta$p, $\beta$n … decays
- Measure half lives, branching ratios, decay energies …



6" wafer-10cm x 10cm area
- 1mm wafer thickness
- Integrated components
  - a.c. coupling
  - polysilicon bias resistors
  
  … important for ASICs
- Series strip bonding (3 together)

# General Arrangement



# DSSD Segmentation

We need to implant at high rates *and* to observe implant – decay correlations for decays with long half lives.

DSSD segmentation ensures average time between implants for given *x,y* quasi-pixel >> decay half life to be observed.

- Implantation profile
  $\sigma_x \sim \sigma_y \sim 2cm$
  $\sigma_z \sim 1mm$
- Implantation rate (8cm x 24cm) ~ 10kHz, ~kHz per isotope (say)
- Longest half life to be observed ~ seconds

Implies quasi-pixel dimensions ~ 0.5mm x 0.5mm

Segmentation also has instrumentation performance benefits

# Instrumentation

**Why use of Application Specific Integrated Circuit (ASIC) technology?**

- Large number of channels required (8 x (128+(3x128))= 4096)
- Limited available space
- Cost

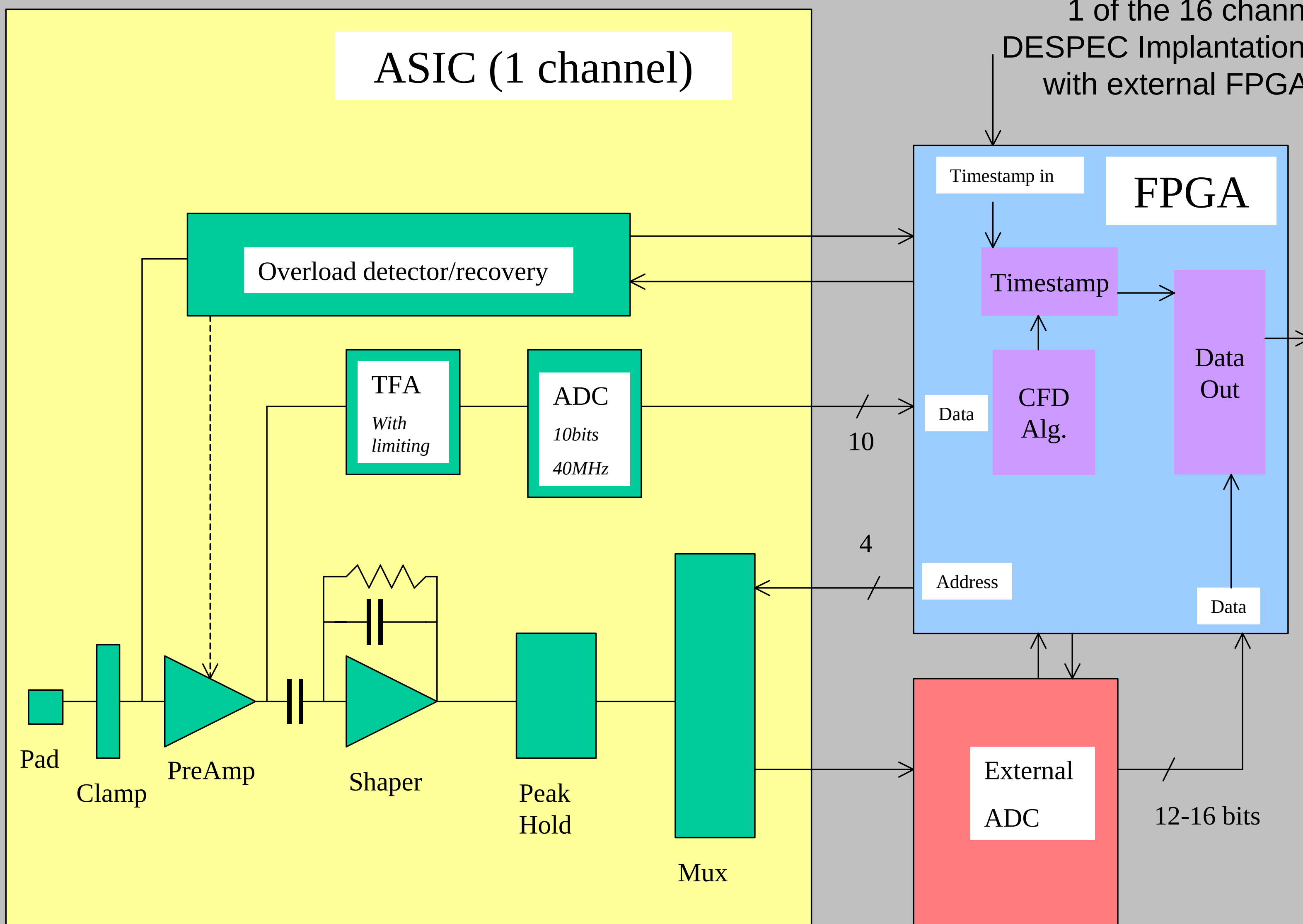
**Outline ASIC Specification**

- Selectable gain: low 20GeV FSR
  high 20MeV FSR
- Noise $\sigma$ ~ 5keV rms.
- Selectable threshold: minimum ~ 25keV @ high gain ( assume 5$\sigma$ )
- Integral and differential non-linearity
- Autonomous overload recovery ~$\mu$s
- Signal processing time <10$\mu$s (decay-decay correlations)
- Receive timestamp data
- Timing trigger for coincidences with other detector systems

*DSSD segmentation reduces input loading of preamplifier and enables excellent noise performance.*

# AIDA for DESPEC

1 of the 16 channels in the DESPEC Implantation ASIC (shown with external FPGA and ADC)



# Other ASIC Possibilities for NuSTAR

Examples currently identified:

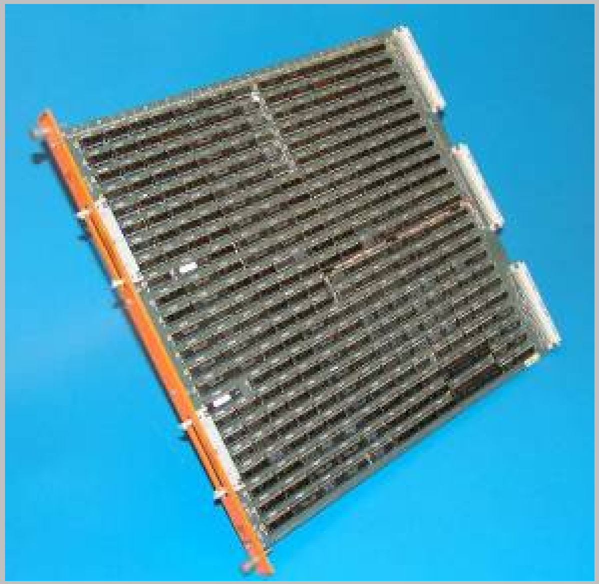
- Fast recovery after implantation of ion in DSSD Si to measure decay in the same pixel.

- EXL CsI calorimeters covering energy range 300keV to 500MeV. 13k channels needed.

- EXL/R3B Si strip and SiLi detector ASIC. Normal Si processing chain of preamp, shaper, mux or ADC, timing. Add PSD too. Maybe 2 ASIC solution?

- Who we are
- Example technologies
  - Particle physics
  - Space Science
- ASIC Goup
  - Current Nuclear Structure physics activity
  - Ideas for Nustar
    - Details for Aida
    - Other experiments – EXL and R3B
- DAQ Systems
  - Current activity and trends
- Summary

# DAQ History



<u>1980</u>

- 300 MSI chips

<u>1988</u>

12 x 2K Gate FPGA

80 x 64Kx4 SRAM

10 PALs

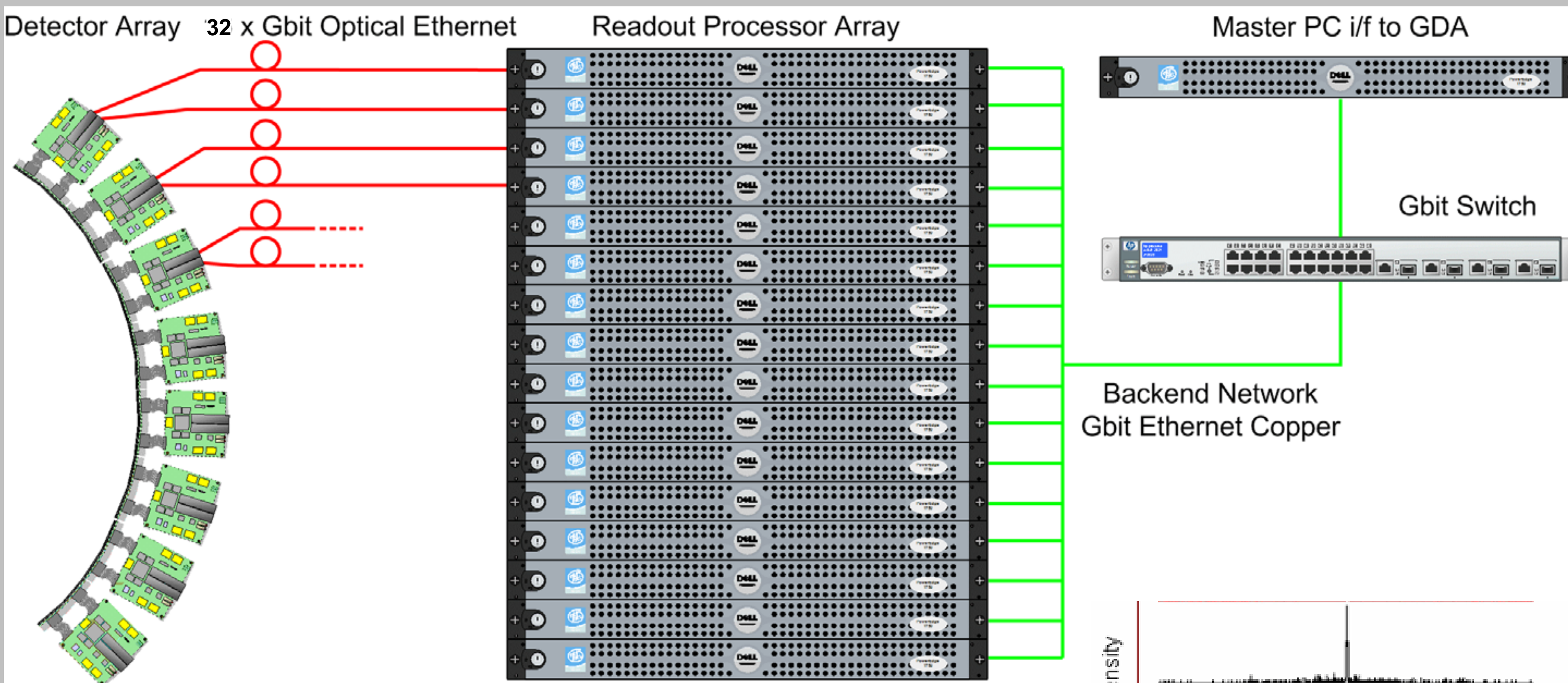
<u>2004</u>

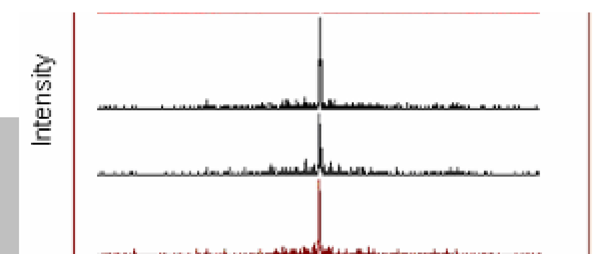
34 x FPGA

3 M Gate Virtex II

40 BGAs

# Commercial Off Detector Electronics

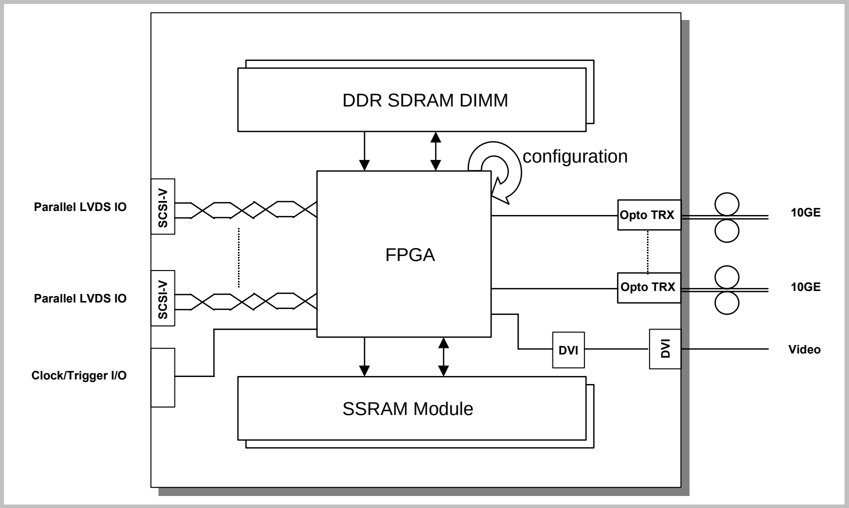


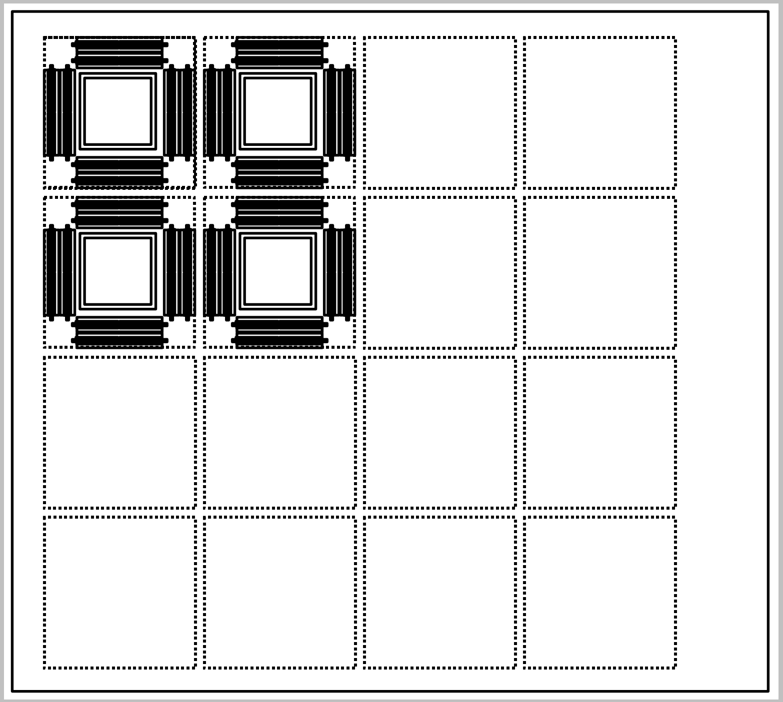




**10 Gbyte/s**

**2.5 Gbyte/s**

# Next Step: FPGA Computing



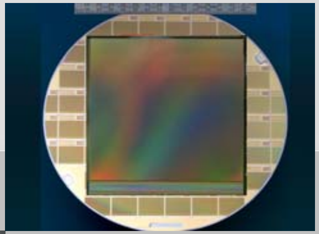
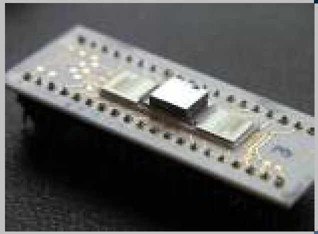
General observations:

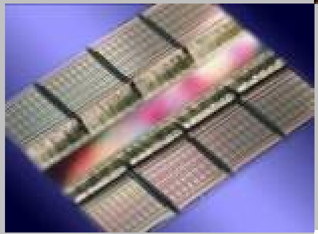
- Future experiments always demand more data processing and reduction
- FPGAs offer a flexible multiprocessor offer massive compute potential
- Fibres permit very high data rates from instruments to processors

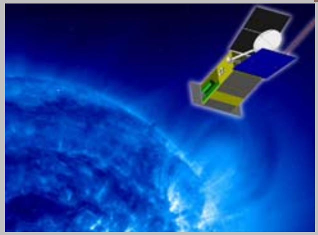
# Summary

Instrument Technology:

- ASIC Design
  - Analogue, Low Power
  - Industrial technologies, CMOS based
- Imaging Devices
  - CCD and CMOS solutions
  - Complex designs, Novel architectures
- DAQ Systems
  - Large data processing capabilities
  - Multiprocessor fibre based systems
- New Projects for FAIR:
  - Aida  DSSD Readout
  - EXL CsI calorimeters
  - EXL/R3B Si Strip and SiLi detector ASIC





# And more technology..