Specification for the MACB

The purpose of the box is to allow Correlation with other DAQ systems and the AIDA/LYCCA systems to exchange signals for identifying events, to distribute the signals required by the FEE64 Timestamping and buffer the Triggers from the ASICs.

The MACB unit can operate as a standalone system, generating its own 50MHz clock or it can distribute an external clock. It can operate standalone for a small number of FEE64s or be extended as part of a hierarchy to operate with many FEE64s.

The Correlation DAQ side of the interface uses Fast NIM signals via Lemo 00 connectors and is isolated from AIDA/LYCCA which uses 3.3v logic. The Timestamping signals are distributed as LVDS and a hierarchy of boxes is used to ensure that signal skew between signals delivered to the FEE64 units is minimised. The ASIC Triggers from the FEE64 units are output from the MACB as isolated Fast NIM via Lemo 00 sockets. The box is in NIM format and is supplied from the NIM power supplies. The box should be in a NIM crate within the AIDA/LYCCA experiment.

Table of signals required for Correlation DAQ. (Fast NIM, Lemo 00 sockets) This table shows the Correlation DAQ configuration of the 8 available Fast NIM Lemo 00 sockets (4 in and 4 out).

Signal name	Source	Specification
Clock10	FEE64 Master unit	10MHz clock used to synchronise activity between the two systems.
Correlation DAQ Accepted Trigger	Correlation DAQ	Pulse of 150nS minimum duration to indicate readout the scaler and transmit an event (block of data)
Scaler reset request	Correlation DAQ	Pulse of 150nS minimum duration to indicate a scaler reset is required.
Scaler reset	FEE64 Master unit	Pulse indicating the rising edge of Clock10 to use to reset the scaler.

For other applications these 8 Fast NIM connections can be reconfigured to give any combination of 4 signals to/from the FEE64 card.

One MACB unit interfaces to up to 4 FEE64 cards as shown below.

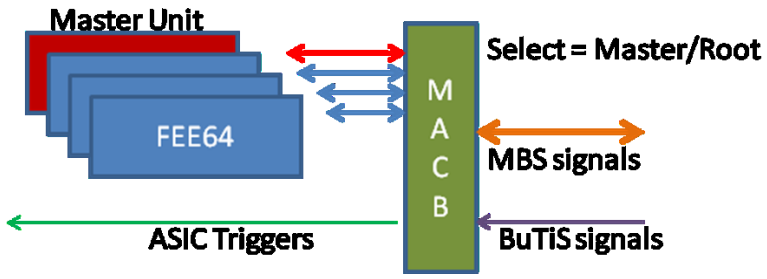

Illustration showing the unit interconnections for four or less FEE64 units.

Larger numbers of FEE64 cards can be controlled by a branch structure of multiple MACB cards interconnected by HDMI type C cables. Each MACB has 5 HDMI connectors one connects to the next level up the hierarchy and 4 connect either to FEE64 cards or to MACB units lower in the hierarchy. FEE64 cards should all be connected at the same level of hierarchy in order to match signal delays. The number of branches can be extended as far as necessary (1 level for up to 4 FEE64, 2 levels for up to 16 FEE64, 3 levels for up to 64 FEE64, 4 levels for up to 256 FEE64 etc.)

The following diagram shows a multi-level configuration.

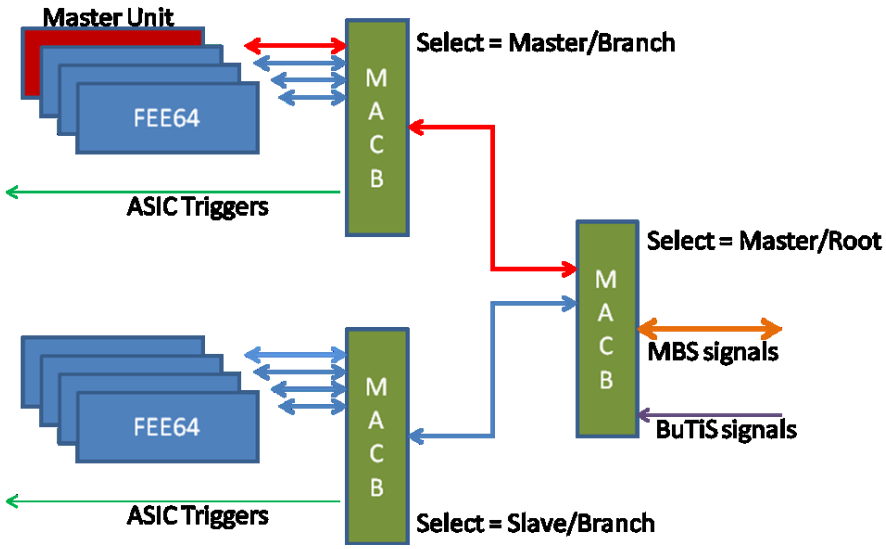

Illustration showing the unit interconnections for five or more FEE64 units.

NOTE: THE MASTER FEE64 MUST ALWAYS BE CONNECTED THROUGH PORT 1 OF THE MASTER SELECTED MACB.

The MACB units can be configured in several different ways depending on where they are in the hierarchy, whether they use the external clock or generate their own, whether they are connected to an FEE64 master or not and whether the Lemo 00 connections are configured in Correlation DAQ mode described earlier or in another configuration.

A 16 position rotary switch at the front panel of the MACB determines the function of the module.

- Master/Slave for FEE64 Timestamping.
- External/MACB for Clock source.
- Root/Branch for the interconnection hierarchy.
- Correlation DAQ for the isolated Fast NIM signals.

The switching of the signals within the MACB is handled by high speed low skew multiplexers for the Timestamping and a JTAG programmed Xilinx CoolRunner II CPLD for all others.

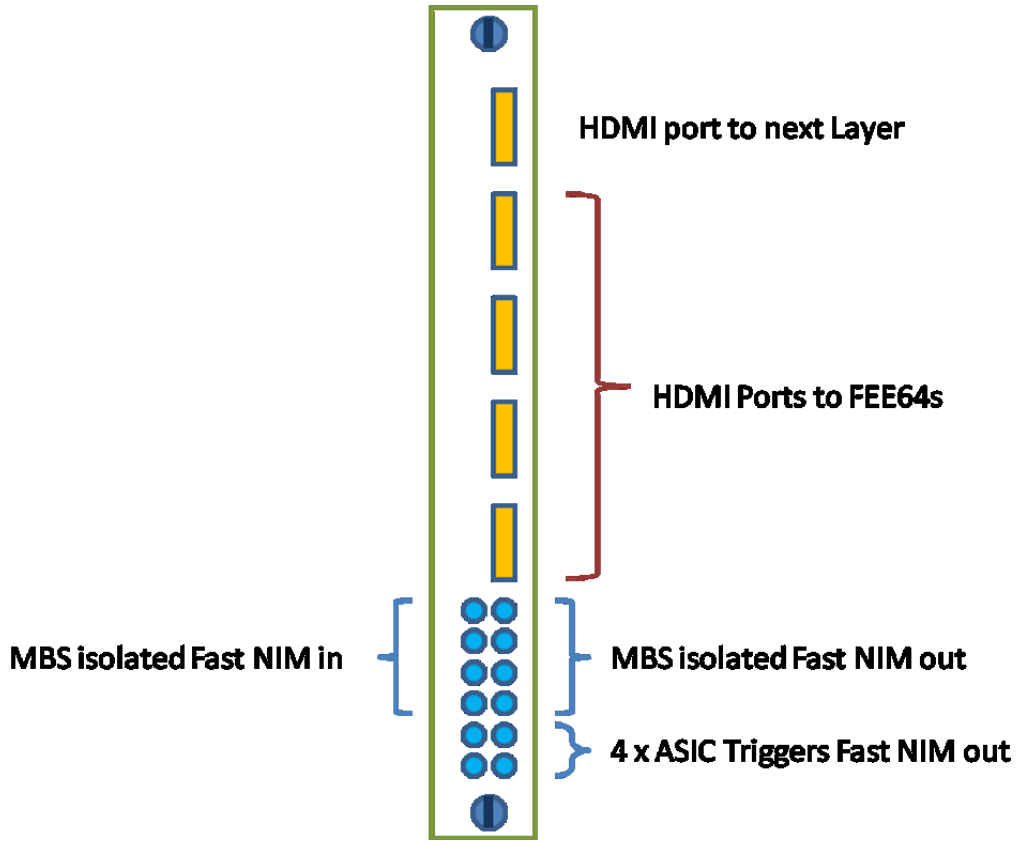

Illustration of the front panel of the MACB NIM unit.

External Clock and SYNC SMA connectors are on the back panel. The JTAG port is accessible through the side.

The functions of the MACB unit in different configurations and the routing of the signals within the unit are detailed in the following tables. Some useful definitions of terms used in the tables:

Definitions:

Master- means that HDMI port 1 is connected to the Master FEE card which generates Sync pulses for the whole system when using the internal 50MHz clock. Port 1 FEE card both generates the sync (via the Sync return line) and receives it again at the same time as the other 3 ports (via the Sync line). Port 1 FEE card also generates the Correlation DAQ 10MHz clock and responds to the Correlation DAQ scaler reset request, generating a Correlation DAQ Scaler reset output (Ports 2-4 are configured to use Correlation DAQ Clock as an input and ignore Scaler Reset Request).

Slave Not operating in Master mode so all 4 HDMI ports behave the same (receives syncs, never generates them; Correlation DAQ Clock is an input).

Root- top level of hierarchy- provides all clock and sync signals. This is the point where Correlation DAQ connects to the Lemo 00 inputs/outputs. ASIC trigger Lemo output is the OR of the FEE cards connected lower in the hierarchy or the FEE card connected to the Port.

Branch- lower level of hierarchy- receives and passes on all clock and sync signals. In Correlation DAQ mode, the only Lemo 00 socket in use is the ASIC trigger output.

Table of signals distributed for the Timestamping FEE64 Master units

Signal name	Source	Specification
Clock	MACB Root or External SMA	50MHz clock signal in LVDS.
SYNC	MACB Root or External SMA	Pulse indicating the clock edge to synchronise the Timestamping counters in all the FEE64 units. In LVDS.
Master_SYNC *(using sync return)*	FEE64 unit	The SYNC pulse for distribution (From the master FEE64 card)

Table of signals distributed for the Timestamping FEE64 slave units

Signal name	Source	Specification
Clock	MACB Root or External SMA	50MHz clock signal in LVDS.
SYNC	MACB Root or External SMA	Pulse indicating the clock edge to synchronise the Timestamping counters in all the FEE64 units. In LVDS.
SYNC_Return	FEE64 unit	The SYNC pulse looped back in the FPGA of the FEE64. In LVDS.

Table of signals in the HDMI cable

Signal name	Source	Specification
Clock	MACB	50MHz clock signal in LVDS.
SYNC	MACB	Pulse indicating the clock edge to synchronise the Timestamping counters in all the FEE64 units. In LVDS.
SYNC_Return	FEE64 unit	The SYNC pulse looped back in the FPGA of the FEE64. In LVDS.
ASIC Trigger	FEE64 unit	The logic signal resulting from the four ASIC OR16 signals. In LVDS.
Spare signal	FEE64/MACB	Four single signals for use by Correlation DAQ or other I/O requirements. In LVCMOS33.
Ground	FEE64	All other pins are connected to ground in the FEE64

Port signal allocations for Code 0: Master / Root / Correlation DAQ / Internal Clock

Port	Signal Name	Source/Destination	Comment
1	Clock	From MACB crystal	50Mhz distributed
	SYNC	From Port 1 SYNC Return	
	SYNC_Return	To all SYNC signals	Distributed by MACB routing
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Spare1: Correlation DAQ Clock	To Correlation DAQ Lemo00 and other FEE64	
	Spare2: Correlation DAQ Reset	To Correlation DAQ Lemo00 and other FEE64	
	Spare 3 : Correlation DAQ_reset_request	From Correlation DAQ Lemo 00	Creates Correlation DAQ Reset
	Spare 4: Correlation DAQ Trigger Accept	From Correlation DAQ Lemo 00	Used to read Scaler.
2,3,4	Clock	From MACB crystal	50Mhz distributed
	SYNC	From Port 1 SYNC Return	
	SYNC_Return	Not yet allocated	
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Spare1: Correlation DAQ Clock	From Port 1	
	Spare2: Correlation DAQ Reset	From Port 1	
	Spare 3 : Correlation DAQ_reset_request	Not used	
	Spare 4: Correlation DAQ Trigger Accept	From Correlation DAQ Lemo 00	Used to read Scaler.

Port signal allocations for Code 1: Master / Root / Correlation DAQ / External Clock and SYNC

Port	Signal Name	Source/Destination	Comment
1	Clock	From External SMA	50Mhz distributed
	SYNC	From External SMA	
	SYNC_Return	Not yet allocated	
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Spare1: Correlation DAQ Clock	To Correlation DAQ Lemo00 and other FEE64	
	Spare2: Correlation DAQ Reset	To Correlation DAQ Lemo00 and other FEE64	
	Spare 3 : Correlation DAQ_reset_request	From Correlation DAQ Lemo 00	Creates Correlation DAQ Reset
	Spare 4: Correlation DAQ Trigger Accept	From Correlation DAQ Lemo 00	Used to read Scaler.
2,3,4	Clock	From External SMA	50Mhz distributed
	SYNC	From External SMA	
	SYNC_Return	Not yet allocated	
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Spare1: Correlation DAQ Clock	From Port 1	
	Spare2: Correlation DAQ Reset	From Port 1	
	Spare 3 : Correlation DAQ_reset_request	Not used	
	Spare 4: Correlation DAQ Trigger Accept	From Correlation DAQ Lemo 00	Used to read Scaler.

Port signal allocations for Code 2: Master /Branch / Correlation DAQ / MACB internal clock

Port	Signal Name	Source/Destination	Comment
1	Clock	From Port Next	50Mhz distributed
	SYNC	From Port Next	
	SYNC_Return	To all SYNC signals	Goes through Port Next to Root layer and then back up to all FEE64 cards
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Correlation DAQ Clock	To Port Next and all other FEE64 in this MACB	
	Correlation DAQ Reset	To Port Next and all other FEE64 in this MACB	
	Correlation DAQ_reset_request	From Port Next	Creates Correlation DAQ Reset
	Correlation DAQ Trigger Accept	From Port Next	Used to read Scaler.
2,3,4	Clock	From Port Next	50Mhz distributed
	SYNC	From Port Next	
	SYNC_Return	Not yet allocated	
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Correlation DAQ Clock	From Port 1	
	Correlation DAQ Reset	From Port 1	
	Correlation DAQ_reset_request	Not used	
	Correlation DAQ Trigger Accept	From Port Next	Used to read Scaler.

Port signal allocations for Code 3: Slave /Branch / Correlation DAQ

Port	Signal Name	Source/Destination	Comment
1,2,3,4	Clock	From Port Next	50Mhz distributed
	SYNC	From Port Next	
	SYNC_Return	Not yet allocated	
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Correlation DAQ Clock	From Port Next	
	Correlation DAQ Reset	From Port Next	
	Correlation DAQ_reset_request	Not used	
	Correlation DAQ Trigger Accept	From Port Next	Used to read Scaler.

Port signal allocations for Code 4: Master / Root / Correlation DAQ / External Clock/ Internal SYNC /External Timestamp reset

Port	Signal Name	Source/Destination	Comment
1	Clock	From External SMA	50Mhz distributed
	SYNC	From Port 1 SYNC Return	
	SYNC_Return	To all SYNC signals	Distributed by MACB routing
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Spare1: Correlation DAQ Clock	To Correlation DAQ Lemo00 and other FEE64	
	Spare2: Correlation DAQ Reset	From Correlation DAQ Lemo00	
	Spare 3 : Correlation DAQ_reset_request	From Correlation DAQ Lemo 00	Creates Correlation DAQ Reset
	Spare 4: Correlation DAQ Trigger Accept	From Correlation DAQ Lemo 00	Used to read Scaler.
2,3,4	Clock	From MACB crystal	50Mhz distributed
	SYNC	From Port 1 SYNC Return	
	SYNC_Return	Not yet allocated	
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Spare1: Correlation DAQ Clock	From Port 1	
	Spare2: Correlation DAQ Reset	From Correlation DAQ Lemo 00	
	Spare 3 : Correlation DAQ_reset_request	Not used	
	Spare 4: Correlation DAQ Trigger Accept	From Correlation DAQ Lemo 00	Used to read Scaler.

Port signal allocations for Code 5: Master / Root / Correlation DAQ / External 50Mhz Clock/ Internal SYNC

Port	Signal Name	Source/Destination	Comment
1	Clock	From External SMA	50Mhz distributed
	SYNC	From Port 1 SYNC Return	
	SYNC_Return	To all SYNC signals	Distributed by MACB routing
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Spare1: Correlation DAQ Clock	To Correlation DAQ Lemo00 and other FEE64	
	Spare2: Correlation DAQ Reset	To Correlation DAQ Lemo00 and other FEE64	
	Spare 3 : Correlation DAQ_reset_request	From Correlation DAQ Lemo 00	Creates Correlation DAQ Reset
	Spare 4: Correlation DAQ Trigger Accept	From Correlation DAQ Lemo 00	Used to read Scaler.
2,3,4	Clock	From MACB crystal	50Mhz distributed
	SYNC	From Port 1 SYNC Return	
	SYNC_Return	Not yet allocated	
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Spare1: Correlation DAQ Clock	From Port 1	
	Spare2: Correlation DAQ Reset	From Port 1	
	Spare 3 : Correlation DAQ_reset_request	Not used	
	Spare 4: Correlation DAQ Trigger Accept	From Correlation DAQ Lemo 00	Used to read Scaler.

Port signal allocations for Code 6: Master / Root / Correlation DAQ / External 100Mhz Clock/ Internal SYNC

Port	Signal Name	Source/Destination	Comment
1	Clock	From External SMA & divided by 2	50Mhz distributed
	SYNC	From Port 1 SYNC Return	
	SYNC_Return	To all SYNC signals	Distributed by MACB routing
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Spare1: Correlation DAQ Clock	To Correlation DAQ Lemo00 and other FEE64	
	Spare2: Correlation DAQ Reset	To Correlation DAQ Lemo00 and other FEE64	
	Spare 3 : Correlation DAQ_reset_request	From Correlation DAQ Lemo 00	Creates Correlation DAQ Reset
	Spare 4: Correlation DAQ Trigger Accept	From Correlation DAQ Lemo 00	Used to read Scaler.
2,3,4	Clock	From MACB crystal	50Mhz distributed
	SYNC	From Port 1 SYNC Return	
	SYNC_Return	Not yet allocated	
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Spare1: Correlation DAQ Clock	From Port 1	
	Spare2: Correlation DAQ Reset	From Port 1	
	Spare 3 : Correlation DAQ_reset_request	Not used	
	Spare 4: Correlation DAQ Trigger Accept	From Correlation DAQ Lemo 00	Used to read Scaler.

Port signal allocations for Code 12: Master / Root / Correlation DAQ / External 100Mhz Clock/ External SYNC

Port	Signal Name	Source/Destination	Comment
1	Clock	From External SMA & divided by 2	50Mhz distributed
	SYNC	From External SMA	
	SYNC_Return	To all SYNC signals	Distributed by MACB routing
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Spare1: Correlation DAQ Clock	To Correlation DAQ Lemo00 and other FEE64	
	Spare2: Correlation DAQ Reset	To Correlation DAQ Lemo00 and other FEE64	
	Spare 3 : Correlation DAQ_reset_request	From Correlation DAQ Lemo 00	Creates Correlation DAQ Reset
	Spare 4: Correlation DAQ Trigger Accept	From Correlation DAQ Lemo 00	Used to read Scaler.
2,3,4	Clock	From MACB crystal	50Mhz distributed
	SYNC	From Port 1 SYNC Return	
	SYNC_Return	Not yet allocated	
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Spare1: Correlation DAQ Clock	From Port 1	
	Spare2: Correlation DAQ Reset	From Port 1	
	Spare 3 : Correlation DAQ_reset_request	Not used	
	Spare 4: Correlation DAQ Trigger Accept	From Correlation DAQ Lemo 00	Used to read Scaler.

Port signal allocations for Code 13: Master / Root / Correlation DAQ / External 200Mhz Clock/ External SYNC

Port	Signal Name	Source/Destination	Comment
1	Clock	From External SMA & divided by 4	50Mhz distributed
	SYNC	From External SMA	
	SYNC_Return	To all SYNC signals	Distributed by MACB routing
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Spare1: Correlation DAQ Clock	To Correlation DAQ Lemo00 and other FEE64	
	Spare2: Correlation DAQ Reset	To Correlation DAQ Lemo00 and other FEE64	
	Spare 3 : Correlation DAQ_reset_request	From Correlation DAQ Lemo 00	Creates Correlation DAQ Reset
	Spare 4: Correlation DAQ Trigger Accept	From Correlation DAQ Lemo 00	Used to read Scaler.
2,3,4	Clock	From MACB crystal	50Mhz distributed
	SYNC	From Port 1 SYNC Return	
	SYNC_Return	Not yet allocated	
	ASIC Trigger	To MACB Lemo00 (fast NIM)	
	Spare1: Correlation DAQ Clock	From Port 1	
	Spare2: Correlation DAQ Reset	From Port 1	
	Spare 3 : Correlation DAQ_reset_request	Not used	
	Spare 4: Correlation DAQ Trigger Accept	From Correlation DAQ Lemo 00	Used to read Scaler.

Other settings are used for Commissioning the MACB.

The signal allocations for the HDMI Type C connector are different from the Type A.

Standard Type C pin	HDMI signal name/description	Type A pin
2	TMDS Data2+	1
1	TMDS Data2 shield	2
3	TMDS Data2-	3
5	TMDS Data1+	4
4	TMDS Data1 shield	5
6	TMDS Data1-	6
8	TMDS Data0+	7
7	TMDS Data0 shield	8
9	TMDS Data0-	9
11	TMDS Clock+	10
10	TMDS Clock shield	11
12	TMDS Clock-	12
14	CEC	13
17	Reserved (still need this connection)	14
15	SCL	15
16	SDA	16
13	DDC/CEC ground	17
18	+5v power	18
19	Hot plug detect	19

The following table shows how the signals are allocated in the MACB to the Type C connector.

Standard Type C pin	HDMI signal name/description	Signal name at MACB
2	TMDS Data2+	Clock_p
1	TMDS Data2 shield	ground
3	TMDS Data2-	Clock_n
5	TMDS Data1+	SYNC_p
4	TMDS Data1 shield	ground
6	TMDS Data1-	SYNC_n
8	TMDS Data0+	SYNC_Return_p
7	TMDS Data0 shield	ground
9	TMDS Data0-	SYNC_Return_n
11	TMDS Clock+	ASIC Trigger_p
10	TMDS Clock shield	ground
12	TMDS Clock-	ASIC Trigger_n
14	CEC	Spare_1
17	Reserved (still need this connection)	Spare_2
15	SCL	Spare_3
16	SDA	Spare_4
13	DDC/CEC ground	Ground
18	+5v power	Ground
19	Hot plug detect	Ground