FEE64 system software interface

Firmware Version date 25th May 2016

The interface is basically an addressed area of 32 bit memory containing controls for the data acquisition readout.

All offsets and addresses are 32 bit word oriented. Multiply by 4 to get byte oriented PPC addresses.

Local controls

Base Address : 0x0000

0 : 32 bit register.

Bit 0 controls the tick timer – 5mS fixed interval.
Bit 1 controls the Peak hold reset applied 2uS after tick for 2uS.
Bits 11 => 8: control how many 5mS intervals between resets.
Bit 15: set to ‘1’ to reset Timestamp modules
Bit 16: set to ‘0’ to invert ASIC1 OR16 signal for Fast NIM output.
Bit 17: set to ‘0’ to invert ASIC2 OR16 signal for Fast NIM output.
Bit 18: set to ‘0’ to invert ASIC3 OR16 signal for Fast NIM output.
Bit 19: set to ‘0’ to invert ASIC4 OR16 signal for Fast NIM output.

1 : 32 bit status register

Bit 0 : Lock Detect bit from LMK03200 #1
Bit 1 : Lock Detect bit from LMK03200 #2
Bit 2 : Lock detect from the internal PLL & DCM for the mux clock.

2 : ADC control register . 32 bit register. (current default is all powered off at FPGA load). Boot software enables and calibrates.

Bit 0 : =>’1’ Power down Flash ADC #1.
Bit 1 : =>’1’ Power down Flash ADC #2.
Bit 2 : =>’1’ Power down Flash ADC #3.
Bit 3 : =>’1’ Power down Flash ADC #4.
Bit 4 : =>’1’ Power down Flash ADC #5.
Bit 5 : =>’1’ Power down Flash ADC #6.
Bit 6 : =>’1’ Power down Flash ADC #7.
Bit 7 : =>’1’ Power down Flash ADC #8.

3 : Trigger output control register. 32 bit register.

Bit 3 => 0 : selects logic source.

Code	Logic signal
0	ASIC1_Data_Ready
1	ASIC1_rdo_range AND ASIC1_Data_Ready
2	ASIC2_rdo_range AND ASIC2_Data_Ready
3	Led_trigger(0)
4	OR64

5	Multiplicity Trigger
6	Sync_registered
7	Force_capture
8	ASIC1_OR_16
9	ASIC2_OR_16
10	ASIC3_OR_16
11	ASIC4_OR_16
12	OR of all four ASICs OR16s
13	Led_trigger(1)
14	Logic ‘0’
15	Readout_done(1)

Bit 4: ‘0’ Trigger is logic signal selected by bits 3 to 0. ‘1’ Trigger is internally is logic signal selected by bits 3 to 0 delayed by the number of 100Mhz clocks as defined by the delay register (#6). The pulse is forced to be 4 clocks wide and have a delay of at least 10 clocks between pulses.

4 : Pulser rate register. 32 bit register. → 2uS pulse *(not used in this version)*
Bits 15 => 0 : Rate for pulser. Default is 0x7D0 => 250Hz.

5 : LMK03200 control register. 8 bit register. Default is 0x07.
Bit 0 : SYNC pin on both LMK03200. Active low
Bit 1 : GOE pin on both LMK03200. ‘1’ enables the clock outputs
Bit 2 : MUX_CLK_SEL. ‘1’ selects the internal 50Mhz oscillator.
‘0’ BuTiS clock from the HDMI connector.
Bit 3 : BuTiS clock divider reset. Active low reset of the divider
Bit 4 : BuTiS clock divider select /4. ‘1’ selects divided input clock.
‘0’ bypasses divider.
Bit 5 : Mux clock DCM reset. Set to ‘1’ to reset the DCM if it hasn’t locked

6 : Trigger delay. 32 bit register.
Bits 31 to 0: The number of 10nS clocks to delay the Trigger output.

7 : Correlation interface control register. 4 bit register. Tri-state if bit set to ‘0’. Default is ‘0’/.
Bit 0: enable drive of Correlation Clock
Bit 1: enable drive of Correlation Reset.
Bit 2: enable drive of Correlation Reset Request.
Bit 3: enable drive of Correlation Trigger.

9 : Wave Capture and ADC reset control. 8 bit register. Set back to zero before continuing.
Bit 0: ‘1’ resets the eight Q8 modules (*Q8_simple.vhd)*
Bit 2: ‘1’ resets the Wave form Capture DMA (*wcap_dma.vhd*)
Bit 7: ‘1’ resets the PowerPC.

10 : Firmware Version number as a character string.
All other addresses return the Hexadecimal Firmware Version Code. DDMYVVII
DD = day , M = month, Y = year 0 is 2016 , VV = version code, II = increment number

Temperature measurements

Base address 0x200

Offset	Name	Function	Comment
0	Start0	Initiates **Virtex** temperature measurement	Write to this address starts the conversion.
1	Value0	13 bit signed temperature measurement. Read only.	Bits 0 to 11 <= value (LSB = 0.0625 degrees). Bit 12 <= sign bit
2	Start1	Initiates **PSU** temperature measurement	Write to this address starts the conversion.
3	Value1	13 bit signed temperature measurement. Read only.	Bits 0 to 11 <= value (LSB = 0.0625 degrees). Bit 12 <= sign bit
4	Start2	Initiates **ASIC** temperature measurement	Write to this address starts the conversion.
5	Value2	13 bit signed temperature measurement. Read only.	Bits 0 to 11 <= value (LSB = 0.0625 degrees). Bit 12 <= sign bit
8	Status		Bit 0 => interface busy Bits 1 to 3 => Hold state (should be exclusive) shows the last device selected.

There is one state machine which accesses two MAX6627 devices on the FEE64 and one on the mezzanine.
The access is exclusive. If access is attempted to more than one device at a time then rubbish will result!
The interface should take about 4 to 5 us to complete an access.
The MAX6627 takes 500ms between samples. It is recommended to leave at least this period between samples.

ASIC Readout buffer and controls

Base address 0x300

Offset	Name	Function	Comment
0	Control		Bit 0 <= ‘1’ : Enable readout Bit 14 <= ‘1’ : RDO_reset Bit 16 <= ‘1’ : SYNC readout clock.
1	State machine positions	The state of each of two stages in the readout process	Bits 0-6 : bit_count Bits 8-15 : readout state Bits 16-19 : gather state
2	Status		Bit 1 <= readout busy Bit 3 <= time fifo full bit 4 <= Last Stage Fifo empty bit 5 <= Last Stage Fifo full bit 6 <= Last Stage Fifo prog empty bit 7 <= Last Stage Fifo prog full bit 8 <= start_adc1 bit 9 <= start_adc2 bit 10 <= start_adc3 bit 11 <= start_adc4 bit 12 <= time fifo < 200 bit 13 <= time fifo > 500 bit 14 <= Pause signal bit 28 <= ASIC1 Fifo almost full bit 29 <= ASIC2 Fifo almost full bit 30 <= ASIC3 Fifo almost full bit 31 <= ASIC4 Fifo almost full
4	ASIC readout states	The state of each of the four ASIC readout machines.	Bits 0-4: ASIC1 Bits 8-12: ASIC2 Bits 16-20: ASIC3 Bits 24-28: ASIC4
6	ASIC_resets		Bits 3 => 0 : directly control resets
7	ASIC readout enable	Enable each ASIC readout circuit	Bit 0 <= ‘1’ : Enable ASIC1 Bit 1 <= ‘1’ : Enable ASIC2 Bit 2 <= ‘1’ : Enable ASIC3 Bit 3 <= ‘1’ : Enable ASIC4
8	Source select	Allows a test counter to be routed through the readout paths instead of normal data	Bit 0 : ‘0’ selects normal data and ‘1’ selects a counter
9	ASIC Stamp	Result of SYNC readout clock	Bottom 8 bits of timestamp when SYNC arrives.
12	Waiting counter	Counts the times any ASIC has data and buffers are full	Bits 31 to 0 : number of missed data readies during Pause. Reset by Control register bit 14.
13	Convert delay	The number of clocks to delay the start of ADC conversion	Bits 7 to 0 : Delay in 10nS increments. Default is 700ns.

14	Time fifo data count		Bits 8 to 0 : how many events are pending

ASIC and Info Event format

An Event consists of two 32 bit words in the GREAT event format.

Info Event format Identifier

Identifier	Description	Information field meaning or value
1	Discriminator	Discriminator number (ASIC#, Channel)
2	SYNC pulse received	0
3	Pause in readout	0
4	Resume in readout	0
5	Correlation Scalar bits LSW	Correlation Scalar[15..0]
6	Correlation Scalar bits NSW	Correlation Scalar[31..16]
7	Correlation Scalar bits MSW	Correlation Scalar[47..32]

Correlation scalar status and controls

Base address 0x310

Offset	Name	Function	Comment
0	Control	4 bit register	Bit 0 <= ‘1’ : Enable Correlation function Bit 1 <= ‘1’ : Cause a RESET pulse on the Correlation output. Only if enable true. Reset after use.
1	Missed trigger counter	Counts when a trigger occurs during a pause	Bits 15 to 0 are the number of missed triggers. Set to 0 by reset.
2	Status		Bit 0 <= fifo_empty Bit 1 <= fifo_prog_full Bit 24 to 16 : Number in Fifo
3	Scalar LSbs	Scalar read back	Scalar value from the counter bits 31 to 0
4	Scalar MSbs	Scalar read back	Scalar bits 47 to 32
5	Trigger Delay	Value in 100ns steps to wait from Correlation Trigger to storing the scalar value and the local timestamp	Bits 31 to 0 are the delay value. Recommended to be set to 0x00000100 for a 25.6uS delay . This should be enough for all ADC conversions for a full 64 channel event.
6	Force trigger	Write here forces an Correlation trigger	

Correlation interface stores the value of the scalar after the programmable delay in a 64 deep FIFO
Fast NIM Signals on the MACB front panel are set up for

NIM out 0 : Clock. In Riken this is 25Mhz
NIM out 1 : Reset pulse.
NIM input 2 : Reset Request
NIM Input 3 : Correlation Trigger

Timestamp control

Base address 0x400

Offset	Name	Function	Comment
0	Control	Controls the timestamp	Bit 0 <= '1' enables the timestamp counter Bit 1 <= '1' enables the Corl reset signal to reset both the slave and the Master timestamp counter. Bit 3 <= '1' Resync request
1	Status	Status of the timestamp system	Bit 0 : Resync done
4	Timestamp readback Shadow	LSBs. Write to this register copies the timestamp into a shadow register.	Bits 31 => 0 : Timestamp shadow bits 31 to 0.
5	Timestamp readback shadow	MSBs read only.	Bits 31 => 0 : Timestamp shadow bits 63 to 32.
6	SYNC value	The bottom 18 bits of the counter to be used to check when a SYNC pulse is received and used to load at the same time.	Bits 17=> 0 : Sync value
8	Timestamp load	LSBs. Write to this register loads the counter and sets the value of the bottom 32 bits.	
9	Timestamp load	MSBs. Write to this register loads a register with the top 32 bits ready for loading into the timestamp counter.	
10	Re-sync value	LSBs. Loaded into the timestamp counter when the re-sync pulse is received	The lower 18 bits are not reloaded. They are always set by the sync pulse.
11	Re-sync value	MSBs. Loaded into the timestamp counter when the re-sync pulse is received.	
12	200Mhz DCM controls	Controls the 200Mhz clock	Bit 1 <= '1' reset the 200Mhz DCM used by the Master.
13	200Mhz DCM status	Results from the 200Mhz DCM	Bit 16 : 200Mhz DCM locked if '1'
14	SYNC error counter	Counts if the SYNC doesn't arrive when expected.	Bits 15 to 0

The timestamp is a 64 bit counter running at 100 Mhz.

Master timestamp counter controls

Base address 0x410

Offset	Name	Function	Comment
0	Control	Controls the timestamp	Bit 0 <= '1' enables the Master function and counter Bit 3 <= '1' Resync request
1	Status	Status of the timestamp system	Bit 0 : Resync done Bit 12 to 8 : Resync state machine.
2	Timestamp readback Shadow	LSBs. Write to this register copies the timestamp into a shadow register.	Bits 31 => 0 : Timestamp shadow bits 31 to 0.
3	Timestamp readback shadow	MSBs read only.	Bits 31 => 0 : Timestamp shadow bits 63 to 32.
4	Master SYNC value	The bottom 18 bits of the counter to be used to create the SYNC pulse when this unit is Master	Bits 17=> 0 : Master Sync value. Default = 0xA0
5	Timestamp load	LSBs. Write to this register loads the counter and sets the value of the bottom 32 bits.	
6	Timestamp load	MSBs. Write to this register loads a register with the top 32 bits ready for loading into the timestamp counter.	
7	Re-sync value	LSBs. If this unit is a master then this value is used to generate the re-sync pulse.	
8	Re-sync value	MSBs. If this unit is a master then this value is used to generate the re-sync pulse.	
9	SYNC alignment selection	Allows the output SYNC pulse to be shifted in 25% steps	Bits 1=>0 : Selects the shift percentage.

Discriminators buffer and controls

Base address 0x500

Offset	Name	Function	Comment
0	Control		Bit 0 : Enable Bit 1: => ‘1’ to reset the Multiplicity Trigger logic.
2	Status		Bit 0: Enable
3	Missed discriminator activity counter	Counts when discriminator pattern could not be stored due to Pause	Bits 15 to 0 are the number of missed patterns. Set to 0 by reset
6	Mask_LSW	Disable selected channels	Bits 31 => 0 : ‘1’ Mask channels 1 to 32 for discriminator readout
7	Mask_MSW	Disable selected channels	Bits 31 => 0 : ‘1’ Mask channels 33 to 64 for discriminator readout
8	ASIC 1 Discriminator value	Instantaneous value	Bits 15 => 0 The state of the discriminator signals from the ASIC
9	ASIC 2 Discriminator value	Instantaneous value	Bits 15 => 0 The state of the discriminator signals from the ASIC
10	ASIC 3 Discriminator value	Instantaneous value	Bits 15 => 0 The state of the discriminator signals from the ASIC
11	ASIC 4 Discriminator value	Instantaneous value	Bits 15 => 0 The state of the discriminator signals from the ASIC
12	Multiplicity Trigger Upper Limit	Number of Triggers needs to <= this number.	Bits 6 to 0 : Number of Discriminators.
13	Multiplicity Trigger Lower Limit	Number of Triggers needs to >= this number.	Bits 6 to 0 : Number of Discriminators.
14	Time Window	Number of 10nS clocks the condition must be true before a Trigger is generated	Bits 7 to 0 : Number of clocks for the Time Window.

Use Offset 3 : Trigger output control register setting 5 to connect the Multiplicity Trigger to the MACB Fast NIM output.

ASIC READOUT – DMA control and status

Base address 0x600

Offset	Name	Function	Comment
0	Control		Bit 0 : Start DMA transfers Bit 15 : reset
1	State Machine status		Bits 3:0 dma_st Bits 15 : 8 state_counter
2	Status		Bit 0: Dma_done Bit 1: mst_cmd_busy Bit 2: Burst_fifo_full Bit 3: Burst_fifo_empty Bit 4: dma_error Bit 5: dma_timeout Bit 6: block_low_done Bit 7 : block_high_done Bits 15:8 item_count
3	Start Address	32 bit address in SDRAM of allocated memory. (Bytes)	This must be at a boundary to accommodate the Memory size as the lsbs of the SDRAM address.
4	High Water Mark	Where to flip between High and Low blocks	This value must be less than (Buffer_size/2) -1
5	Block low item counter	Count of the total number of data bytes transferred in the Low block.	
6	Block high item counter	Count of the number of data bytes transferred in the High block.	
7	Flush	A write to bit 0 at this address forces the current block to complete.	Any write forces a Flush.
8	Test counter		The current value of the incrementing test_counter
9	Buffer_size	(Bytes)	The amount of memory available to this DMA channel. The block size = this value /2
10	Source select		Bit 0 : ‘1’ selects test_counter to the data stream
11	Block low taken	Write only	A write to this location clears the Low Done flag and allows the block to be used by the channel
12	Block high taken	Write only	A write to this location clears the High Done flag and allows the block to be used by the channel
13	Waiting	Read only (100Mhz)	Increments if a buffer isn’t available

The memory start address and buffer size values are used to create two equal sized blocks of memory for storing events.
The two blocks are filled on a flip/flop basis with flags to indicate the completion and availability.
The ‘flush’ command will force the flip from one block to the next.

Wave Capture READOUT – DMA control and status

Base address 0x700

Offset	Name	Function	Comment
0	Control		Bit 0 : Start DMA transfers Bit 15 : reset
1	State Machine status		Bits 3:0 dma_st Bits 15 : 8 state_counter
2	Status		Bit 0: Dma_done Bit 1: mst_cmd_busy Bit 2: Burst_fifo_full Bit 3: Burst_fifo_empty Bit 4: dma_error Bit 5: dma_timeout Bit 6: block_low_done Bit 7 : block_high_done Bits 15:8 item_count
3	Start Address	32 bit address in SDRAM of allocated memory. (Bytes)	This must be at a boundary to accommodate the Memory size as the lsbs of the SDRAM address.
4	High Water Mark	Where to flip between High and Low blocks	This value must be less than (Buffer_size/2) -1
5	Block low item counter	Count of the total number of data bytes transferred in the Low block.	
6	Block high item counter	Count of the number of data bytes transferred in the High block.	
7	Flush Request	Finish the current DMA and flip to the next buffer	Any Write to this address will cause a flush.
8	Test counter		The current value of the incrementing test_counter
9	Buffer_size	(Bytes)	The amount of memory available to this DMA channel. The block size = this value /2
10	Source select		Bit 0 : '1' selects test_counter to the data stream
11	Block low taken	Write only	A write to this location clears the Low Done flag and allows the block to be used by the channel
12	Block high taken	Write only	A write to this location clears the High Done flag and allows the block to be used by the channel

The memory start address and buffer size values are used to create two equal sized blocks of memory for storing events.

The two blocks are filled on a flip/flop basis with flags to indicate the completion and availability.

FADC interface align and control

Base address 0x800 *ADCs are currently aligned at boot time.*

Offset	Name	Function	Comment
0	Control	Controls the ADC serial alignment	Bit 0 : Set to '1' to start Alignment: bitAlignGo Bit 3: Set to enable the DCMs
2	Bit Align Done	Status of the bit alignment	Bits 0-7 : Bit alignment done for each chip when set.
3	Chip status		Bit 0 : Chip Align Done Bit 1: Clk50-Clk175 locked Bit 2 : Clk200 locked Bit 4 to 7 : IDELAYCTRL readies.
4	Word Align Status		Bit0-7 : Word Align Done for each of the eight ADC chips

Carry out the following to all the ADCs to start the pattern generation for alignment.

Offset in ADC	Value	Comment
0x19	0x80	Load User pattern
0x1A	0x3F	
0x1B	0x80	
0x1C	0x3F	
0x0D	0x48	Set the mode to output the user pattern
0xFF	0x01	Load the values to the ADC registers

LED controls

Base address 0x900

Offset	Name	Function	Comment
0	ASIC1	LED controls	Bit 0-15: Threshold Bit 16: Polarity
1	LED enable ASIC1	A bit for each LED	Bit 0-15: Enable Channel # for waveform capture.
2	ASIC2	LED controls	Bit 0-15 : Threshold Bit 16 : Polarity
3	LED enable ASIC2	A bit for each LED	Bit 0-15: Enable Channel # for waveform capture.
4	ASIC3	LED controls	Bit 0-15 : Threshold Bit 16 : Polarity
5	LED enable ASIC3	A bit for each LED	Bit 0-15: Enable Channel # for waveform capture.
6	ASIC4	LED controls	Bit 0-15 : Threshold Bit 16 : Polarity
7	LED enable ASIC4	A bit for each LED	Bit 0-15: Enable Channel # for waveform capture.
8	Capture Size	Number of samples stored	Bit 0-9 : Number of samples
9	Pre-Trigger Size	Number of samples stored before the trigger	Bit 0-9 : Number of samples stored before the trigger
10	Force capture	Forces all enabled channels to collect a waveform	Bit 0: Force waveform capture on write ‘0’ to ‘1’
11	Sample Rate	Number of clocks between samples	Bits 0-15: used in a counter counting down to 0. When 0 a sample is stored.
12	Stop Triggers	Stops the generation of Wave form Triggers	Bit 0 => ‘1’ to Stop

Polarity :- ‘0’ => Positive ; ‘1’ => Negative.

Threshold is the ADC value bear in mind 0 level is 8192 so +1 is 8193.
The logic is :-

For Positive polarity (positive going edge) a trigger is generated if the Difference is greater than the threshold.

For Negative polarity (negative going edge) a trigger is generated if the Difference is less than the threshold.

Trace post capture maths controls

Base address 0x910

Offset	Name	Function	Comment
0	B_Samples	Number of samples for the baseline calculation	Bit 0-9: Only powers of 2 acceptable. So 2,4,8,16,32,64,128 etc. This is due to simple shifter division. Should be set less than the pre-trigger value.
1	Delay Length	Number of samples to delay the input for the CFD	Bits 0-3 : the number of samples to delay the input for the CFD.
2	Threshold	Threshold for CFD	Bits 0 – 15 : Two's complement value
3	Fraction	CFD multiplier	Bits 0 – 7 : fraction value for the cfd. Bit 7 => 0.5 Bit 6 => 0.25 ... etc. So 0xC0 = 0.75.

Two 14 bit data words are overwritten by the CFD results at the last two entries of the trace data.
First is the integer offset of the zero crossing from the trace data timestamp.
Second is the vernier in bits 7:0 and a flag in bit 13 to indicate the CFD was successful.

Waveform capture Readout controls

Base address 0xA00 *(Q8_transfer_simple.vhd)*

Offset	Name	Function	Comment
0	Control		Bit 0 <= ‘1’ : Enable readout Bit 7 <= ‘1’ : local reset of State machines and FIFOs
1	State machine positions		Bits 0-3 : transfer state machine Bits 22 – 16 : Scanner value
2	Status		Bit 0 <= ‘0’ Bit 1 <= readout busy Bit 2 <= ‘0’ Bit 3 <= time fifo full bit 4 <= Last Stage Fifo empty bit 5 <= Last Stage Fifo full bit 6 <= ‘0’ bit 7 <= Last Stage Fifo prog full bit 8 <= ‘0’ bit 9 <= ‘0’ bit 10 <= ‘0’ bit 11 <= ‘0’ bit 12 <= time fifo < 200 bit 13 <= time fifo > 500 bit 14 <= Pause signal bits 23 – 16 : Q8_Ready bit 31 <= ev_actives(scanner)
3	Test counter		Bits 17 => 0 : Number of writes to the last stage fifo.
4	Icc counter	The number of incorrect channel numbers	Bits 0 - 15: icc counter
5	Ev_actives	A channel has data for this timestamp	Bits 31 to 0 : Channels 31 to 0 ASIC 1 and 2
6	Ev_actives	A channel has data for this timestamp	Bits 31 to 0 : Channels 63 to 32 ASIC 3 and 4
8	Source select	Allows a test counter to be routed through the readout paths instead of normal data	Bit 0 : ‘0’ selects normal data and ‘1’ selects a counter
9	Info counter	Increments when an Info data item is output	Bits 15 to 0
14	Time fifo data count		Bits 8 to 0 : how many events are pending
15	Last stage data count	How many 128 bit words are in this fifo	Bits 7 to 0

The Enable is set to operate the waveform capture. All other registers are diagnostic.

ASIC1 controls

Base Address 0x4000

Offset	Title	Default	Register bits
0	preamp reset	5'b00100, 4	S[4:0]
1	shaper reset	5'b00101, 5	S[9:5]
2	filter reset	5'b00110, 6	S[14:10]
3	fast filter reset	5'b00010, 2	S[19:15]
4	peak hold reset	5'b00111, 7	S[24:20]
5	clamp reset	5'b01000 ,8	S[29:25]
6	comparator reset	5'b01001, 9	S[34:30]
7	hold timing	4'b0100, 4	S[38:35]
8	low_ref (pre-amp polarity)	1'b0 ,0	S[39]
9	shaping time 4u,2u,1u,0.5u	4'b0011, 3	S[43:40]
10	MEC (medium/low energy selection)	1'b0, 0	S[44]
11	clamp threshold 1V=0100, 2.4V=1101	4'b0100, 4	S[48:45]
12	slow comparator threshold (LEC/MEC) 0.102V	8'b00001111, 0x0F	S[56:49]
13	shaper reference 0.945V=001110100 2.376V=11010011	8'b00110100, 0x34	S[64:57]
14	fast comparator threshold HEC 0.102V	8'b00001111, 0x0F	S[72:65]
15	fast comparator threshold LEC/MEC 0.102V	8'b00001111, 0x0F	S[80:73]
16	vcasc_n for buffers 1.284V	8'b11010010, 0xD2	S[88:81]
17	vcasc_p for buffers 2.071V	8'b10000000, 0x80	S[96:89]
18	preAmp ref 0.198V=00010110 1.602V=10110010	8'b10110010, 0xB2	S[104:97]
19	biasRC preamp HEC 0.828V	8'b01011100, 0x5C	S[112:105]
20	vcasc_preamp_HEC 0.936V	8'b01101000, 0x68	S[120:113]
21	Ibias LF feedback 10uA	4'b1000 , 8	S[124:121]
22	biasRC preamp LEC 0.828V	8'b01011100, 0x5C	S[132:125]
23	Ibias preamp SF 5mA	4'b1000, 8	S[136:133]
24	vcasc_preamp LEC 0.936V	8'b01101000, 0x68	S[144:137]
25	Ibias preamp 1.112mA	4'b1000, 8	S[148:145]
26	diode link threshold 0.18V=00010100 1.53V=10101010	8'b11001010, 0xCA	S[156:149]
27	Unused	3’b000, 0	S[159:157]
28	Write to this address causes the ASIC to be loaded		
29	Status of the load. Bit 0 : loading busy Bit 1 : value of the ASIC shift_out signal		

	Bits 20 : 16 Fixed at '11111' for legacy software.		

The chip layout actually has 160 bits for the register, with the Serial_Out connected to the 160th bit, S[159]. Bits S[158:157] are unconnected. I recommend clocking the register fully (160 positive clock edges in sequence) so that all the bits are defined. If the load sequence is then repeated, the Serial_Out will have the same bit sequence as Serial_In. This is a good check that the clocking is working.

Note that the control register is loaded from Serial_In in reverse order. The first positive Serial_Clock edge loads Serial_In onto register bit S[0], and this bit then propagates through the register step by step. After the 160th clock edge, the first Serial_In bit has become S[159], the second Serial_In is S[158] etc. It is best to allow >10ns between changing the Serial_In and applying the positive clock edge, just in case there are timing delays on chip. The negative clock edges have no effect, so their timing is not important.

For checking the operation of the shift registers, and the presence of an ASIC, the 160 bit register to be sent to the ASIC is copied as 5 x 32 bit words. The data shifted back into the FPGA is presented in the same format. Note: To check the ASIC operate the load twice to ensure the new contents of the control register in the ASIC are re-loaded.

Offset	Register name	Comment
32	ASIC control register copy. Read only	[31:0]
33	ASIC control register copy. Read only	[63:32]
34	ASIC control register copy. Read only	[95:64]
35	ASIC control register copy. Read only	[127:96]
36	ASIC control register copy. Read only	[159:128]
40	ASIC control register returned. Read only	[31:0]
41	ASIC control register returned. Read only	[63:32]
42	ASIC control register returned. Read only	[95:64]
43	ASIC control register returned. Read only	[127:96]
44	ASIC control register returned. Read only	[159:128]

ASIC2 controls

Base Address 0x4040

ASIC3 controls

Base Address 0x4080

ASIC4 controls

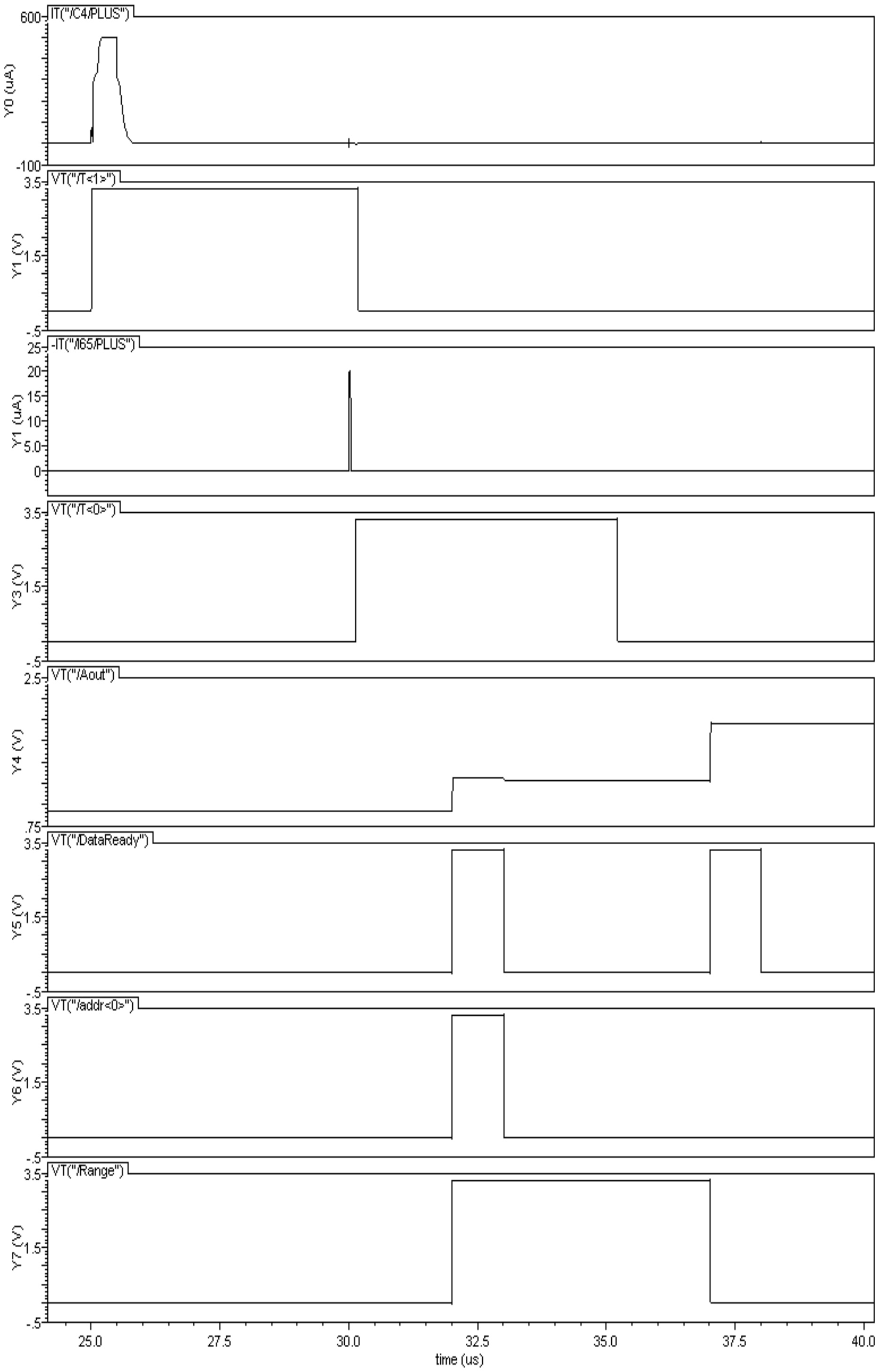
Base Address 0x40C0

Map of the monitor points to channels on the Logic Analyser

The monitor connector on the underside of the FEE64 card is designed to have the plastic carrier for the “soft-touch” probe soldered in place. This then allows the probe to be connected.
There are 13 signals available for the logic analyser.
These signals are allocated in the top level of the VHDL and will vary according to the version in use.

Monitor signal number	FPGA pin	ODD-Pod bit number	Comments
0	E31	D0	
1	F31	D2	
2	F30	D4	
3	AA30	D5	
4	G30	D6	
5	AC29	D7	
6	AD29	D8	
7	AD30	D9	
8	AE29	D10	
9	AF30	D11	
10	AF31	D12	
11	AJ31	D14	
12	AK31	D15	

Example waveforms for mux output of two channels (high energy and low energy)



Large current pulse on channel 1

Trigger output 1

Small current pulse on channel 0

Trigger output 0

Analogue mux output, connected to channel 1 output from t=32 to 33us, channel 0 from t=37 to 38us.

Data ready – mux output valid from 32-33us and 37-38us (clock period is 1us)

Address<0> high from 32-33us (channel 1), low from 37-38us (channel 0)

Range high from 32-33us (high energy range on channel 1), low from 37-38us (low energy on channel 0)

The analogue mux settling time is roughly 100ns (ignoring the external amplifier). These waveforms are applicable for clock rates in the range ~0.5M – 2MHz approx. 1MHz is the standard rate for simulation purposes – the clock runs continuously. All external waveform transitions occur on positive clock edges.