Report on TAMU experience and things to do as a result

Dates : 15th May to 21st May 2010 at the Cyclotron Institute in Texas A&M University College Station.

The equipment was installed by TD and only required minor changes before first power on. The FEE64 module (B4:06) was air cooled by a large (12") fan operating continuously. There were three aluminium heat sinks on the top of the FEE. The Mezzanine copper block had a heat sink with operating fan. Throughout the week there were no problems with temperature. All stayed below 50. The FPGA got hottest when operating the FADC chips, 48.

Power supply for the FEE was two switch mode programmable power supplies from TTi. They were responsible for 70khz noise. Two Agilent 6653A linear supplies were rented locally and these replaced the switch modes. Noise was reduced but only a small change in fwhm was observed. 98 => 68. The switch mode supply used for -5v failed in power cycling.

The control TCL was changed to include the readout state machine reset before the acquisition software was started. This reduced the number of times the readout state machines became clogged and stopped.

To help with the investigations of the effect of a low energy pulse after a high energy pulse the clock box was connected and an output from the "trigger" FAST NIM LEMO socket generated after a programmable delay to trigger the PB4 pulser connected to the interface card test input. This was successful. A double peak was observed when the delay was less than 10mS from the high energy signal. The start of the delay could be from a number of software selectable sources. Just the ASIC data ready of ASIC1 was used to setup the NIM. Then the data ready in coincidence with the range bit being true.

The ASIC readout state machines were found to have a "deadly embrace" situation where a state could be waiting for a flag that could never be set true. A new version of the FPGA code was developed to include a watchdog feature. A chipscope logic analyser was included in this design to allow the situation to be captured when the watchdog fired. This system worked well and uncovered another fault. It was possible for the ADC conversion to be associated with the wrong channel number due to a break in the pipeline handshake system. An attempt was made to correct this and a counter put in place to monitor the action should it occur. During a subsequent overnight run the counter stayed at 0.

It turns out that the ASIC 4 doesn't have an ADC due to an accident while at Daresbury. Thus the readout would stop when ASIC4 was used. This occurred during high energy calibration when it was impossible to disable the readout sequence for the ASIC4. This took a while to realise and caused some wasted effort!

Things to do and discuss.

- Power supply re-think – Linear or Switch mode
- Investigate maximum allowable temperature for the FPGA.
- Readout of ASICS sequence of handshake to stop the slip of data relative to the channel number
- Change the test input system and investigate the problems with saturated inputs feeding back into the test network.
- Why does location 0 in the internal peripheral get cleared at power-up.
- FADC triggering – more complex options perhaps using a chipscope ILA as the source.
- FADC channel to ASIC input mapping needs to be investigated for clarity.
- HEC + delayed pulser – why are there 2+ peaks from the pulser in rthe LEC range. Why do they go if the delay is >10mS.
- Design the earthing structure into the mechanics.
- Transfer the modified TCL from the server to the NPG systems.
- Investigate and propose solutions for the apparent effect of different routing of the buffered preamp outputs having different noise performance. Perhaps change the relative position of the buffers and ADCs.
- Why does the FADC signal range not cover the full ASIC output swing.
- Why does the discriminator readout system stop working at high rates.
- What is the true maximum specified input rate for the system.
- Send the broken TTi power supply back for repair.
- Investigate the Ethernet differential operating speeds problem
- Re-try the water cooling. Also with two modules in place and powered up.
- Try out the effect of an isolating transformer as a method of noise reduction in conjunction with Linear and Switch mode supplies.

Incorporate changes required by new requests (copied from FEE64 revisionA document) .

1. Incorporate -5v analog bias using DC-DC and linear regulators (-5v at 2.5A min)
2. Change Mux readout adc to incorporate sliding scale.
3. Change Mux readout adc to run at 2Msps or possibly AD7982 a an 18 bit at 1Msps.

4. Change HDMI connector to be type ‘B’/’C’ for mechanical fit.
5. Add logic outputs for monitoring?
6. Re-route the preamplifier outputs from the mezzanine connectors to the ADC buffers and change the relative position of the ADCs and buffers. (needs another prototype.)

Problems that must be solved and tests that must be done before production.

- Power supply re-think – Linear or Switch mode
- Investigate and propose solutions for the apparent effect of different routing of the buffered preamp outputs having different noise performance. Perhaps change the relative position of the buffers and ADCs.
- Why does the FADC signal range not cover the full ASIC output swing.
- Investigate the different Ethernet operating speeds problem. Why do some boards not respond to requests/load LINUX at the same rate as others.
- Re-try the water cooling. Also with two modules in place and powered up. Check for noise performance and cooling ability.
- Try out the effect of an isolating transformer as a method of noise reduction in conjunction with Linear and Switch mode supplies.
- Test the operation of all 64 FADC channels and their affect on the ASIC multiplex readout.
- Estimate the % occupation of the FPGA with MWD to decide if the larger Virtex5 is needed.