Readout Module for Gassiplex ASIC used in Prisma SED.

The Prisma secondary electron detector (SED) is readout by a multi wire proportional counter (MWPC). The number of wires is based on a spacing of 1mm. The prototype detector will measure 4x8cm or 8x8cm, requiring a maximum of 160 channels of readout.
It is proposed to instrument each wire with a 16 channel ASIC where each channel contains a pre-amp, a switchable filter, a shaping amp, and a track and hold circuit. The purpose of this is to reduce the number of connections between the data acquisition (DAQ) electronics and the detector passing through the vacuum and gas interfaces. The outputs of the ASIC are readout sequentially as analogue values to a remote ADC under control of the DAQ when a detector trigger occurs. The data are then forwarded with information related to the event that caused the trigger, either an event number or a timestamp, to a data storage device or event processing system.

The proposed ASIC to be used for the prototype is the Gassiplex0.7-3 chip designed for use in CERN. This is a 16 channel device with the following attributes.
Input range : 290 fC. (if leakage current is greater than 1nA use AC coupling)
Shaping Amplifier : Peaking time 1.2us with 120K feedback resistor. Returns to baseline after 5 us.
Track and hold window:
Hold time:
Clock rate: 2Mhz (500ns).
Analogue output drive: 0 to 2V
Test pulse injection via a 1pF internal capacitor, and analog switch .
Control signals: Readout Clock in , Test Pulse, Test channel clock, Test channel clear, Reset, Track/Hold, Filter

The Prisma SED requirement is summarised as :
Readout at a rate of 10khz per wire:
Charge range:
Number of bits of accuracy:
Percentage deadtime of the detector:

The proposed readout module will reside in VME for ease of interfacing with existing systems at Manchester University, and LNL. MIDAS software will be used for data storage, and device control.

The board will contain interfaces to control four ASICS. An FPGA will carry out the readout sequence for each ASIC in parallel when an external trigger is provided.
A functional block diagram of one interface is included at Fig 1.0.

An interface to an external clock will be implemented to allow synchronization with other DAQ by means of event numbers, or timestamps.

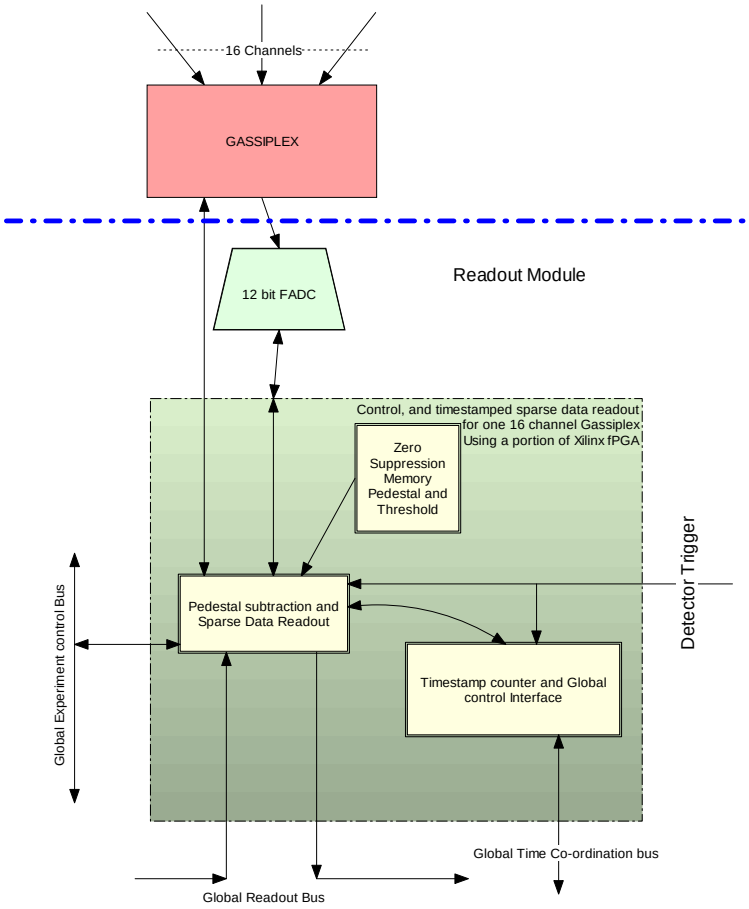

Fig 1.0 Functional diagram of the proposed readout.