Digitiser Segment ADC card functional test

1 Prior to Power up

1.1 Visual Inspection

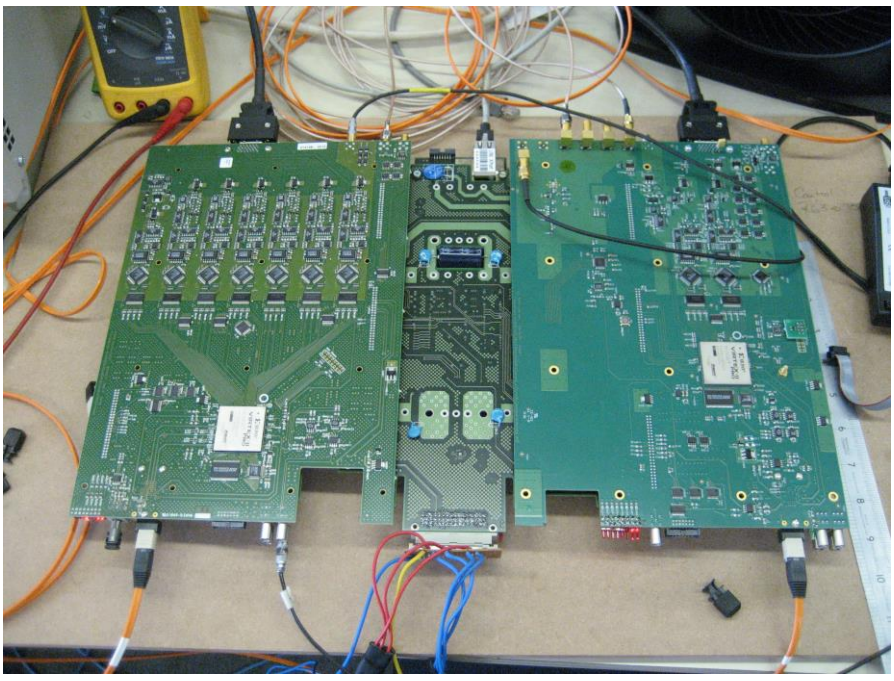
Check for all components in place, mechanical alignment of LEMO and SMA sockets. Basically give the board a good look for anything odd !
Open a Wordpad document and save it as
AGATA_Digitiser_Database\Segment_ADC_cards\Segment_<serial number>\Log.txt
Enter the serial number as the first line and record and save the test results from the following sections. Record each test result on a separate line.

1.2 Resistance across power rails

Open a copy of the Excel 2003 spreadsheet *Segment_voltages* from the *AGATA_Digitiser_Database\Test_Scripts\Segment* directory. Fill in the serial number and save into the database as
AGATA_Digitiser_Database\Segment_ADC_cards\Segment_<serial number>\Segment_voltages.xls
Using the Voltage measuring point drawing as a guide, record all the resistance to ground values in the spreadsheet. Save the spreadsheet

1.3 Install on power supply board.

Install on the test power supply board and check the sockets line up correctly.



2 Power up and program load

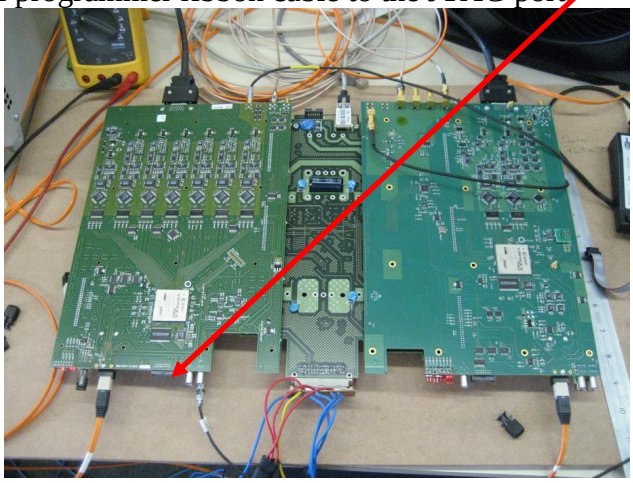
Switch on the bench power supply and check the current for the +12volts is about 4.

2.1 Power supply voltages

Using the measuring point drawing as a guide, record all the voltages in the Excel spreadsheet.
Check the warnings column and investigate any measurements that don't report "OK"
If all reports OK – Save the spreadsheet.

2.2 Program the FPGA proms

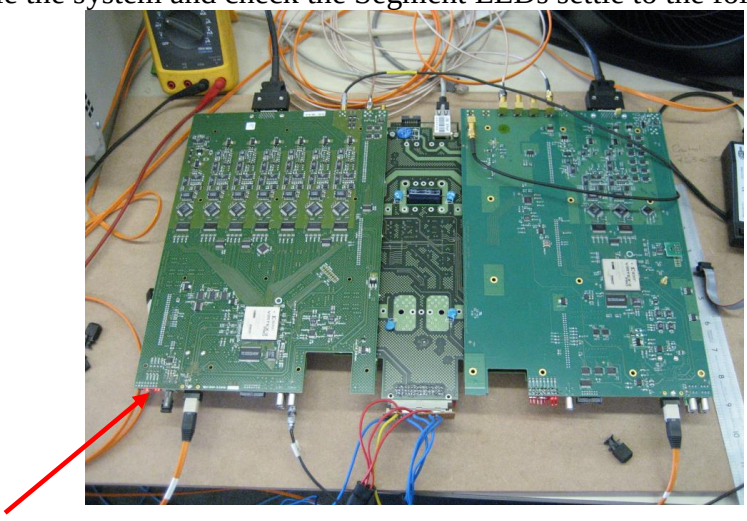
Connect the Xilinx programmer ribbon cable to the JTAG port.



Open Impact (Xilinx programming software) and launch the wizard to check the JTAG chain. In Impact open the Segment.ipf file to setup the programming environment.
Program the three proms.

3 Clock reception and distribution

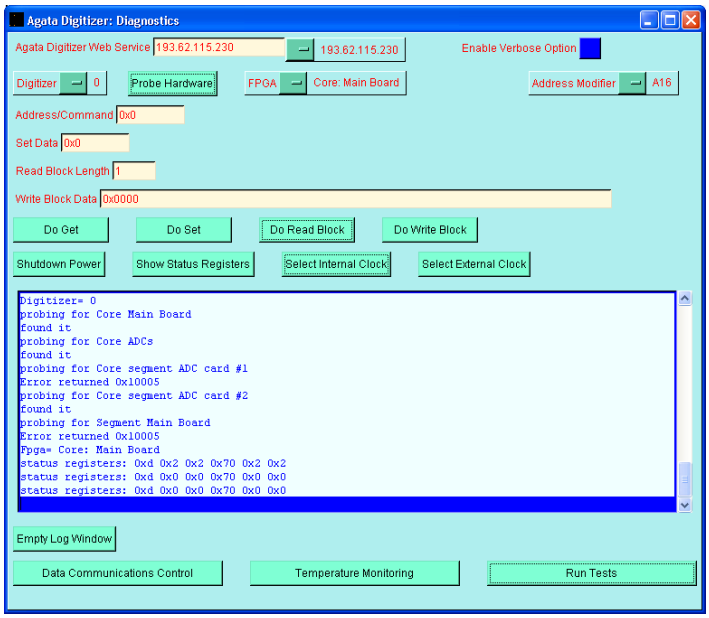
Connect the clock from the Core module using the SMA cable.
Power cycle the system and check the Segment LEDs settle to the following state:



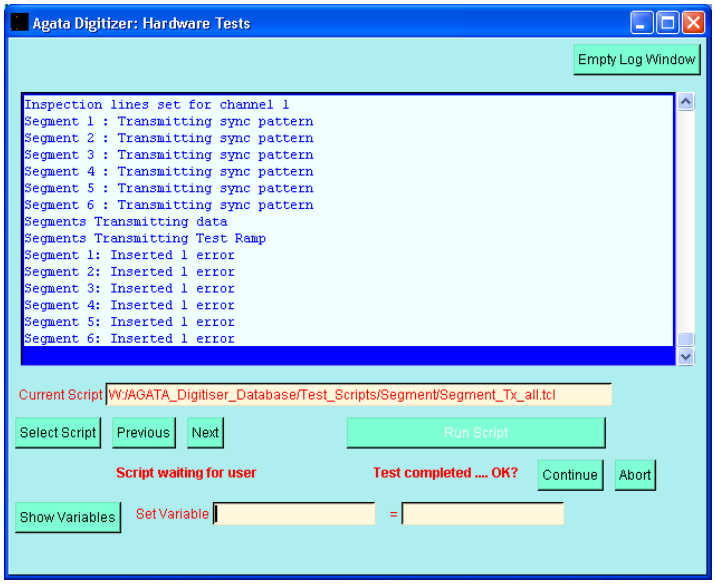
0	1	2	3	4	5	6	7
Off	Off	Off	Counting			On	On

4 Slow control interface and registers

In the MIDAS Diagnostics window for Digitisers select the IP code for the Digitiser from the pull down menu.
Use “Probe Hardware” button to connect until successful.
Use the “Run Tests” button to open the Hardware Tests window.



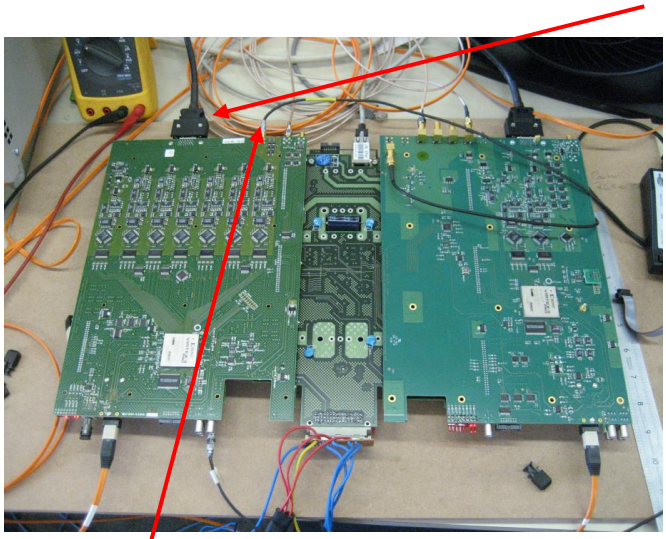
In the MIDAS “Hardware Tests” window select and run the *Core_init.tcl* script to connect the Core optical system to the V2Pro test system and selects to distribute this Global clock. Answer the prompts until the script completes.



Select and run the *Segment_init.tcl* script which checks communication with the segment module using a bit test with register 2 and changes the state of LED 7.

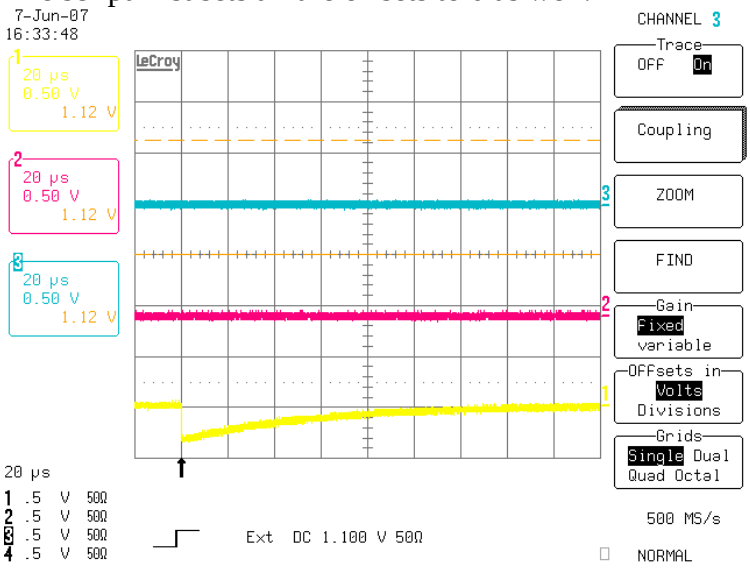
5 Analog Inspection signals

Connect the cable between the Segment test board and the input to the module.



Connect the Analogue inspection signal to a ‘scope with source pulse input to a second channel.
Connect the pulse signal to the analogue input on the Segment test board and run the *Segment_Inspection.tcl* script. Follow the instructions to step through the analog inspection signals checking the ‘scope output for each one.

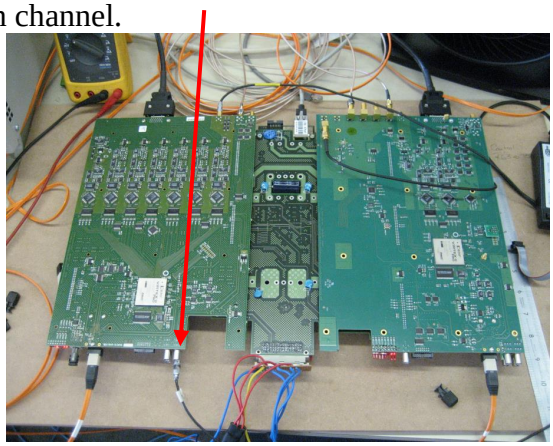
The script first sets all the offsets to 0 as well.



Channel 1 is the Analogue Inspection signal

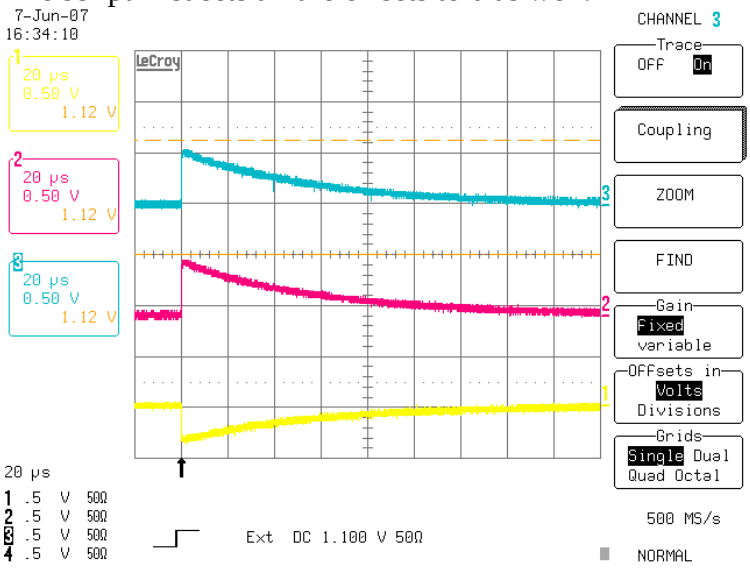
6 Convertors, Offset DACs and Digital inspection

Connect the cable between the Segment test board and the input to the module. Connect the Analogue and two Digital inspection signals to a ‘scope with source pulse input to a fourth channel.



Connect the pulse signal to the analogue input on the Segment test board and run the *Segment_Digital_Inspection.tcl* script. Step through the analog and digital inspection signals checking the ‘scope output for each one. The script also switches the Gain setting for each channel.

The script first sets all the offsets to 0 as well.



Channel 1 is the Analogue Inspection signal
Channel 2 is the DAC inspection line 1
Channel 3 is the DAC inspection line 2

Disconnect the input cable.

Run the *Segment_Offset.tcl* script to exercise each of the Offset DACs in turn. Use the ‘scope channels set up for the Inspection lines in the previous test to verify the function of the DACs. The script enables a VHDL routine which writes a sequence of numbers to make a ramp.

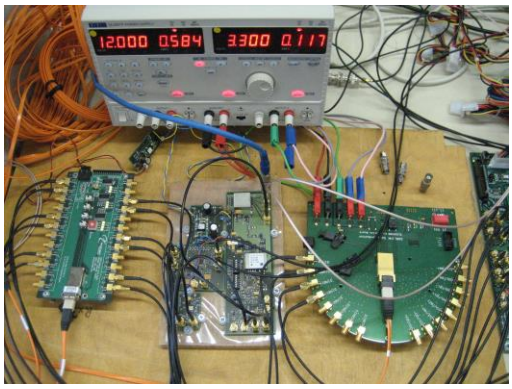
7 RAM

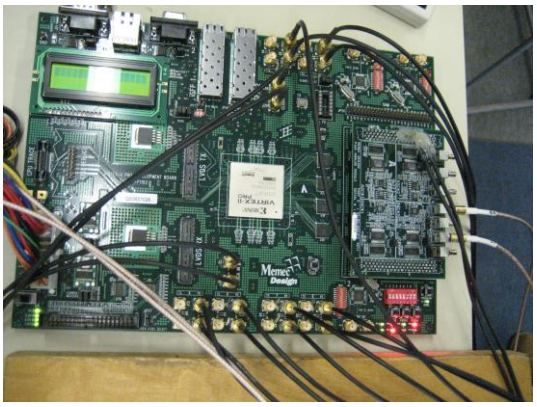
Run the RAM test script. *Segment_ram_test.tcl*

8 From input to V2Pro DAC

Power down the system and install the ZL60101 12 way optical transmitter. Power up the system, Probe Hardware and run the script *Core_init.tcl* as for test 4.
Connect the fibre test box to the transmitter output port and the test system input fibre to channel 1 on the box. (Here shown connected to channel 6)

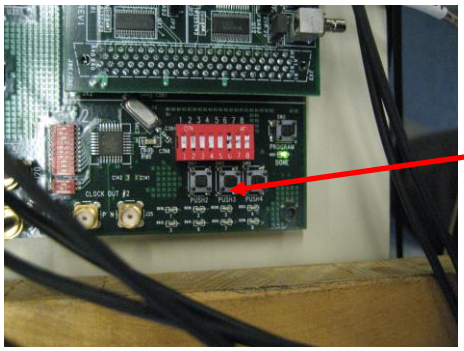
Connect the test system DAC1 output to the ‘scope.



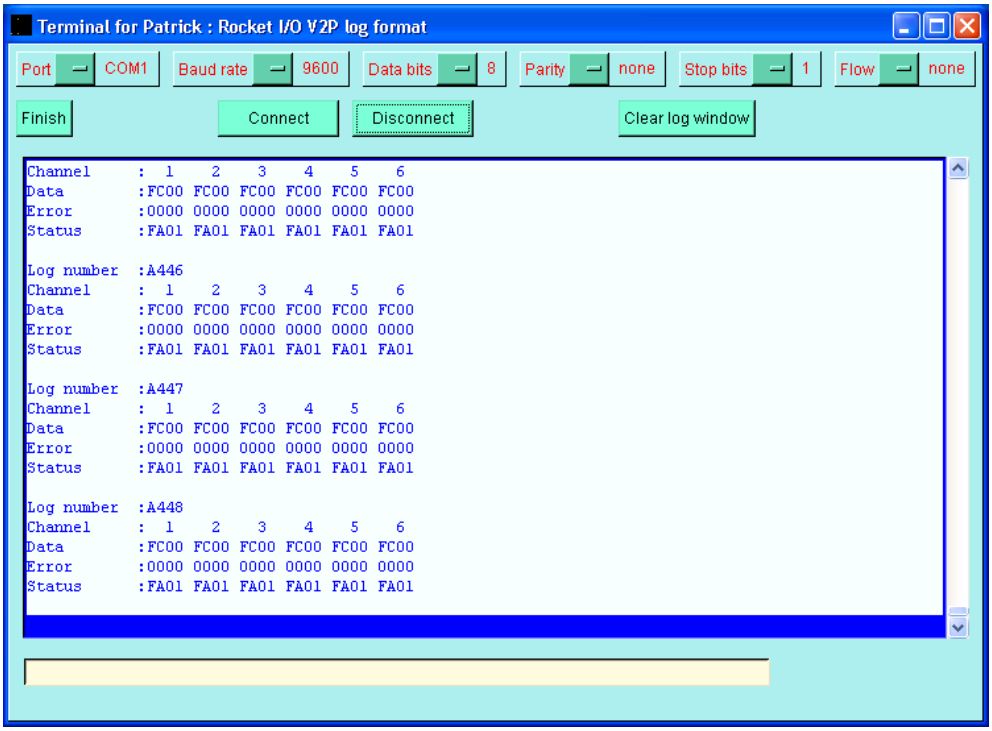


Check the test system switches are set :-

1	2	3	4	5	6	7	8
ON	ON	ON	ON	OFF	ON	ON	ON

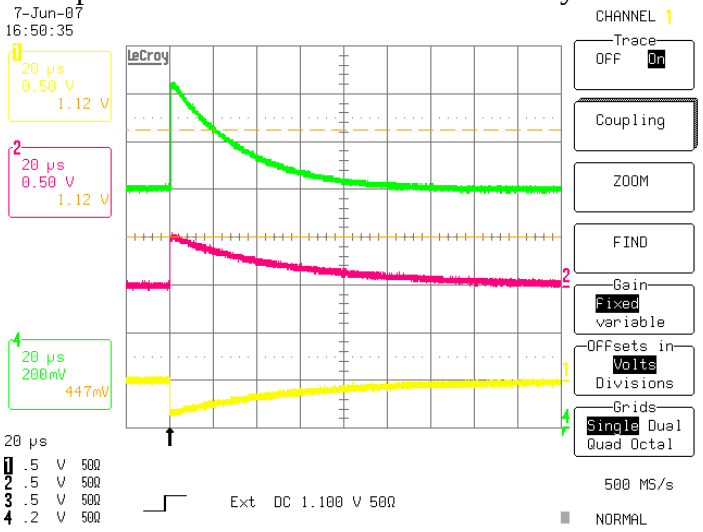


This setting is for synchronization and printing the log.
(Hint : if the output of the test system DAC is not working try and reset the V2P clocks using switch 6 and push button 3)
Connect another two ‘scope channels to the Segment DAC Inspection lines. Open the MIDAS terminal and connect it to COM1 using the buttons at the top.



This test uses only Channel 1 of the optical receiver. The data and status reposrting is only relevant for this channel. The error counter has no meaning for this test.

Run the script *Segment_init_Transmit_1_by_1.tcl* and follow the instructions to see the input waveform transmitted to the test system and shown on the ‘scope.



Channel 1 is the Analogue Inspection signal
Channel 2 is the DAC inspection line 1
Channel 4 is the DAC on the test system.

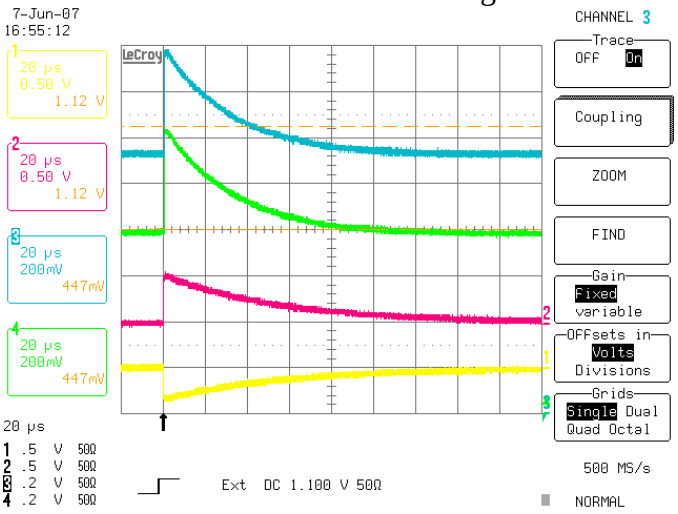
9 Spare channel

Connect as for test 8.
Run the script *Segment_Spare_Tx_1_by_1.tcl* . This steps through the 6 channels replacing each in turn by the spare. Each time the spare channel offset is changed to prove the signals are truly passing through the spare ADC. Follow the same sequence with the optical coupling to check the path from the input channel to the optical receiver.

10 Optical integrity

Connect the 12way ribbon cable between the Segment board and the test system.
Run the script *Segment_Tx_all.tcl* .
Check the terminal for the output to show all six channels transmitting alignment data patterns successfully. Data should be FC00. Status should be #A01 where # is allowed to be any value.

Press “Continue” to transmit the data on all six channels, check the scope for channel 1 and 2 data from the test system DACs and the terminal for changing data on all six channels. The status words should all remain stable. That is they should report 0x#000 where the # nibble is allowed to change.



Channel 1 is the Analogue Inspection signal
Channel 2 is the DAC inspection line 1
Channel 4 is the DAC A on the test system.
Channel 3 is the DAC B on the test system.

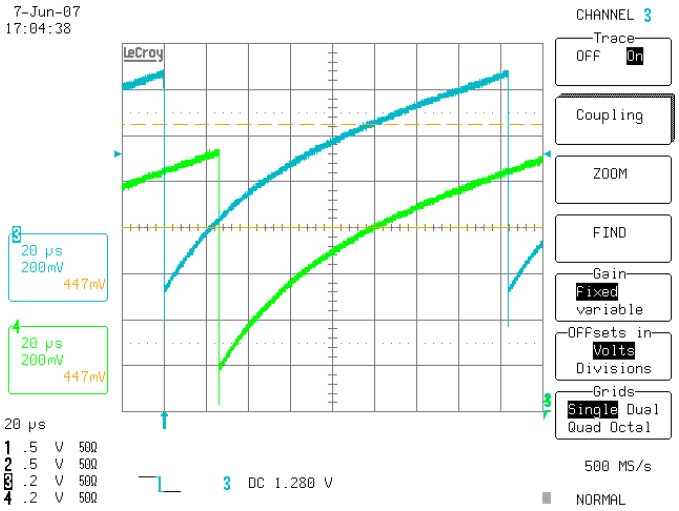
Press “Continue” to transmit the test ramp on all six channels, check the scope for channel 1 and 2 data from the test system DACs and the terminal for changing data on all six channels. The status words should all remain stable. That is they should report 0x#000 where the # nibble is allowed to change.
The data on the scope and on the terminal should remain locked in step. Check the selection of “external clock” has been made correctly to ensure both ends are using the same clock.

Set the test system switches to :-

1	2	3	4	5	6	7	8
OFF	OFF	OFF	OFF	OFF	ON	ON	ON

Press PUSH3 to load the new settings.

This setting is for checking the test ramp data and printing the log.



Channel 4 is the DAC A on the test system.
Channel 3 is the DAC B on the test system.

Press “continue” to insert an error into each of the channels in turn. Check only 1 error is seen at the receiver for each channel in turn. One error is reported at the start of the test as the receiver picks up the place in the ramp.
Leave this test running for 10 minutes and ensure no extra errors are reported.

11 Optical spare connections and offset control receiver.

Connect up as for test 10.
The six optical links that are not used for transmitting ADC data are used for 4 digital signals and 2 Rocket I/O signals.
The digital signals are connected to the Laser spares test box and can be monitored on a scope.
Run the script *Segment_laser_spares.tcl* and check the signals on the scope.
Check channel 1 is the same as the LI1 signal at 25Mhz.
Channel 2 is 12.5Mhz
Channel 3 is 6.25Mhz
Channel 4 is 3.125Mhz

Connect the offset control transmitter to the receiver input on the segment board.
Connect the signal driving the transmitter to the scope and check the signal is copied on LI2 with a delay of ??ms due to the length of the fibre optic cable.

Check the two spare rocket I/O connections are showing status aligned and data is 0xFC00.
Continue the script to transmit data 0xF00D with status aligned.

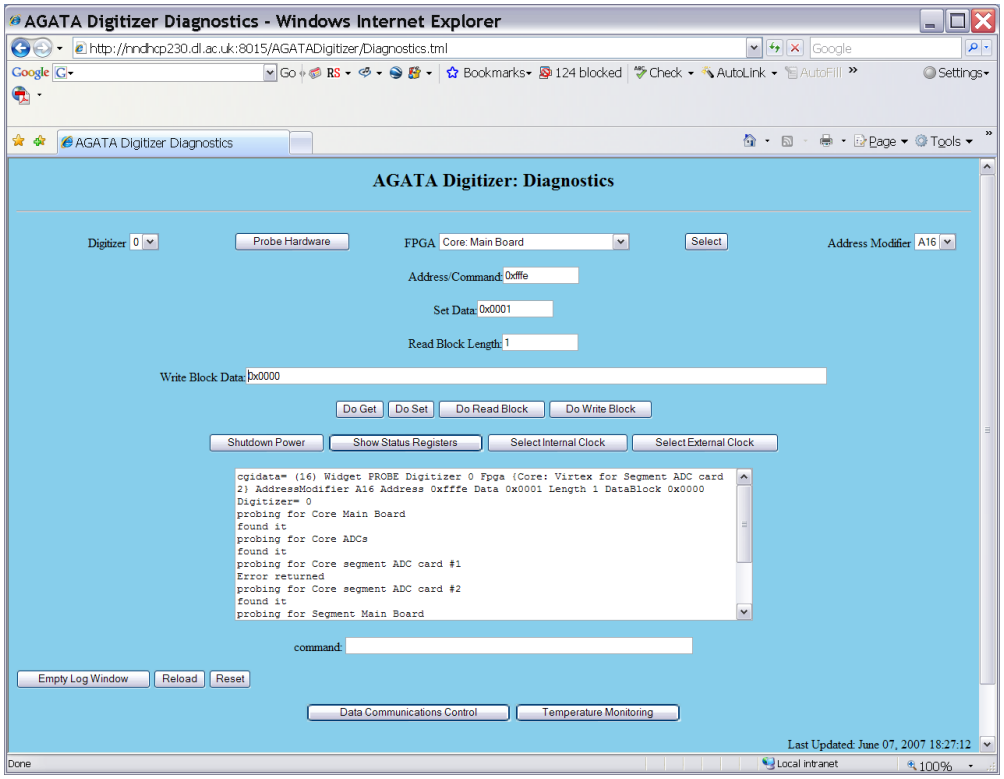
12 Preamp isolators and SYNC front panel input.

Ensure the isolation power connection is made to the Power board.
Ensure the Segment Test board is connected to the input.
Insert the loopback plug into the 34pin connector on the front panel of the Test board to allow the path of the Inh signals to be tested.
Connect the Logic Inspection lines to a scope.
Connect a Fast NIM pulse to the Sync front panel and to the ‘scope to allow monitoring.

Run the script *Segment_bits.tcl*. The script prompts for checks of the state of LEDs on the Test board and the logic state on the scope.
When prompted by the script check the Sync signal on the scope. The first one is the signal transmitted from the Core module. The second is the front panel signal.

13 Temperature sensors

Open an Internet Explorer window and connect to the AGATA digitizer page.



Probe for hardware until found.

The open the temperature monitor window. Check the temperatures for the segment card are within range of this typical reading :

```
Core at June 07, 2007 14:54:10
Seg2 Virtex = 39.5C
Seg2 analog = 34.5625C
Core Virtex = 33.875C
Core analog = 31.5C
PSU 1       = 22.4375C
PSU 2       = 26.5C
PSU 3       = 28.625C
```