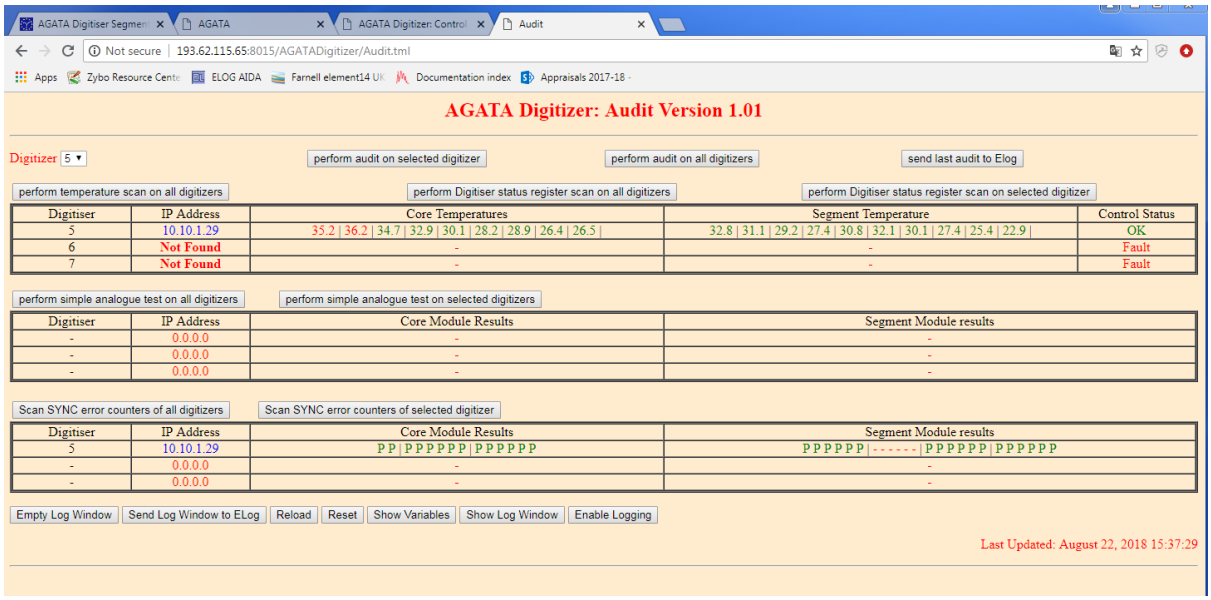
Using the AGATA Audit web page.

Overview

The AGATA digitizer controls contains an audit web page.

Access the Audit web page using http://<digitiser server ip >/AGATADigitizer/Audit.tml

(Pop-ups should be enabled)



When the page is opened it will use the global list of digitizers to create the “Digitizer” menu. Then create the results tables required for the number of digitizers; in the case of the example window there are three available.

When each of the Audit tests is performed the detailed results will be shown in a pop-up window and a summary will appear in the Audit window. That is in the case of the ‘simple analogue’ and the ‘SYNC error counter scan’ there will be a green P or a red F in the relevant module/channel position. If a module or ADC card is missing the results space is filled with red ‘-‘ instead.

Individual scans and tests

1. *Temperature scan*

The temperature scan always operates on all digitizers in the system. If a temperature measured is greater than 35.0 then it is shown in red otherwise its green. The control card status registers are read and analysed. The result is a green ‘OK’ or a red ‘Fault’ in the table. The pop-up window gives a deeper analysis which is helpful in the event of a Fault.

2. Digitiser status register scan

The control card status registers are read and analysed for each module. The result is a green ‘OK’ or a red ‘Fault’ in the table. The pop-up window gives a deeper analysis which is helpful in the event of a ‘Fault’.

3. Simple Analogue test

For each detector channel in each ADC board in the Digitizer the offset DAC is set to one of three voltages in sequence. The FPGA on the board has a built in average accumulator for each ADC output. 16 sequential ADC values are accumulated and then divided by 16. The result is compared to upper and lower limits for each DAC setting. Then a ‘P’ or ‘F’ is displayed in the table. The pop-up window shows the values read back for each channel.

The three DAC settings and associated limits are :-

DAC Setting	Lower Limit	Upper Limit
-Full Scale (0x8000)	0	2000
0	7000	9000
+Full Scale (0x7FFF)	14000	16000

4. Scan SYNC error counters

The SYNC pulse is received in the Core ADC card and distributed to the Core and Segment channels using the backplane. Each channel checks that SYNC pulses are arriving at the correct interval. If they are not then an error counter is incremented. If the Core ADC card is not receiving SYNC pulses at all then a message is printed in the table.

This test reads all the counters, waits for a second, reads them all again and compares the results. If the first and second are equal then it is a pass , ‘P’ , or else a fail , ‘F’. The pop-up window shows the values read back for each channel.