Report of Digitiser Segment board to Pre-Processor Segment Mezzanine optical data link tests at CSNSM Orsay. 23rd and 24th May 2006

Those present.
Patrick J. Coleman-Smith, Daresbury Laboratory UK.
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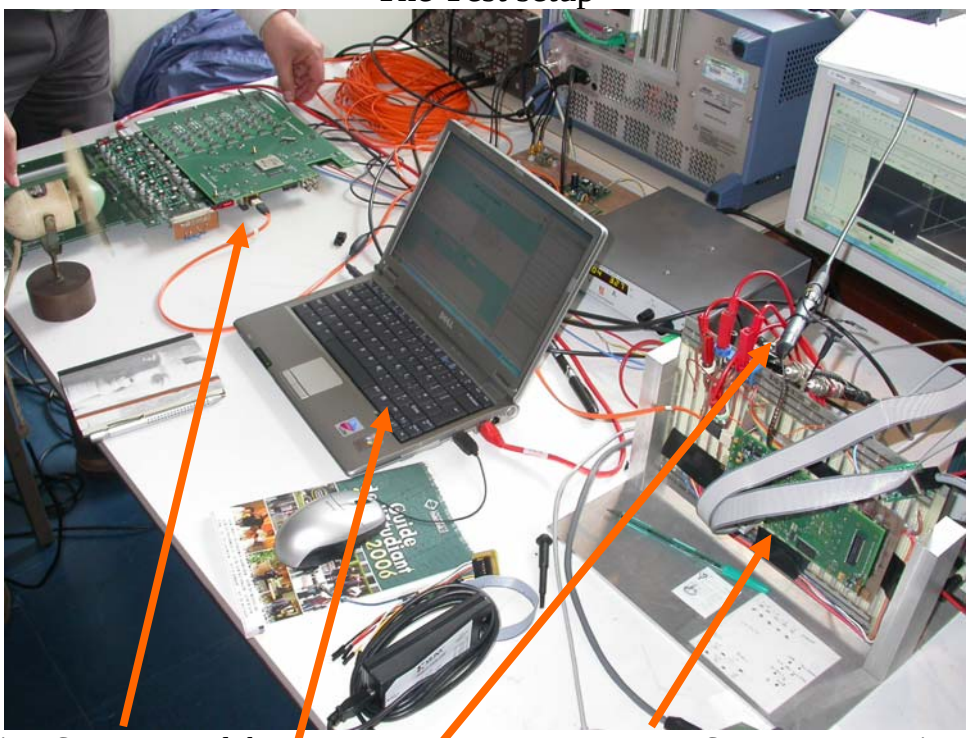
Sebastien Lhenoret, CSNSM Orsay, France.

The purpose of the test was to ensure data could be successfully transmitted from the digitiser to the preprocessor using the Xilinx Rocket I/O links over 6 fibres of a 12 fibre ribbon connection. Once established the connection should be tested over as long a period as possible. The quality of the signals in the data link to be investigated using a high bandwidth 'scope on loan to CSNSM from LeCroy.

The Test setup



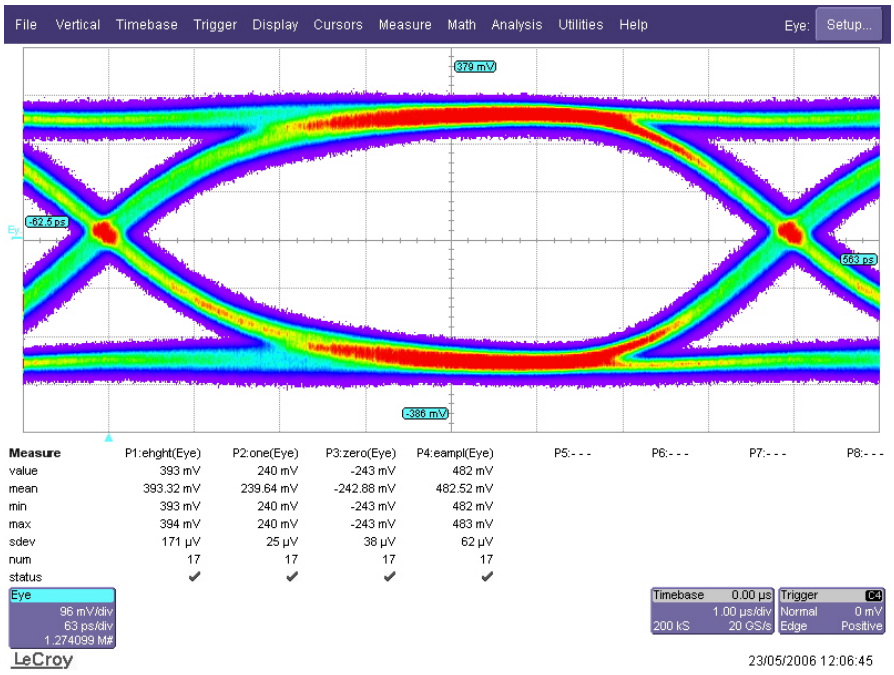
Digitiser Segment Module *Pre-Processor Segment Mezzanine*
Laptop controlling digitiser *LeCroy 7GHz probe*

Tuesday 23rd

The digitiser segment module and clock generator were unpacked, and established with the fan and power-supply provided by CSNSM. Communications between the web services in the controlling laptop and the digitiser were established after a few problems with the laptop networking.

The mezzanine board was installed on the test rig, and the external clock input was tested with different versions of VHDL. The intention was to use the same clock for both the receive, and transmit ends of the data link. The test was not successful. The

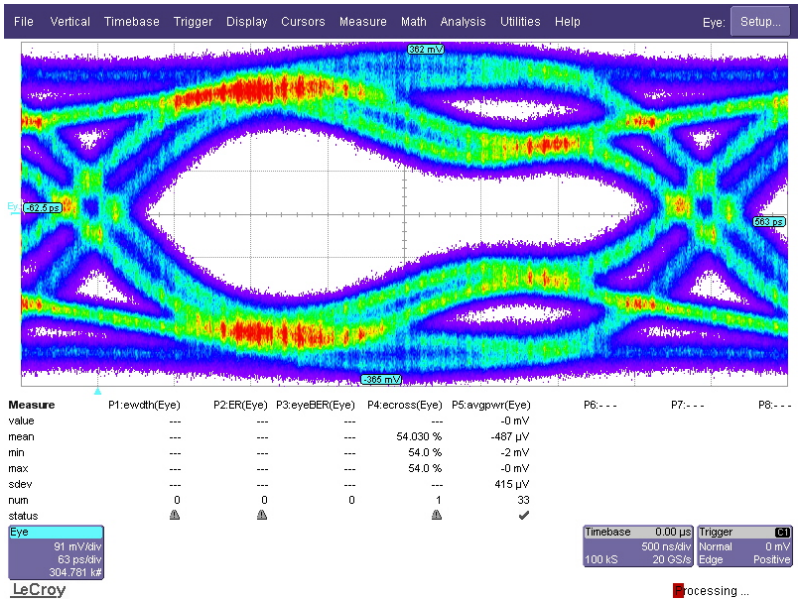
Mezzanine link tests had previously been carried out using the receive clock recovered from the input data.
The LeCroy ‘scope was an SDA6000, a very useful instrument for such tests as it was able to decode the serial data and determine signal quality. The ‘scope was connected to the output of a fibre optic receiver development board to examine the quality of signals transmitted from the Digitiser segment module. The result of a typical channel is shown below in the form of an ‘eye diagram’. This is a measure of signal quality as it shows the overlayed signal for each bit in the data stream. A wide open eye is good.



Output from a development board for the Fibre Optic receiver when connected to the fibre from the Digitiser Segment board.

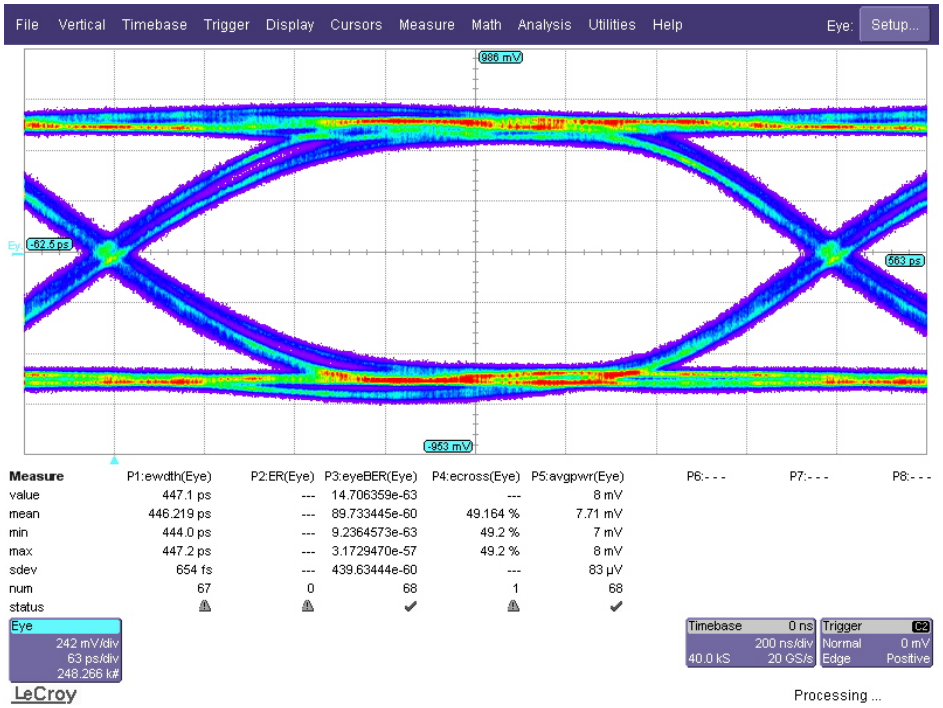
Wednesday 24th

It was decided to use the VHDL test code developed for the Mezzanine link tests, which used the recovered clock, instead of continuing to try and use the external clock input. The VHDL was modified to allow the input data stream and internal error counters to be displayed on an Agilent logic analyser when requested via an RS232 link between the Mezzanine card and a PC.
The links were established and incrementing data was successfully transmitted and viewed. The digitiser firmware is able to insert a single error when instructed. The error counters in the mezzanine card responded correctly showing a single error had been received and the following data was still valid.
The test was left running over the lunch period. Unfortunately during this time the Digitser segment firmware re-loaded for no apparent reason. (*Subsequent investigation at Daresbury has shown bad solder joints under a power supply module that delivers 1.5volts for the Virtex2Pro. This has been found in one other power supply board at Liverpool University, and is a manufacturing fault. The transport in hand luggage probably made this worse.)*
It was decided to use the remaining time to view the data link signal quality on the mezzanine board. A special 7GHz bandwidth probe was soldered onto the board, and an ‘eye diagram’ of the signal obtained. This is shown below.



LeCroy 7GHz BW probe connected to Pre-Processing Segment mezzanine Rocket I/O Receiver differential line on the pcb where it connects to the capacitors AC coupling the Optical receiver to the Rocket I/O port.

A second connection was tested, this had a worse ‘eye diagram’, but no hard copy was made.
In view of the poor quality a similar probe was used to monitor the data signal quality where it enters the fibre optic transmitter. This is shown below.



LeCroy 7GHz BW probe connected to Digitiser Segment module Rocket I/O Transmit differential line on the pcb where it connects through to the Optical transmitter.

The cause of this signal quality was not understood, and Patrick recommended testing the other data links on the mezzanine card while the LeCroy ‘scope was available.

The mezzanine board will be redesigned in the future to use a Virtex4 device to replace the two Virtex2Pro devices.

Conclusions.

The links between the two parts were established, and data transferred successfully despite the poor quality of the measured signals.
The link was not tested over an extended time period.
The quality of the signals at different points in the connection were monitored and those at the mezzanine where not good. Those at the Digitiser transmitter, and from the optical receiver development board were good.
A further test is required to achieve confidence in the data link over a longer period, a week would be sufficient. It is proposed to discuss this at the AGATA week in Liverpool in June.