AGATA digitizer to pre-processor Optical link trial.

The objective is to build a trial version of the optical link between the AGATA digitizer and the pre-processor.

The board will have the following equipment.

1. Xilinx FPGA with eight Rocket I/O serial links (XC2VP20-5FG676I).
2. Socket for a 12 channel VCSEL transmitter from Manufacturer A connected to three Rocket I/O links.
3. Socket for a 12 channel VCSEL receiver from Manufacturer A connected to three Rocket I/O links.
4. Socket for a 12 channel VCSEL transmitter from Manufacturer B connected to three Rocket I/O links.
5. Socket for a 12 channel VCSEL receiver from Manufacturer B connected to three Rocket I/O links.
6. Two Rocket I/O links connected to SMA connectors for wired connection tests.
7. Static RAM for test patterns to send and receive via the link.
8. Configuration memory for the Xilinx device programmable via JTAG, or Xilinx interface.
9. Buffered outputs for monitoring selected signals from the Xilinx device. Also a DAC for monitoring.
10. A TDR metronome interface to allow a single stable clock to be connected to both ends of the link, and for a timestamp to be generated.
11. VME bus interface to the Xilinx device for parameter control of the Rocket I/O links, loading and testing the RAM data, and control of the tests.
12. Power for the Xilinx to be provided either from the VME bus, or external power supplies. The choice is made using solder connections.
13. External clock input options connected to the Xilinx global clock inputs. For example PLL devices, and stable oscillators.

The trials to be held using two of these boards are :

A. Trial for the best link set-up method. This is the data sent when the link is started to ensure the bit stream is correctly synchronized.
B. Bit error rate test using simple transmission of a 16 bit counter over an experimental period (days ??).
C. Transmission of a sequence of data from the RAM, to be checked at the receiver against the same data.
D. Determining the effectiveness of the layout in producing good quality links.
E. Determining differences between the two manufacturers devices.
F. Implement a system to include IDLE, and COMMA (special bit patterns) words during normal transmission of data, rather than at link set-up to allow insertion of CRC, and improve stability of the transmitted clock.
G. If possible try different lengths of optical fibre ribbons with the data quality tests mention above.
H. Use the metronome timing interface to determine the time stability of the link relative to a SYNC pulse.