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AGATA – Report on Digitiser and Preprocessing test at Orsay November 2006

What happened

Since the proposal it was decided at a working group video conference to reduce the scope of the tests. The data transfer test was not carried out. The proposal is added at the end of this document.

The digitiser core module and equipment to validate it were shipped from Daresbury sucessfully.
The equipment was unpacked and the watercooling pipes connected to a cold water tap and sink in the test laboratory. The Core module was successfully controlled from a web interface on the Daresbury laptop PC. The temperatures monitored within the Core module showed a stable value of about 36 deg C.
The test equipment shipped from Daresbury was used to successfully validate the operation of the Core module. Nothing had been damaged in the process of shipping from Daresbury to Orsay.

The NIM modules were installed and connected to the digitiser Core module. A sine wave generator was used to drive all 14 ADC channels (2 x 6 segment + 1 x 2 Core) using 10m camera-link cables.

The preprocessor Core mezzanine was connected via a 10m fibre optic cable to the digitiser Core card. Clock and SYNC signals were successfully sent. The ADC data from the two core channels was seen on a logic analyser attached to the preprocessing core mezzanine.
VHDL firmware to receive and monitor the SYNC pulse stability as described in the proposal was developed to test all 14 channels.
The two preprocessor segment mezzanines were added, and connected to the segment cards of the digitiser core module. One with a 10m and the other with a 100m fibre optic cable.
The SYNC stability test was run successfully, with no errors, from 14:30 on the Wednesday to 09:30 on the Thursday.

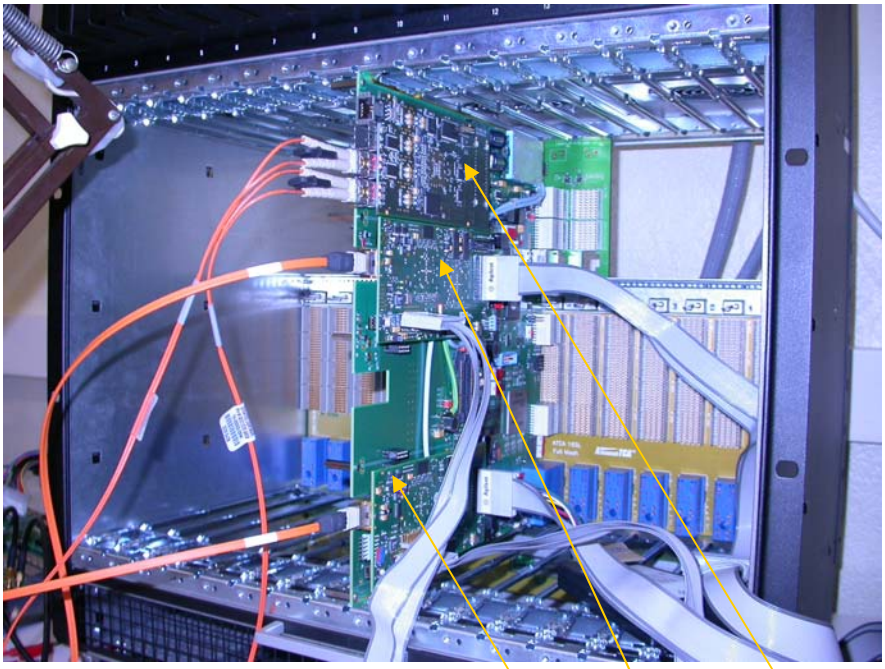
VHDL firmware to align the received data in the preprocessor based on the SYNC pulse was developed and tested successfully.

The equipment was dismantled and repacked for return to Daresbury on Thursday.

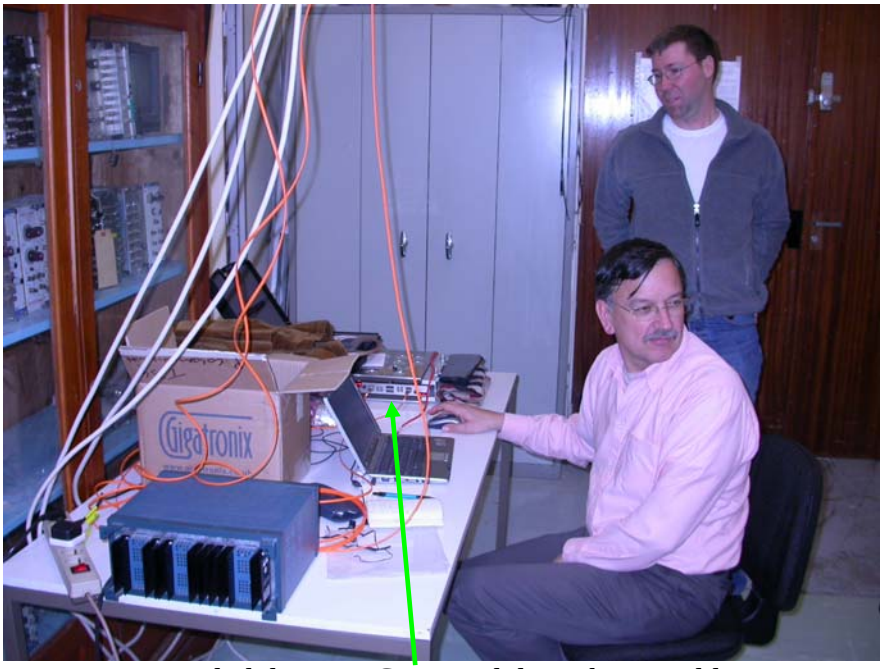
There follow some photographs of the equipment and some screen shots of the preprocessor logic analyser.

Conclusion.

The Clock and SYNC distribution within the Local Level processing of the AGATA data acquisition will operate successfully to provide stable aligned data.



Preprocessing ATCA crate with Carrier, Segment, Core and GTS Mezzanines.



Water cooled digitiser Core module with control laptop,
Orange fibre optic links, and white analogue Camera link cables.

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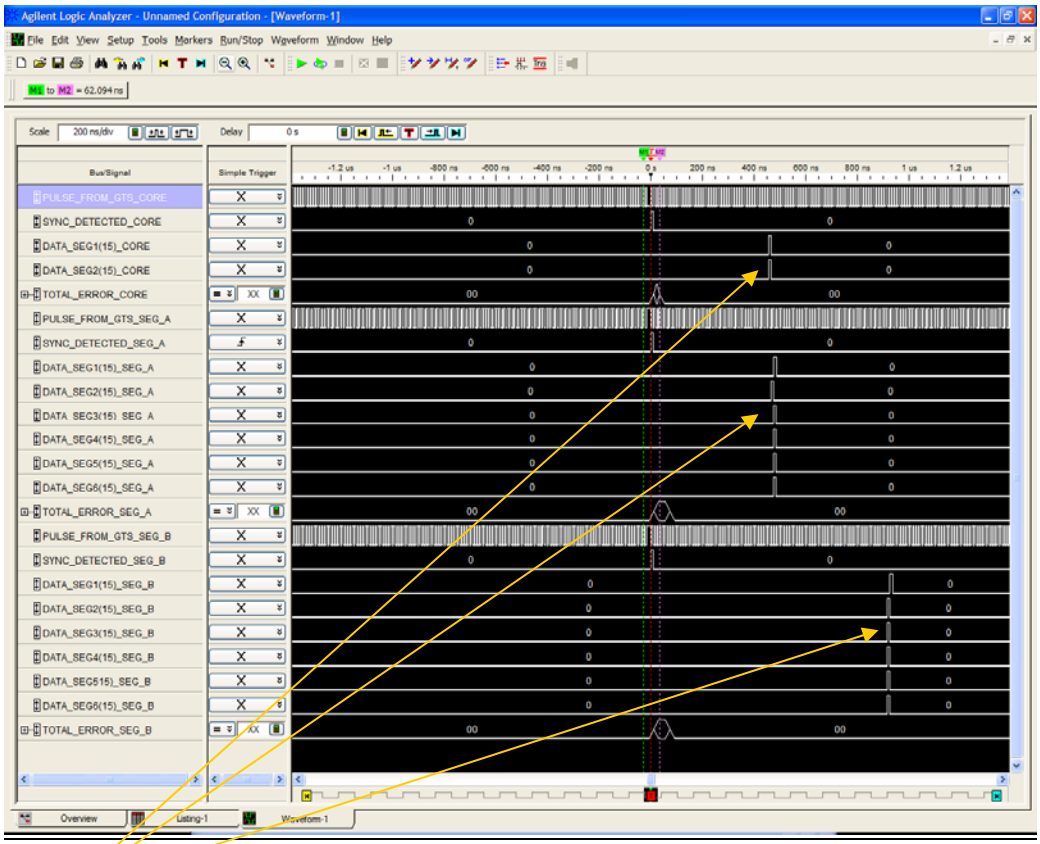
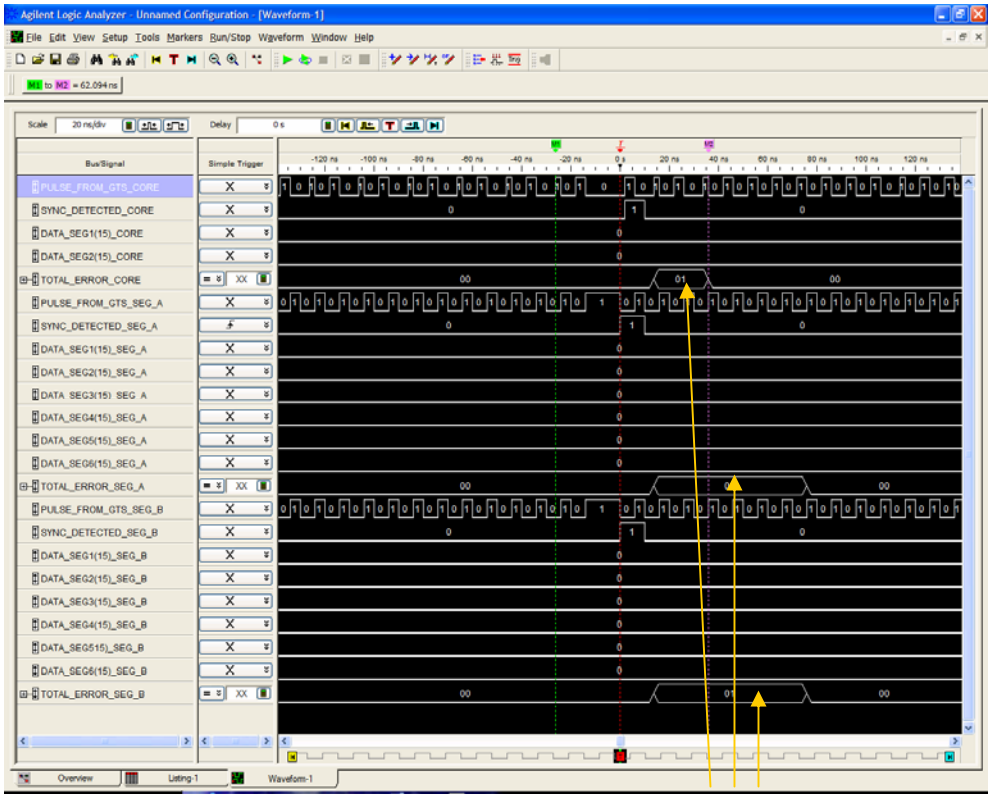


Logic analyser trace from the preprocessor showing the difference in arrival of the sync pulse (data bit 15 in each ADC channel) over the 10m and 100m cables.



Logic analyser trace from the preprocessor showing the error counters for all channels. The counter for each channel is shown in sequence.

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The proposal.

Abbreviations: Digitiser : DG ; Pre-Processor : PP.

Purpose. – prove the DG and PP can communicate.

To validate the transmission of the 100Mhz system clock from the PP core to the DG core.
To validate the transmission of the Sync pulse from the PP core to the DG core, and returned via the data paths.
To validate the transmission of data from the two DG core and 12 DG segment channels to the PP receivers.

Required AGATA equipment.

DG – Core module containing 1 Core ADC card, 2 Segment ADC cards, 1 Core power supply card, and 1 control card. 48volt power supply.
PP – 1 Carrier card, 1 ATCA crate, 1 GTS mezzanine, 1 Core mezzanine, 2 Segment mezzanines.

Required other equipment.

3 Single to differential convertor boxes to drive MDR-26 inputs of the DG core/segment boards from a pulse generator.
NIM crate.
PB4 or sine wave generator.
Water cooling for the DG module.
Logic Analyser to readout Mezzanines ?
Scope.

Test proceedure.

- Power up the equipment and ensure it works seperately.
- Connect the PP to DG core optical link. Check for clock at the output of the DG core clock distribution. Check for the presence of the Sync pulse at the DG inspection line. (*Would be useful to have a scope trigger from the GTS for this ?*)
- Connect the segment optical link. Transmit data (ramp/PRN) and read the error counters from the PP mezzanines. Inject single errors from the DG, and see single increments. Include the core channels.
- Transmit data from the DG ADCs (this will include the Sync). PP mezzanines to count the number of clock cycles, δt, between the transmitted Sync (distibuted on carrier card) and the received Sync from the DG (bit 15 of data). If δt measured is different from δt last measured, then increment a counter. Then the stability of the 14 data channels can be measured by reading the error counters. Similarly if Sync never comes ??