VME Metronome unit manual (C1100)

Unit description

The Metronome unit is a 12HP wide VME unit which is an A32,D8(O),D32 device. Most addressing is done in the VME I/O space with only one address used in the 32 bit memory address area.

The purpose of the unit is to generate 100MHz clock signals that are adjustable in 2.5ns delay steps (quadrature clocks) in order to synchronise the arrival times of equivalent edges at the end of the distribution cables for each channel in use. The sync and resync pulses are also delayed but in 2.5ns steps from 0 to 160ns to remove cable delays from them. Figure (1) shows the reason for this.

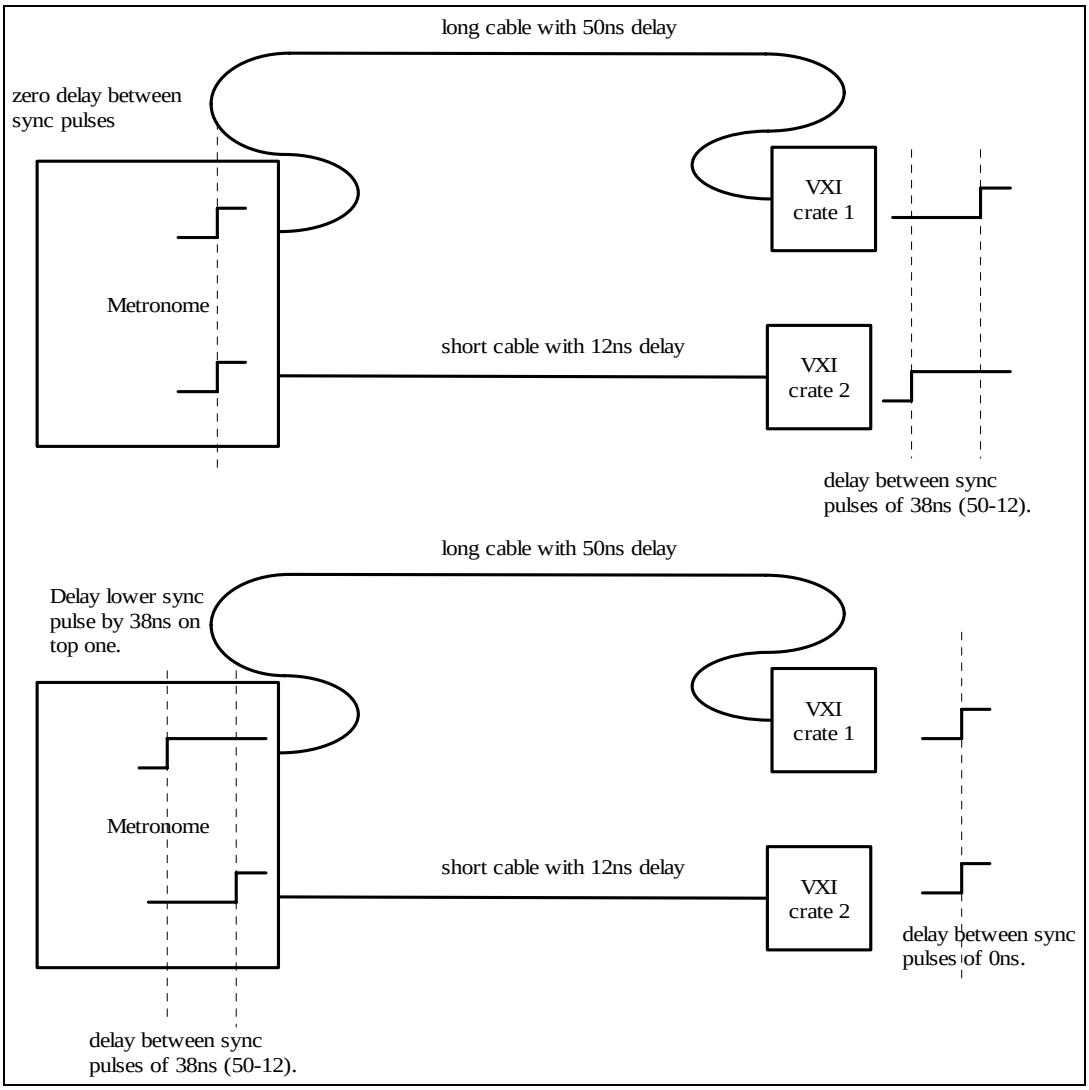

Figure 1 Effect of cable lengths on sync pulse delay showing Metronome compensating.

It is important for the time stamp system to work correctly that each piece of equipment supplied by a clock signal from the Metronome unit receives the sync pulse and clock phase at the same relative time.

Each channel in the Metronome unit has the ability to have a delay and clock phase programmed in order to compensate for these delays. The method of calibrating each channel of the Metronome will be discussed later.

The Metronome unit contains a 100MHz crystal and the main clock generation counter is contained in a low power Xilinx CPLD device. This allows for a battery backup system to be incorporated in the unit. This will keep the Metronome ticking even when mains/crate power has been off for several hours. This will allow for resolving any power supply or crate problems without loss of timing in the experiment. It should be also possible to unplug the Metronome from a faulty VME crate and place it in a new one (crate powered off) without loss of timing information.

The card does not respond to resets from a VME backplane in the normal manner. This is deliberate to prevent the unit being reset when a crate is powered on or off or a sysreset is done. In order to reset the unit, at the start of an experiment or after doing a calibration, it is necessary to write to a set VME address three times. Each write has a different data value required and the sequence must be completed to reset the unit. The reset circuitry will re-initialise itself if the wrong data is written or if it is written in the wrong sequence. The first write has data AA(hex) the second has 55(hex) and the third write will actually do the reset on the unit (without any specific data value but avoiding AA(hex) or 55(hex)).

A reset will have the following effect.

- The unit will be stopped
- The main time counter will be set to zero.

Other registers in the unit will be unaffected. Any delay values written will not be changed and any other settings will be maintained.

To start the main clock at the start of an experiment or during calibration a VME write ‘Start Once’ is performed. This has the effect of starting the main counter and removing the RESET signal from each of the channel outputs on the 9 pin D types. It is possible to halt data collection without stopping the main counter by issuing a ‘Stop’ command. This will re-assert the RESET signal on the D types without effecting the main clock. The ‘Start Once’ command will now restart data collection without reinitialising the main counter. Note that the main counter continues to run continuously until an ‘Initialise’ sequence is issued. NOTE it will be necessary to run a resync sequence after issuing a Stop/Start event as the external time stamp counters will not restart with the correct experiment time in them.

IMPORTANT NOTES

The STOP/START mechanism should be used with great care. It should only be used if a power failure or similar event has caused a major system fault. It is not a general experiment RUN/HALT and should not be used as such. A ‘Stop’ should ideally only be done at the very end of an experiment to allow all the data buffers in the system to empty before ending.

A ‘Stop’ command is performed by issuing a START command with data = 0.
A ‘Start’ command is performed by issuing a START command with data = 1.

Calibration sequence

In order to determine the delay along each cable connected to the external equipment and the Metronome unit, it is necessary to do a calibration. Assuming cables are connected to

Channel 0,1 and 2. Channel 0 is first selected with the 'Channel Select' VME command (data on D2-D0 = 0). The remote unit is put into "calibrate foldback" mode, the Metronome clock is initialised and 'Start Once' is issued so that sync pulses are driven out on the D type connector pins. The returned sync signal is received on the ERROR lines of the D type. To make a calibration measurement an 'Arm Calibration Test' command is issued (D0 = 1). After 2 sync pulsed are sent the returned delay value (in 2.5ns steps) is available in the Delay Value register, which is read by the 'OE Delay Value' command. The bits read are D0-D5 delay time data (in 2.5ns steps), D6 = 1 indicates delay too great and D7 = 1 indicates that the data is a valid value, returned in response to the 'Arm' command. The delay will be between 0 and a maximum 160ns. This is the delay up and back down the cable and includes any delay in the remote electronics.

The process may be repeated for the same channel in order to collect statistical variance of the delay to choose the correct delay value to apply later to the 3 channels being used. Each time a measurement is to be made an 'Arm Calibration test' command must be done with D0=1 to enable the time measurement logic. Two sync pulses are always required to make the measurements. A delay, between arming and reading the resultant value, of 1,320us must be allowed.

The delay for channel 1 is done in exactly the same way (initialise and Start Once will not be required if already done for channel 0). The channel is selected with the 'Channel Select command' and then the 'Arm Calibration Test' command is issued. After 2 sync pulses the delay value will be in the delay value register.

The above is repeated for channel 3.

Using the results.

Suppose we measure the following delays after several samples to generate statistical average delays.

1. Ch 0 delay 27.8ns (cable delay of 27.8/2ns=13.9ns)
2. Ch 1 delay 84.3ns (cable delay of 84.3/2ns=42.15ns)
3. Ch 2 delay 61.5ns (cable delay of 61.5/2ns=30.75ns)

The channel with the longest delay (Ch 1) will have the shortest delay time put into its delay register.

- Suppose we load 0ns into the register for Channel 1.
- Channel 0 will need a delay of ((84.3-27.8)/2)ns = 28.25ns loaded and
- Channel 2 will require a delay of ((84.3-61.5)/2)ns=11.4ns loaded.

Since it is only possible to load values in 2.5ns steps the actual values for Channel 0 and 2 respectively would be 27.5ns and 12.5ns. The values actually loaded would be 0B(hex), 0(hex) and 5(hex) for the three channels. These are the nearest values to the calculated delays (errors of 28.25-27.5=0.75ns and 12.5-11.4=1.1ns respectively. After doing a calibration the main clock may be reset by issuing an initialisation sequence if it is a requirement that the clock is zeroed at the beginning of a run. It is not necessary to do this if a calibration has been needed during an experiment or if the absolute clock value is not required.

The Metronome is now calibrated and ready for basic use.

It is not necessary to load the Metronome delay registers with any particular value, nor zero them before doing a calibration run.

Error return signals

The Error Status checking must be enabled in order to function. This is done by writing zero with the 'Arm Calibration Test' command. (D0=1 arms test mode and must be done before each sample (arms time measurement circuits). D0=0 sets system back into Error checking mode after calibration (prevents error flags being set during calibration)).

If any of the equipment (VXI crate etc.) detects a time sync error then an ERROR signal is sent to the Metronome unit channel connected to that equipment. This error is latched as a bit in the Error Status Register ('Read Interrupt Status' command) in the Metronome unit. Also, if enabled, an interrupt can be generated from this occurrence. Please see later for interrupt setting.

Errors can be cleared with the 'Clear Error Status' command once the error has been removed from the channel input.

Resynchronisation of faulty external channel

When a faulty channel sync has been detected externally and an ERROR signal has been received by the Metronome and subsequently detected by the VME controller, it is necessary to resynchronise the external equipment to the correct time stamp count.

(NOTE - In certain conditions when the data from the faulty external unit shows no time stamp errors in the top 32 bits, it would not be necessary to do a resynchronisation cycle. The lower 16 bits will have been resynchronised automatically and the ERROR flag can safely be cleared both in the external unit and the Metronome. The suitability of not doing a resynchronisation cycle is dependant an the external hardware, software and data rates and will be experiment dependant. Not doing a resync saves time and less data is lost. It is all a matter of how easy it is and how long it takes to determine that the data from the faulty unit has not got a corrupted top 32 bit time stamp value)

In order to resynchronise the external unit the following procedure is followed.

1. External unit(s) has a 32 bit value loaded into its time stamp register which is some time later than the current time stamp value (top 32 bits of time stamp value only).
2. The same value as loaded in 1 (above) is loaded into the resync register in the Metronome unit. ('Write resync register' command).
3. The External unit is "Armed" to accept a resynchronisation cycle.
4. When the Metronome detects the same time stamp counter value as the value in the resync register, a RESYNC pulse is added 16 counts after the normal sync pulse for that cycle. The external unit will use this resync pulse to reset the top 32 bits of its time stamp register to be the same as the Metronome. The bottom 16 bits are reset by the Sync pulse each cycle so will already be in sync.

Several channels can be done simultaneously as the resync pulse will be present on all the channel outputs.

Note that after starting a new experiment or restarting using the 'Start Once' command all external crates will be out of sync. Therefore a Resynchronisation cycle will be required to synchronise all the external units to each other.

When starting a new experiment all external modules should be reset to have their counters at zero. After 42 clocks of the Metronome counter a sync pulse will be generated and all

external units will then be in synchronism. Any data collected in the first 42 clock pulse period (420ns) should be discarded. This is due to the RESET signal, used to start and stop external units, on each channel not being guaranteed to be in time sync with any clock or sync pulse. For all modules the top 32 bits in the time stamp will therefore agree (0) and any time error in the lower clock bits will be corrected by the time aligned sync pulse.

Interrupt setup

The unit can be set up to generate an interrupt if any channel receives an ERROR signal from any channel. To do this the jumpers on the card need to be configured (see later) and the Vector Address loaded into the Interrupt Vector register ('Load Vector' command with D0-7).

To enable interrupts from the unit the 'Load Interrupt Enable' command is issued with D0=1 to enable and D0=0 to disable interrupts. The 'Arm Calibration' register must be set to 0 to enable the error register ('Arm Calibration test' command with D0=0).

When any ERROR signal is received by an input on the Metronome unit the corresponding error bit will be set in the interrupt status register and an interrupt will be generated on the VME bus (if interrupt enabled). When the status register is read the interrupt will be disabled. To re-enable the interrupt after the error has been processed (and any resync required is done), the 'Load Interrupt Enable' command must be done again (D0=1).

Jumper and switch settings

There are 2 DIL switch modules for RAM address space decoding, SW2(lsb)/SW3(msb), and 1 DIL module for I/O, SW1. Closing a switch sets the bit associated to 0. An open switch is a 1. The Ram address range is 0000xxxx to ffffxxxx and the I/O range is 00xx to FFxx.

Interrupt jumpers are labelled IS0-IS2 and I1. IS0-2 are set to be the interrupt level chosen as a binary code. Closing a jumper will set the bit to 0. e.g. 010 is Interrupt level 2. Placing the jumper on any of IS0-2 jumpers to the top (pins 1-2) sets a 1, placed toward the bottom of the jumper implies a 0 (pins 2-3), The Jumper I1 sets which interrupt line is driven on the VME backplane. The location selected for this jumper must match the code set on IS0-2. Pin 1 on the I1 jumper is toward the bottom of the board and represents interrupt level 1, the next location interrupt 2 etc.. The top location is a jumper storage point and no interrupt is selected. Note that Interrupt 0 is not a valid selection.

Jumper CS selects the Crystal Source for the main clock chip. This jumper selects either the on board crystal (default) or the external LVDS crystal input on the LEMO connector L1. Set to the right hand pins (pins 2-3) to select the on board crystal or set to the left hand pins (pins 1-2) to select an external source.

All other jumpers and links on the board are for design use only and should not be tampered with.

For information only >>> VS selects Crystal Voltage (+5V/+3.3V), to allow for other crystals and should not be changed. PUON, RES and GSR are debug pins only for the BGA chip. M1 to M6, P1 to P6 and Q1 to Q6 are to program the logic devices on board and should have nothing connected to them. WARNING power supplies are present on some of these pins. DO NOT SHORT with jumpers etc.

Starting an experimental run

When beginning and experiment the following typical sequence of events should be performed. This is not a definitive sequence and it is up to the user to determine what is suitable and required for their circumstances. It is included as a guide only.

1. Units connected to the metronome should be placed in 'Calibrate' modes in order to perform cable calibrations.
2. Metronome is initialised and calibration is performed.
3. Calibration values should be loaded into the Metronome either as just measured or from a file if no changes have been made since previous calibration.
4. Metronome should be Initialised once more (if absolute clock time required).
5. Error checking should be enabled as should interrupts in the Metronome.
6. Metronome counter value is read and value is loaded into external units.
7. External units should be made ready to run and placed in a 'Running' state waiting for the Metronome generated RESET signal to be removed.
8. Metronome is set to generate a resync sequence.
9. The 'Start Once' signal is sent to the Metronome and the experiment begins.
10. After 42 clock pulses the Sync pulse at each external unit will reset all the time stamp counters to be the same as in the metronome. Please see footnote 1.
11. Error status bits occurring in the first 1us after the start should be ignored and reset.
12. The first 420ns of data should be discarded.

An annotated diagram is shown of the top of the PCB for information (Figure 2) below.

[1] The counter in the time stamp unit will be 16 (42-26 (plus cable delays)) counts ahead of the external time stamp value, which is set in the external units to a count of 26 when a sync pulse is detected. This is not important, it is the accurate repetition time of 655.36us that matters. The time stamp is 48 bits long. The RESYNC pulse sets only the top 32 bits of time stamp to a preset value. The SYNC pulse only resets the bottom 16 bits to be 26. This ensures that small timing errors are corrected within 655.36us. Large timing errors, caused by power outs etc., are cured by use of the resync pulse system. Software checking should be able to determine the fault in the external units.

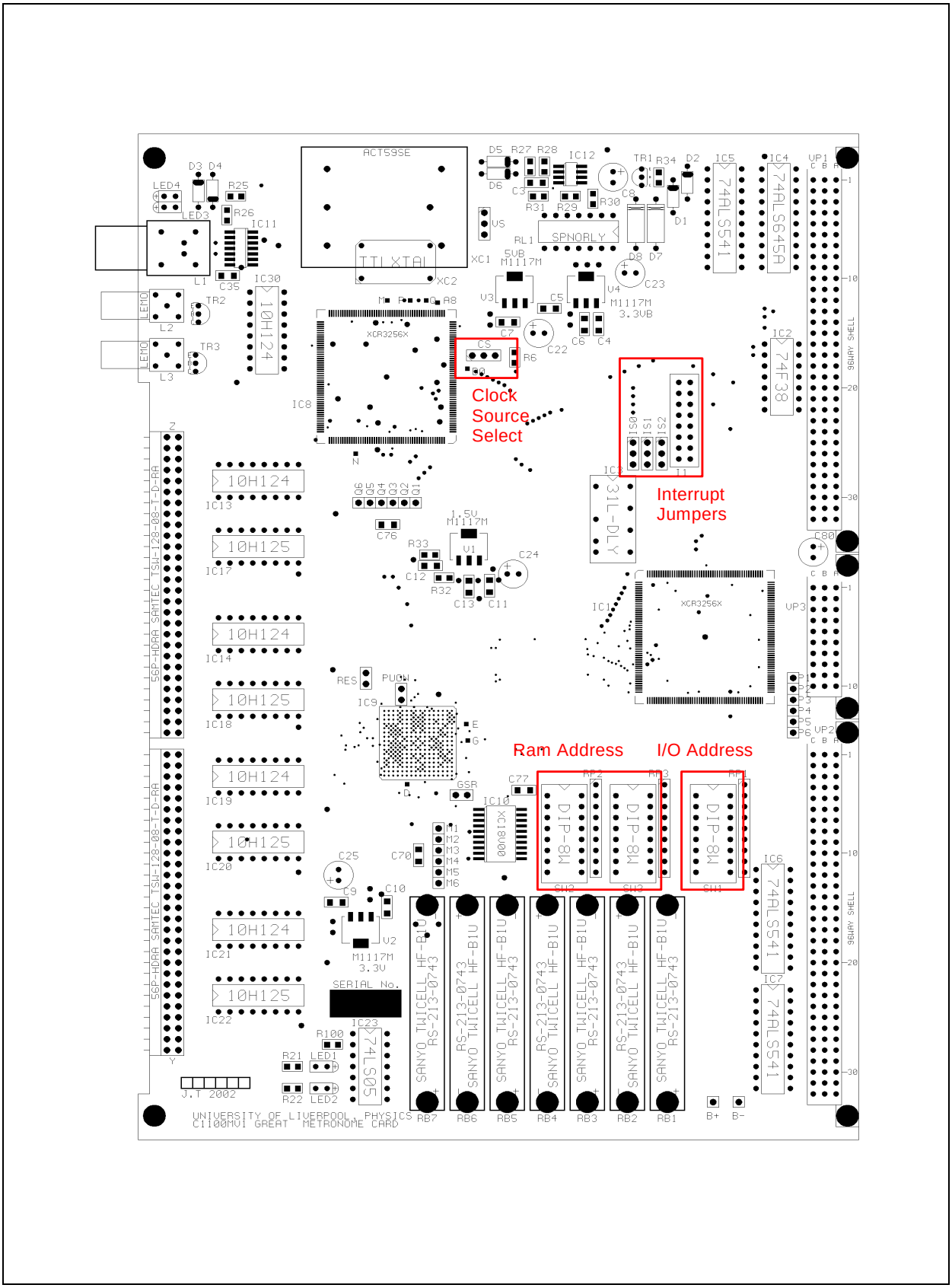

Figure 2 PCB Layout showing user Jumpers and Switches

Address decoding.

A32, D8 (O), D32.

COMMAND (R/W)	*ADDRESS*	*DATA*
Initialise (W+W+W)	xx13 (Note 2)	D0-D7 (aa – 55 – xx)
Start Once (W) (or Stop)	xx15	START =01, STOP=00
Load Resync value (W)	xxxxFFFC	D0-D31
Read counter and status (R)	xxxxFFFC	D31-D1 counter top 31 bits. D0 = Start/Stop state (1=Started 0 =Stopped) [Clock is NOT stopped]
Initialisation status (R)	xx01 (SR0) (Note 1)	Status bit D0
Channel error found	xx01 (SR0) (Note 1)	Status bit D2

COMMAND (R/W)	*ADDRESS*	*DATA*
Load clock and sync delay (W) ch0	xx01	D0-D5
Load clock and sync delay (W) ch1	xx03	D0-D5
Load clock and sync delay (W) ch2	xx05	D0-D5
Load clock and sync delay (W) ch3	xx07	D0-D5
Load clock and sync delay (W) ch4	xx09	D0-D5
Load clock and sync delay (W) ch5	xx0B	D0-D5
Load clock and sync delay (W) ch6	xx0D	D0-D5
Load clock and sync delay (W) ch7	xx0F	D0-D5
Arm calibration test (W) (Arm before each timing measurement is made)	xx11	arm=01, disarm=00 (must be disarmed to allow error checking)
Channel Select (W)	xx19	D0-D2
OE delay value (R)	xx0F	Dly0-Dly5, Oflw, Valid
PLL Lock status (R)	xx01 (SR0) (1)	Status bit D1

Interrupter requirements (contained in VME interface chip)

COMMAND (R/W)	*ADDRESS*	*DATA*
Load interrupt vector (W)	xx1D	D0-D7
Load interrupt enable (W)	xx1F	enable=01, disable=00
Read interrupt status (R) (Read ERROR status)	xx15	D0-D7
Clear Error status (W)	xx1B	No Data

Interrupt is disabled during vector read cycle (ROAK).

NOTES.

(1) SR0 is Status Register 0 contained within VME interface chip.

(2) The unit requires 3 write events in sequence to reset the master counter to zero and clear the unit for the start of an experiment. Data xx is any value except AA or 55. This ensures that after a reset it is more difficult to accidentally get a reset within the unit.

Status Register

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
x	x	x	x	x	Channel Error	Clock PLL Lock	Init Ready

Figure 3 Status Register

The status register reflects the following conditions

- The Initialisation Ready bit (D0) is set to 1 if an initialisation sequence has been completed sucessfully (Three writes to initialisation register with correct data).
- The Phase Lock Loop (PLL) of the main clock chip being sucessfully locked (D1=0). This is the good state. 1 indicates a clock error which is a fatal condition.
- If any channel is showing an ERROR input D2 is set to 1, normally 0.

Front panel connections and indicators.

From the top of the panel down as follows :-

Battery Power	On when battery charging or running from battery power only
Crate Power	On when crate power is present.
Ext LVDS Clock	External 100MHz clock. LVDS differential clock input.
Sync Monitor	Negative NIM output of master, undelayed sync pulse.
Resync Monitor	Negative NIM output of master, undelayed resync pulse. Only when present during programmed resync cycle.
CH0 to CH7	Main timing outputs (CLOCK, SYNC, RESET and ERROR). 8 time aligned output channels.

Channel output connector pinouts

9 Pin ‘D’ type sockets. (CH0-CH7)

Pin Number	Function
1	100MHz CLOCK out ECL (H)
2	0V
3	ERROR input ECL (H)
4	RESET out ECL (H)
5	SYNC out ECL (H)
6	100MHz CLOCK out ECL (L)
7	ERROR input ECL (L)
8	RESET out ECL (L)
9	SYNC out ECL (L)

The *reset* signal is the Start/Stop setting of the *Start Once* register.
The *error* signal is a returned error from the external equipment and also the cable delay feedback signal in calibrate mode.

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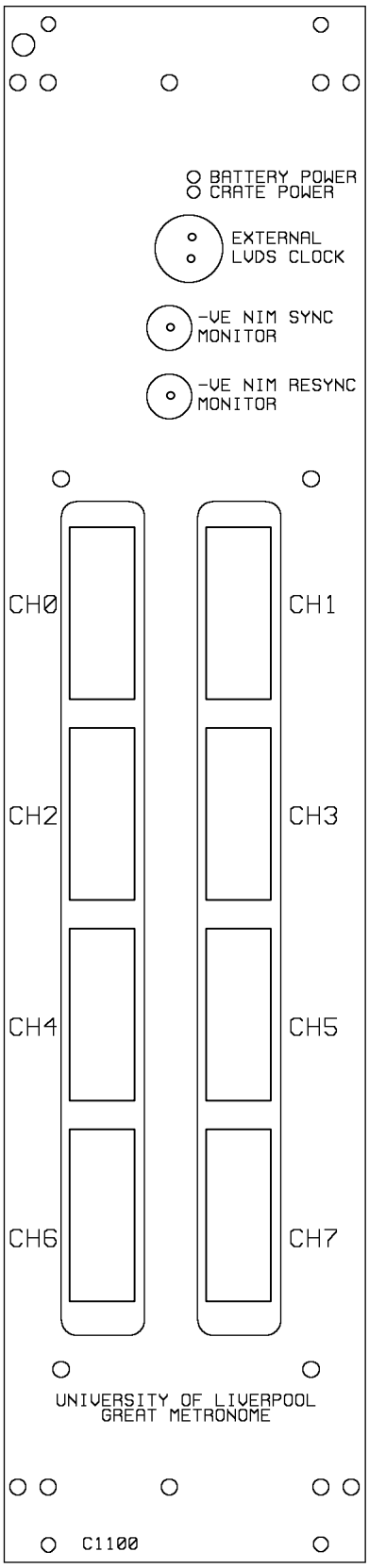

Figure 4 Front Panel Layout