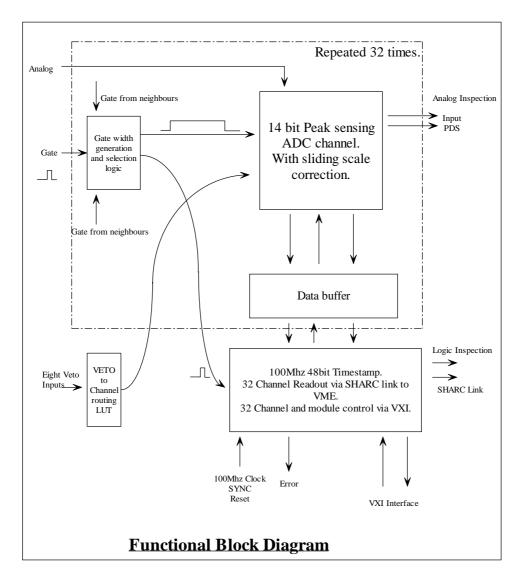
## GREAT 32 channel peak sensing ADC module: User Manual

## **Specification:**

32 independent timestamped peak sensing, ADC channels.

- $\triangleright$  Input range 0 to +8V.
- > Sliding scale correction.
- > Peaking time greater than 1uS.
- ➤ Gate input Fast NIM, and Differential ECL.
- ➤ Timestamp derived from a 100Mhz 48 bit counter, synchronized to a Master counter present in the system timing co-ordinator, the VME based Metronome module. The timestamp is the time of the leading edge of the input Gate pulse.



The block diagram above shows the functional layout of the module. There are 32 independent channels. Each channel comprises Gate selection and pulse width generation, an ADC channel card, and a data buffer. The channels are controlled and readout by common logic. Analog and Logic inspection lines allow the function of the channel to monitored.

The Gate selection and pulse width generation logic is used to route the input Gate signals from the front panel to the ADC. The ADC gate pulse width is determined by a slider on the MIDAS TDR32V control window. It is possible to route other front panel Gate inputs to generate the channels ADC gate in cases such as strip detector neighbour triggering. This is controlled by selecting the 'Channel Mode'. For a more detailed explanation of the different modes see EDOC505.

A Timestamp is stored at the leading edge of the Gate.

The ADC channel converts at the end of the ADC gate signal. The ADC gate signal should be greater than 1uS wide for best results.

The input voltage to the ADC card must be in the range 0 to 8V (8V approximately). It must be positive with respect to ground. The Peak detector will only operate with positive inputs and erroneous ADC codes will be generated should the 'peak' happen to pull the input below ground.

After conversion the ADC is readout, and reset. The data is stored in a buffer for transmission with the Timestamp to the Event Collator in a VME crate. The module will run with all 32 channels working with random data at 10K conversions per channel. Should the buffer become full, due to flow control, the entire module is inhibited. A scaler, Blocked Event Scaler, counts every Gate that is missed during this period.

Each module has eight scalers which can be allocated to any of the 32 channels using the main window in MIDAS.

## User Interface in MIDAS.

Controls for each channel:

Enable/Disable.

ADC gate pulse width, 50nS to 25.6uS.

Gate Selection.

Channel Mode: Disabled.

Direct.
Neighbour.
Group 1 or More.
Group only 1.

Analog Inspection:

Input to channel.

PDS from ADC module. (Peak Detect and Stretch)

Logic Inspection. There are a large number of options on this menu. Three signals provide the best information about the use of the channel.

Front\_panel\_gate\_input: Signal into the ADC Gate selection logic.

ADC\_Gate: Signal to the ADC. Select through the ADC sub-

menu from the main Digital inspection line

menu.

Gate\_input\_to\_width\_chip

Signal within the logic indicates the channel Busy time. Select through the ADC sub-menu from the main Digital inspection line menu.

```
Disconnected
Front_Panel_Gate_Input
Blocked Increment
Timestamp_Counter_Clear
Timestamp_Counter_Enable
SYNC
Sync_error_reset
Sync_to_error
Gate_inminus1
Gate inminus2
Gate_inplus1
Gate_inplus2
Ready_for_next
Wait
Data Ready
FIFO_Read_request
FIFO_Write_request
FIFO Full
Pause
Resume
Halted
Sync_Pulse
Sync_A_not_equal_B
Sync_error
FIFO_empty
Blocked_Scaler_Overflow
Front_Panel_Veto
ADC
ADC 0=>15
ADC_16=>31
SHARC
Ts ready
Ts_read
Sharc_fifo_read_request
Sharc_fifo_write_request
Readout Halted
Readout_Anyfull
Readout_Fifo_Empty
```

Main Digital menu

Gate\_input\_to\_width\_chip

ADC\_Gate

ADC\_Veto

ADC\_Selected

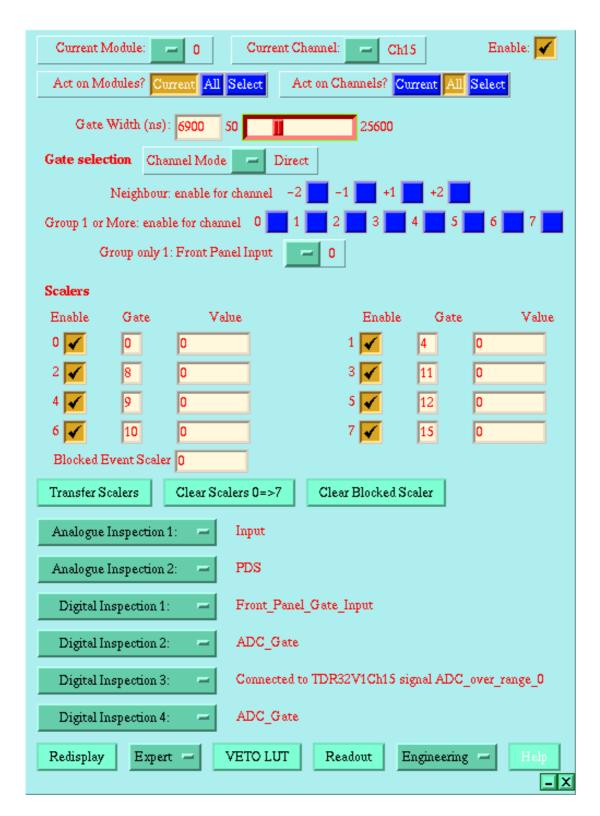
ADC\_Data\_Available

ADC\_readout\_fifo\_empty

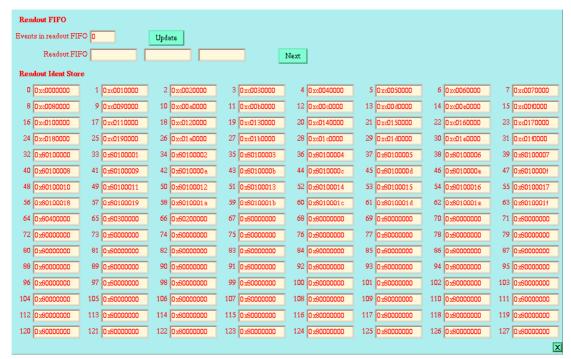
ADC\_readout\_fifo\_full

ADC\_readout\_fifo\_write

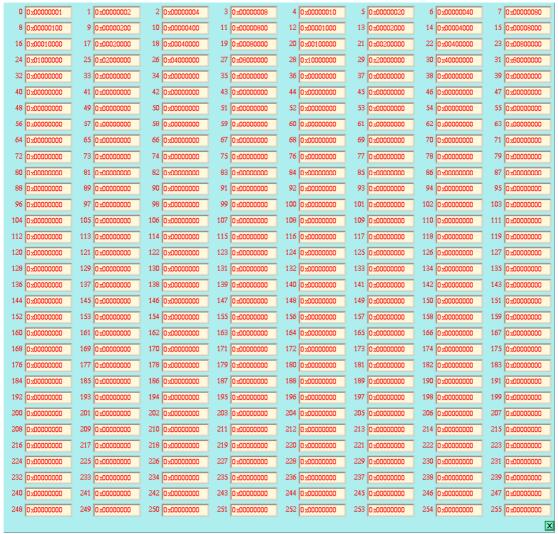
ADC sub-menu



Main card setup window. Launched by selecting TDR32V from the VXI module menu in the Base frame.

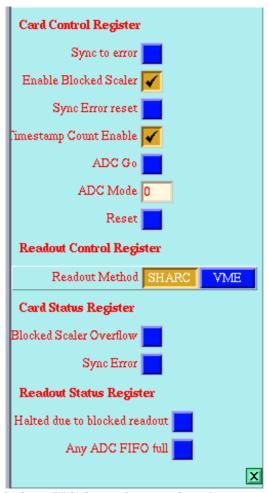


The ident attached to the ADC data, and the information sent with the full timestamp is stored here, in the Readout ident store.





The Engineering => electronics selection. The serial number, and modification number of the module are shown here.



The Expert => setup window. This is used to monitor the status of the SYNC pulse synchronisation. The counter is enabled , and errors reset.

