User Guide for EXOGAM Escape Suppression Shield (ESS) Card

Contents:

1 Introduction

The EXOGAM segmented Clover Ge detectors use escape suppression shields made of Bismuth Germanate (BGO) at the sides and Caesium Iodide (CsI) as back-catchers. The number of BGO crystals in the shield varies depending on whether EXOGAM is operating in its close packed mode or its normal mode, however the phototubes are ganged together in both cases to give 4 outputs from the side pieces and another 4 from the back catcher. All that changes is that extra phototubes are added to the daisy chain when the extra side pieces of BGO are added.

The HV is daisy chained between phototubes with a small potentiometer provided on each base for gain matching. It is not possible to individually switch HV on/off to gain match or test individual phototubes via this VXI card. There are no gain adjustments in the ESS card. Gain is set on the tubes.

The 8 signals from a shield are handled by a single channel of electronics which measures the sum energy of all 8 inputs and the timing of each quarter of the shield measured against its respective Ge CFD. In addition to energy and timing, a 12 bit hit pattern is generated from each shield and its associated Clover Ge. All inputs can be time-aligned before inclusion in the pattern or use in TDCs.

Four Vetos are provided from each shield (one per Ge crystal) for the associated Ge cards. The user may select whether each Veto is generated from all the shield elements (i.e. all 4 are the same) or generated individually from just the quarter nearest its Ge crystal. The user may also select whether the Veto is derived from the side pieces alone, the back catcher alone or from the back catcher and side pieces taken together. The timing (delay and width) of the veto is adjustable under software control for optimum suppression.

The ESS card is designed primarily to enhance the Ge peak-total, hence the name, Escape Suppression Shield (ESS) card. The card also measures the shield's sum energy in the range 0-20MeV. The ESS card's prime purpose is providing good Veto information.

The signals from the phototubes to the ESS card are driven from buffers in the HV distribution box mounted close to the shield. The signals are amplified and driven by line drivers in the preamplifiers along cables to the ESS card. There is no shaping in the preamplifiers to reduce the signal delays and therefore give the best timing. All signal shaping takes place within the ESS card.

A front panel sumbus output is provided, generating 4mA/active shield.

Each ESS card instruments 4 complete escape suppression shields.

v3 (Originally created May 2001)
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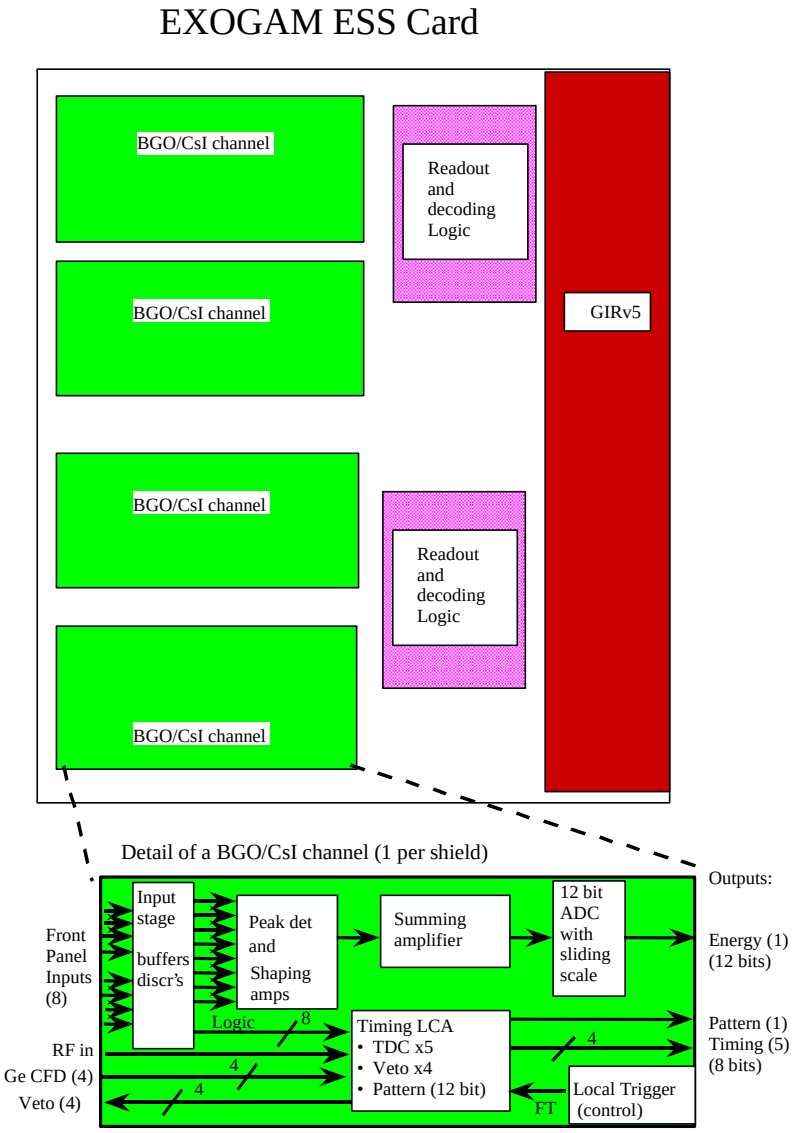
2 General Architecture



3 User Interface

The ESS card, like the rest of EXOGAM, is controlled from the MIDAS GUI. The following diagram shows the control window and indicates where further information can be found about the effect of the sliders and buttons in the sections from 3.1 to 3.17.

Note that sliders can be adjusted either by dragging the slider or by typing a text value into the box to the left of the slider and pressing the <enter> key. Buttons toggle their state (on/off) every time they are clicked. Pull down menus are accessed by the left mouse button.

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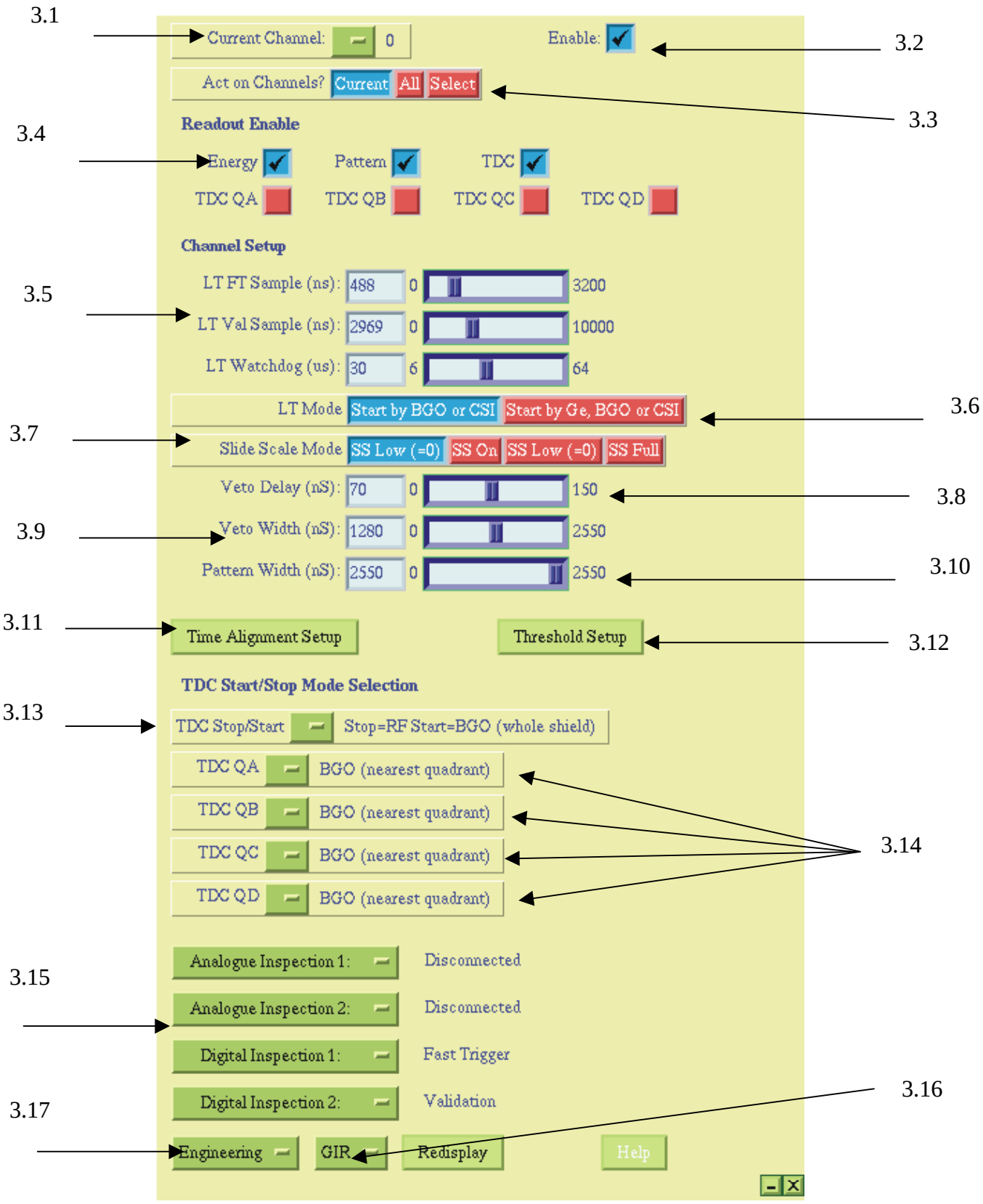

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3.1 Current Channel
A pull down menu to select the channel (numbered 0..15 in EXOGAM) on which this window operates when it shows and controls settings. *(see also 3.3)*

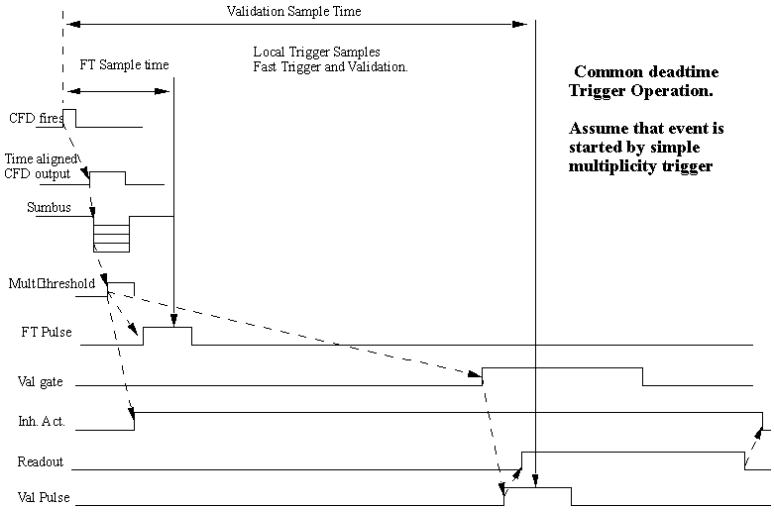
3.2 Enable/Disable
Enables the current channel when ticked. Click again to remove the tick and disable the channel. Disable prevents all Vetos, pattern generation, energy and timing measurements for the channel.

3.3 Act on all channels
These buttons allow changes to the current channel to be applied simultaneously to other channels. Settings updated on the currently displayed channel can optionally be written to either all other ESS channels (All) or a subset selected by tickboxes (Select). The Current setting means that changes affect only the currently displayed channel. Note that the existing settings are not transferred to other channels. Only the changes are applied. The act on All channels is useful if there is no restore file for the experiment and allows the user to set up one channel correctly and then just fine-tune the others by switching back to Current mode. Use with care: it can also destroy all the fine-tuned values by overwriting them. For this reason the All and Select settings are cancelled automatically after each parameter update so that setups are not destroyed inadvertently. Users should also back up working settings regularly using the VXI "Save Card Setup" option in the "VXI Module Control" menu.

3.4 Readout enable
The ESS card generates 7 parameters per channel and these tick boxes control which of the parameters is included in the readout. The following parameters may be read from each channel (each shield):

- Energy: 0 - 20MeV in 4k channels
- Timing A: 0 - 2.5us in 256 channels
- Timing B: 0 - 2.5us in 256 channels
- Timing C: 0 - 2.5us in 256 channels
- Timing D: 0 - 2.5us in 256 channels
- Timing E: 0 - 2.5us in 256 channels
- Pattern: 12 bits (BGO1-4, CsI1-4, Ge1-4)

3.5 Local Trigger timing control
The local trigger sample points for Fast Trigger (FT) and Validation (Val) must be adjusted so that they hit the middle of the Fast Trigger and Validation pulses respectively.



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Users should observe the FT pulse and the FT sample on the logic inspection lines (3.15) while adjusting LT FT sample. Val Pulse and Val sample should be observed while adjusting LT Val Sample. LT watchdog resets the channel in case of an error or a timeout. The diagram above (taken from edoc415) explains the timing relationship between EXOGAM trigger signals.

3.6 Local Trigger Mode

The local trigger is normally started by the OR of the time-aligned BGO/CsI discriminators (Start by BGO or CSI). Sometimes the hit pattern containing Ge CFD outputs is required regardless of whether the shield was hit too. In this case the "Start by Ge, BGO or CSI" button should be pressed instead.

3.7 Sliding scale mode

This should always be set to Sliding Scale on by clicking the SSon button. The other two settings are only used for diagnostics and for sliding scale calibration.

3.8 Veto Delay

The veto pulse delay is set here. The delay of Vetos is adjustable by software to obtain optimum suppression in steps of 10ns from 0 to 160ns. (Common adjustment within each shield.).
Important: the veto is generated using time aligned inputs *(see 3.11)* so alignment delays should be kept as short as possible. The veto pulse is started by the same logic condition used to stop the 4 TDCs TDCQA..D 900ns later. It can be derived from BGO alone, CsI alone or (BGO or CsI). The BGO and/or CsI signals can be taken from either the whole shield or just the nearest neighbour *(see 3.14)*.

3.9 Veto Width

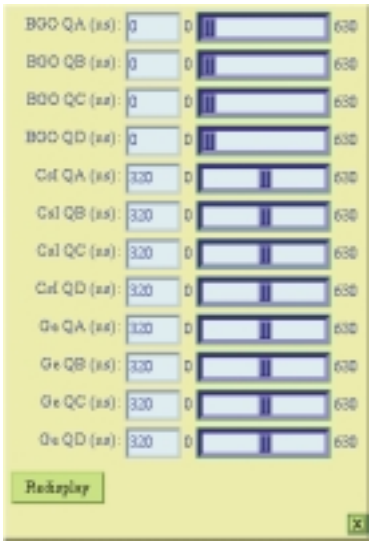
The veto pulse width is set here. The width of Vetos is adjustable by software to obtain optimum suppression in steps of 10ns from 0 to 2.5us. (Common adjustment within each shield.). If the local trigger FT sample fails to hit the FT pulse then a reset is issued by the local trigger which aborts the current veto pulse regardless of the width setting so that the channel is ready for a new event.

3.10 Pattern Width

A 12 bit pattern is generated for each Clover comprising the status of the Ge CFDs, BGO and CsI discriminators during a programmable window. The pattern is generated by starting a local coincidence window when the first of the 12 inputs is detected. The width of the coincidence window is programmable in 10ns steps up to a maximum of 2500ns using this slider. The pattern is generated using time-aligned discriminator signals *(see 3.11)*.

3.11 Time Alignment Setup

Each of the BGO, CsI and Ge inputs can be delayed so that all 12 are time aligned. The outputs are delayed copies of each input signal, delayed by a software selectable period in the range 0 to 560ns, in steps of 10ns. This is in addition to the 70ns delay required to reject noise. So the alignment range is 70ns to 630ns. The pulse width is not affected except to be rounded to the nearest 10ns. The inputs and outputs of this alignment LCA are available on logic inspection lines to enable the users to perform this alignment remotely. The Time alignment adjustment sliders (right) are accessed by clicking Time Alignment Setup.



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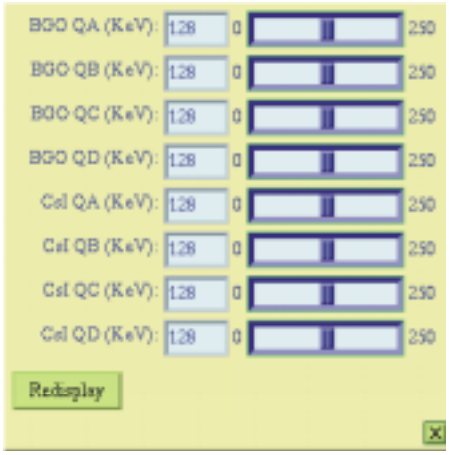
3.12 Threshold setup

Each of the BGO and CsI inputs has its own threshold setting. The threshold adjustment sliders are accessed by clicking the Threshold Setup button.



3.13 Common TDC control

There is one common TDC (2.5µs range, 10ns step size) which is started by one of the following:

- OR of all BGO input discriminators
- OR of all CsI input discriminators
- OR of all BGO + CsI input discriminators
- OR of all Ge CFDs

The TDC stop is generated by one of:

- RF (Beam pulse)
- Fast trigger (back edge)
- OR of all Ge CFDs

This pull down menu selects the stop and start signals for the TDC.

3.14 Quadrant TDC control and Veto logic selection

Each of the Ge crystals sends a CFD input to the ESS card which starts a TDC. The TDC range is 2.5µs with a step size of 10ns. The TDCs are each stopped by a delayed version of one of these logic signals (selected from a pull down menu):

- BGO discriminator output from nearest quarter only
- BGO discriminator output from whole shield
- CsI discriminator output from nearest quarter only
- CsI discriminator output from whole shield
- Logical OR of BGO + CsI discriminator outputs from nearest quarter
- Logical OR of BGO + CsI discriminator outputs from whole shield
- RF (Beam pulse) *NB the VETO is not valid for RF TDC stop*
- Fast trigger (back edge) *NB the VETO is not valid for FT TDC stop*

The delay in the stop signal is not adjustable. Its nominal value is 900ns. If the Ge and the shield fire simultaneously, the TDC measures just the STOP delay of 900ns. The TDC can record shield events up to 900ns before and 1600ns after the Ge fires. (The delay is biased towards the time after the Ge fired so that the slower CsI signals are not lost.)

The TDC stop condition for quadrant n (before the 900ns delay) is also used to generate the Veto for quadrant n, so if the TDC is stopped by RF or FT then the Veto is meaningless. The veto can be derived just from its own quadrant or from the whole shield, using BGO, CsI or both BGO and CsI.

3.15 Inspection line selection
Many of the signals within the ESS card can be observed using the logic and analogue inspection lines. Pull down menus allow the user to select the signals they wish to see on the inspection lines. Previously selected signals are automatically disconnected by the software. The full range of signals available is listed in section 4.2

3.16 GIR control
There are no user controlled items in this menu

3.17 Engineering Menus
There are no user controlled items in these menus.

4 ESS card: further details.

4.1 Energy Measurement Method
The 8 analogue signals in the input stage are integrated using simple integrating shaping amplifiers whose outputs are gated from the time the associated discriminator fires for a period of 1.5µs for BGO and 3µs for CsI. The BGO peak value is held for a further 1.5µs with its gate closed until the CsI input has been integrated for 3µs. The sum of the BGO and CsI peaks is transferred to the ADC. The peak hold capacitors are discharged after the ADC convert command is issued.

The peak detector gate and hold signals are reset by one of the following situations:
- failure of FT or Validation sample point to coincide with FT or Val pulse
- event reject signal being active
- successful completion 3µs charge collection period (normal reset)
- watchdog timeout (error recovery condition)

The energy output is a single sum energy measurement for the whole shield (side and back). The energy range to be measured is 0 to 20MeV to account for direct hits in the CsI back catcher even though the Compton scattered spectra are all in the 0-2MeV range. With a 12 bit ADC this equates to 5keV/channel, so for the minimum discriminator threshold (25keV) the resolution is 20%.

4.2 Inspection Lines
Logic and analogue inspection lines are connected to all important internal signals and may be switched to the VXI bus inspection lines under software control. Appendix A shows typical signals.

Note on software: the hardware is designed such that a write to the parameter (signal) selection register is applied to all channels, and the channel to be enabled is selected via the channel selection register. The 2 registers may be written in either order to achieve the same result after the 2nd write.

4.2.1 Logic Inspection Lines:
Each of the 4 channels has 64 signals (in 3 groups) for use on either (or both) of the two LI lines. The LI line parameter register selects 1 of 64 signals and the channel is chosen by the LI channel registers. LI lines are disconnected by selecting channel 0 (parameter 0 does not disconnect the LI lines). Channels 1-4 select electronics for one of the 4 shields, and channel 5 selects the common LI signals.

Group A (General x32)	Group B (Alignment)	Group C (TDC)
BGO discriminators (x4)	Ge CFD 1 (in)	TDC_QA start
CsI discriminators (x4)	Ge CFD 2 (in)	TDC_QB start
PD Gate BGO	Ge CFD 3 (in)	TDC_QC start
PD Hold/Reset BGO	Ge CFD 4 (in)	TDC_QD start
PD Gate CsI	Ge CFD 1 Aligned (out)	Common TDC start
PD Hold/Reset CsI	Ge CFD 2 Aligned (out)	TDC_QA stop
Veto (x4)	Ge CFD 3 Aligned (out)	TDC_QB stop
Local Trigger (LT) Start	Ge CFD 4 Aligned (out)	TDC_QC stop
LT FT sample	BGO 1 Aligned (out)	TDC_QD stop
LT Val sample	BGO 2 Aligned (out)	Common TDC stop
LT Reset out	BGO 3 Aligned (out)	Any BGO
LT Valack	BGO 4 Aligned (out)	Any CsI
LT Watchdog	CsI 1 Aligned (out)	Any Ge
ADC busy	CsI 2 Aligned (out)	Start Pattern
ADC Clock	CsI 3 Aligned (out)	Pattern Gate
ADC Fail	CsI 4 Aligned (out)	TDC reset in
ADC Output Enable		
Read TDC1-5 (x5)		
Read Pattern		

LI lines for pre-card signals (not per-channel)
Fast Trigger
Validation
Inhibit Action
LT Reset in
Internal readout Data-ready
Internal readout Data-ack
Internal readout daisychain ren-in
Internal readout daisychain last pass

4.2.2 Analogue Inspection lines

Each of the 4 channels has 16 signals (only 13 defined: 3 are spare) for use on either (or both) of the two AI lines. The AI line parameter register selects 1 of 16 signals and the channel is chosen by the AI channel registers. AI lines are disconnected by selecting channel 0 (parameter 0 does not disconnect the AI lines). Channels 1-4 select electronics for one of the 4 shields.

Analogue Inspection x13 signals per channel
BGO input (buffered) x4
CsI input (buffered) x4
BGO Peak
CsI Peak
Sum of BGO+CsI peak
BGO PZ test point
CsI PZ test point

5 Summary of Adjustments

The following list summarises the settings which must be checked and adjusted if necessary by the users of this card. The list includes the names of the inspection lines which allow this parameter to be observed. All inspection lines are logic except those marked *(analogue).* The section number in this document describing how to set the parameter is also listed.

Parameters to set/check before enabling the channel:

Parameter	**Inspection Line(s)**	**Section number**
BGO thresholds (4 per channel)	BGO input QA..D *(analogue)* BGO discr QA..D	3.12
CsI thresholds (4 per channel)	CsI input QA..D *(analogue)* CsI discr QA..D	3.12
BGO input alignments (4 per channel)	BGO discr QA..D BGO-out Aligned QA..D	3.11
CsI input alignments (4 per channel)	CsI discr QA..D CsI-out Aligned QA..D	3.11
Ge CFD input alignments (4 per channel)	Ge CFD-in QA..D Ge CFD-out Aligned QA..D	3.11
LT Mode (1 per channel)	Not required	3.6
SS Mode (1 per channel)	Not required	3.7
Readout enable (7 per channel)	Not required	3.4
Veto delay (1 per channel)	Not required (Veto QA..D)	3.8
Veto width (1 per channel)	Not required (Veto QA..D)	3.9
Pattern width (1 per channel)	Not required (Pattern Gate)	3.10
TDC stop/start selection (5 per channel)	Not required	3.13 and 3.14
LT Watchdog (1 per channel)	Not required	3.5

Parameters to check (and adjust if necessary) after enabling the channel (see 3.2):

Parameter	**Inspection Lines**	**Section number**
LT FT sample (1 per channel)	LT FT sample Fast Trigger	3.5
LT Val sample (1 per channel)	LT Val sample Validation	3.5

Other inspection lines can be used by curious users to monitor what is happening inside the card, but their use is optional.

The shaping amplifiers have "once only" adjustments for offset and pole-zero which are made using potentiometers during commissioning. If errors are observed in pole zero setting or offset the user should ask for help from technical support staff who can adjust the appropriate potentiometers.

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6 Inputs and Outputs (Production ESS Card)

6.1 Front Panel Signals

6.1.1 Inputs:

- Each channel of shield electronics has 8 inputs from the phototubes.

Connector type: 3M SCI coaxial with one RG174 coaxial cable per signal.
Signal Type: Analogue (50 ohm)

Pinout looking at ESS front panel

TOP

CsI_D (16)	GND (15)
GND (14)	CsI_C (13)
CsI_B (12)	GND (11)
GND (10)	CsI_A (9)
BGO_D (8)	GND (7)
GND (6)	BGO_C (5)
BGO_B (4)	GND (3)
GND (2)	BGO_A (1)

(for the prototype card the signals are on pins 1,3,5,7,9,11,13,15. Production cards were changed to match the cables made at GANIL using pinout above.)

- Each channel of shield electronics has 4 inputs from the Ge CFDs.

Connector type: IDC header (twisted pair ribbon cable)
Signal Type: ECL (twisted pair ribbon cable; no input bias network; 50ohm terminations to ground via 100nF capacitor)

Pinout looking at ESS front panel

TOP

Veto_D- (16)	Veto_D+ (15)
Veto_C- (14)	Veto_C+ (13)
Veto_B- (12)	Veto_B+ (11)
Veto_D- (10)	Veto_A +(9)
CFD_D-(8)	CFD_D+ (7)
CFD_C- (6)	CFD_C+ (5)
CFD_B- (4)	CFD_B+ (3)
CFD_A- (2)	CFD_A+ (1)

6.1.2 Outputs:

- Each channel of shield electronics generates 4 Vetos.

Connector type: IDC header (twisted pair ribbon cable)
Signal Type: ECL (twisted pair ribbon cable, 330ohms to -5.2V on each output.)
(see 6.1.1, CFD connections for pinout)

- Each card generates a sumbus output indicating the number of active shields.

Pulse width determined by the width of the Veto pulse.
Connector type: Lemo 00 (2, for daisy chain in/out)
Signal Type: Analogue, 4mA per active shield.

6.1.3 LEDs

"Comfort" LEDS are provided to indicate that discriminators are active.

6.2 Back panel:

The back of the card connects to the VXI bus P1, P2 and P3 uses the GIRV5 board which handles all VME bus cycles for set-up and readout. There are no other back panel connections.

7 Data formats

The ESS data words are formatted using the normal Exogam/Eurogam/Euroball item and group numbers to identify the detector and the parameter to which they refer. The item/group field is programmable. The top 2 data bits are qualifiers. In the ESS card the qualifiers are not used and are set to 0 always.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	Item and group field														Data															

The meanings of the various data words are shown below:

7.1 Pattern

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	CsI D	CsI C	CsI B	CsI A	BGO D	BGO C	BGO B	BGO A	Ge D	Ge C	Ge B	Ge A

7.2 All TDCs

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	Time (0-2550ns in 10ns steps)							

7.3 Energy

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	Sum Energy (BGO+CsI) (12 bits)											

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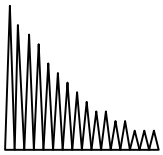
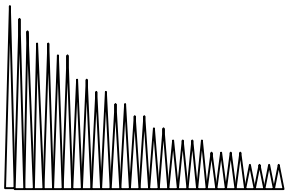
Appendix A: Typical Inspection line signal shapes

All signals shown as they would appear on an oscilloscope connected to the front panel of the resource manager with the oscilloscope channel terminated in 50ohms

A.1 Analogue Inspection lines



BGO input (buffered) x4

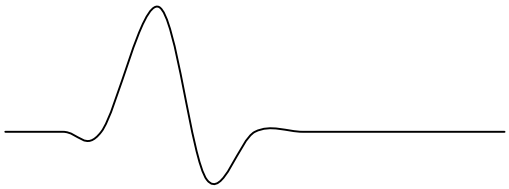


CsI input (buffered) x4

BGO Peak

CsI Peak

Sum of BGO+CsI peak



BGO PZ test point and CsI PZ test point (shown badly adjusted!)

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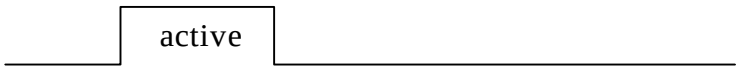
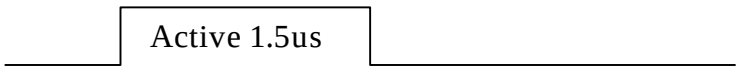
A.2 Logic Inspection lines

These diagrams are drawn to look like the 'scope traces; the higher level is 0V and the lower is -0.8v. The drawings are not to scale although an attempt has been made to show approximate time ordering.

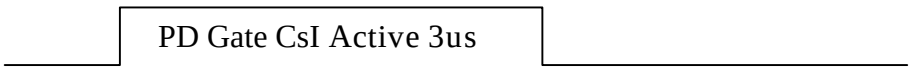


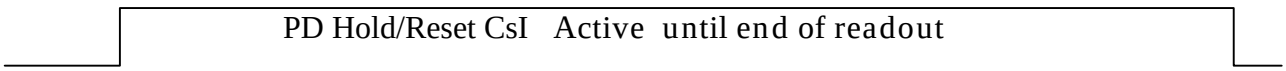
BGO discriminators (x4) and CsI discriminators (x4)

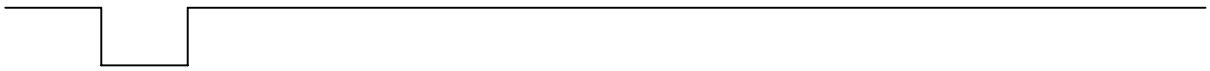


PD Gate BGO

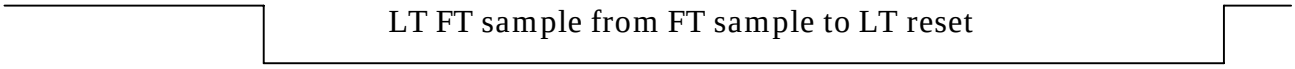
PD Hold/Reset BGO- *No signal (inspection line not used)*

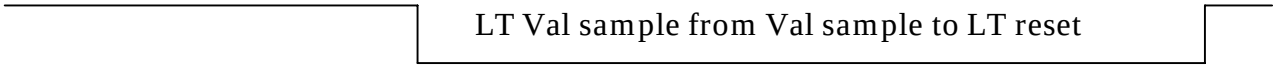


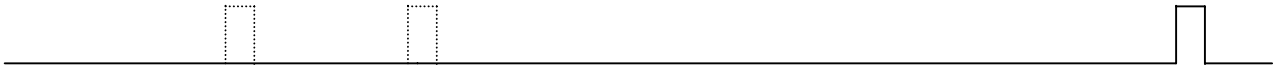




Local Trigger (LT) Start







LT reset out. Normally after readout unless ft/val samples miss ft/val pulses.

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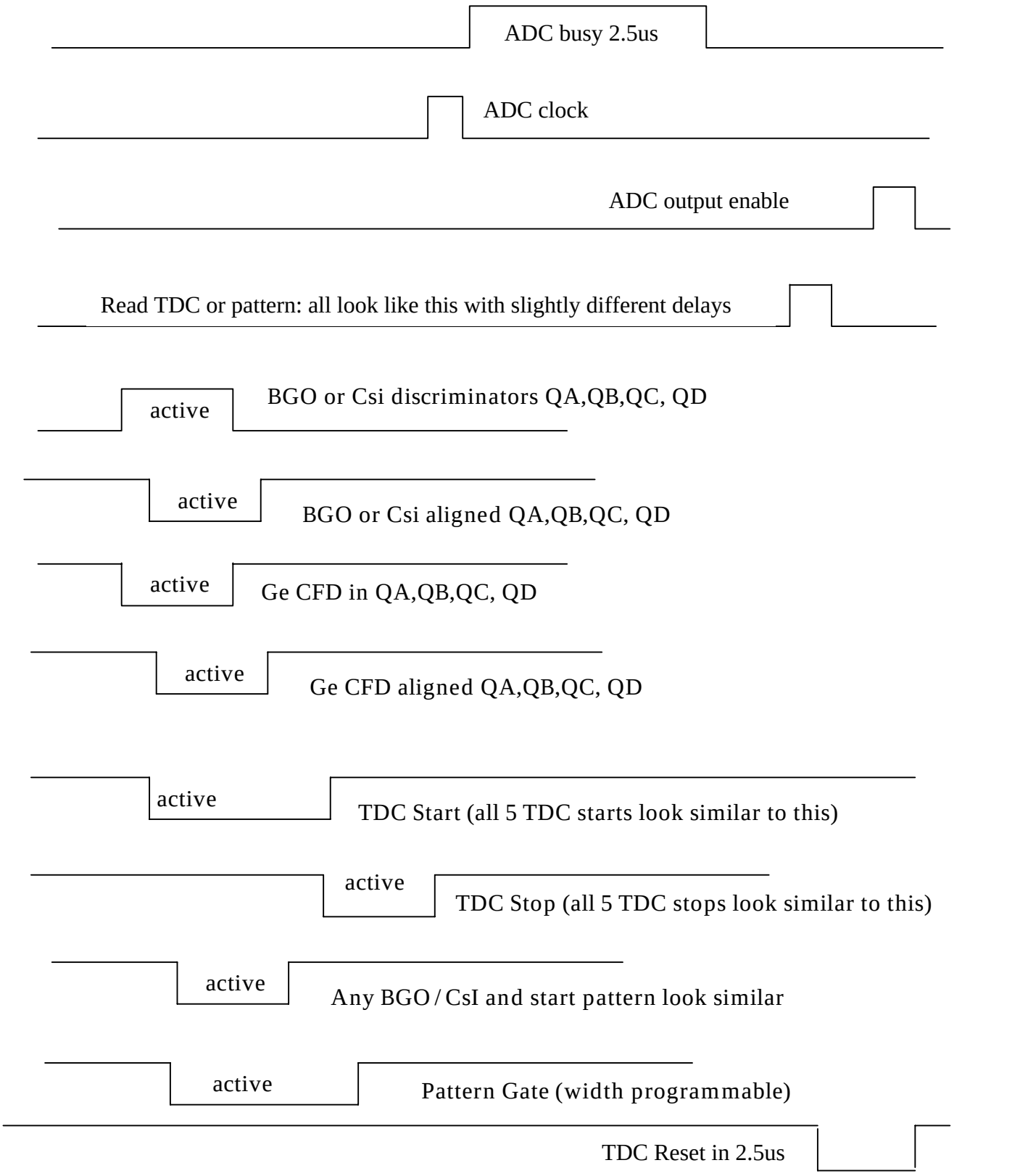

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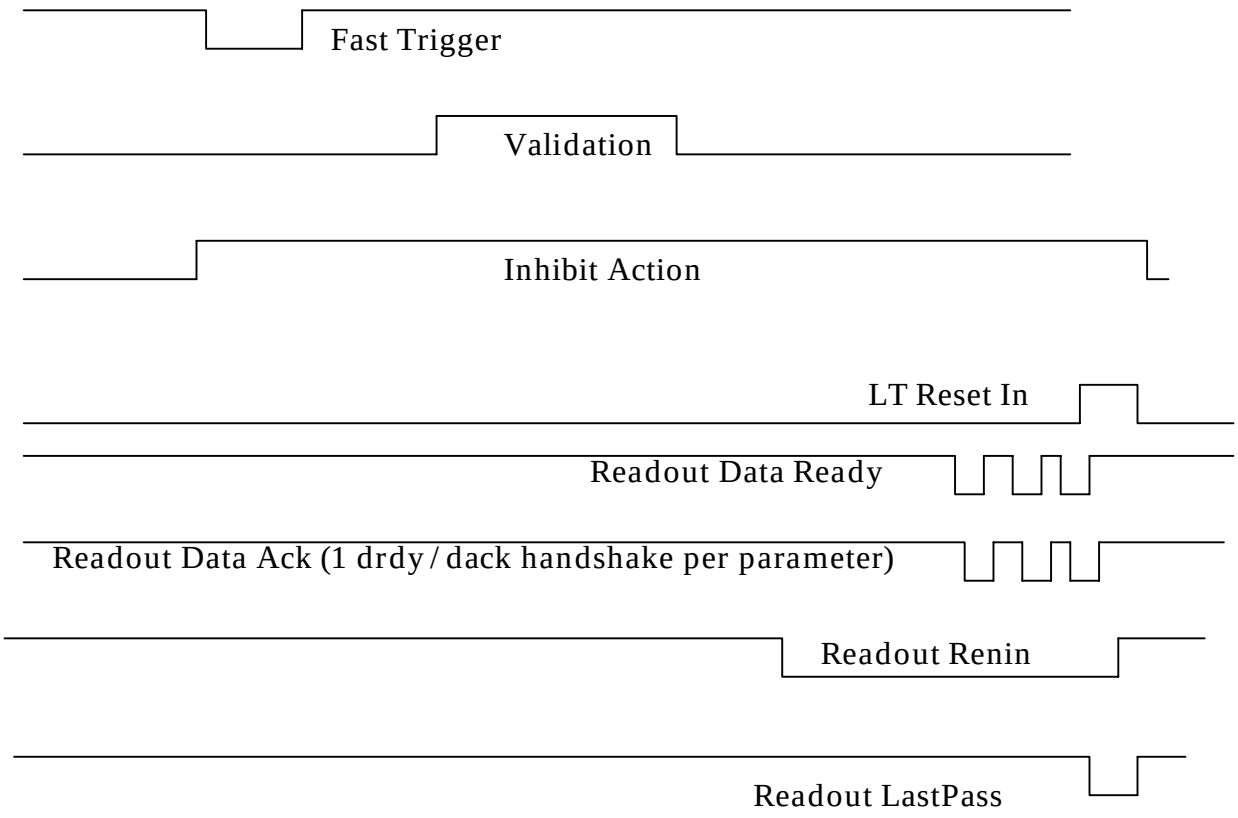
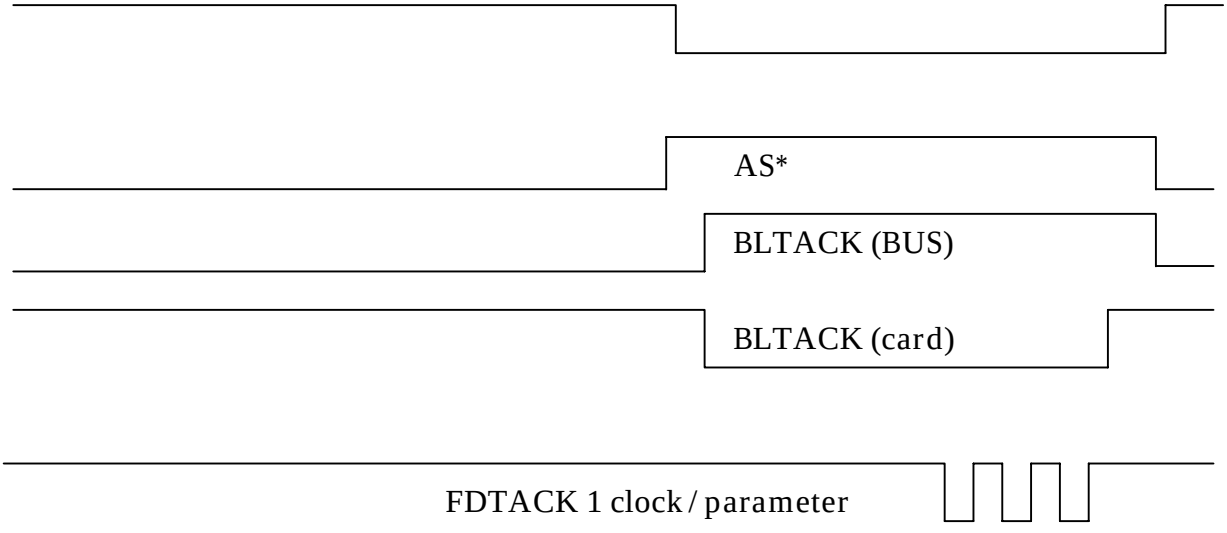


GIR LI lines used during readout:



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